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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | H8SX |
| Core Size | 32-Bit Single-Core |
| Speed | 50MHz |
| Connectivity | EBI/EMI, I²C, IrDA, SCI, SmartCard, USB |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 92 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 56K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 8x10b; D/A 2x8b |
| Oscillator Type | External |
| Operating Temperature | -20°C ~ 75°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LFQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f61668rn50fpv |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 11 | IRQ11F | 0 | R/(W)*1 | [Setting condition] |
| 10 | IRQ10F | 0 | R/(W)*1 | • When the interrupt selected by ISCR occurs |
| 9 | IRQ9F | 0 | R/(W)*1 | [Clearing conditions] |
| 8 | IRQ8F | 0 | R/(W)*1 | • Writing 0 after reading IRQnF = 1 (n = 11 to 0) |
| 7 | IRQ7F | 0 | R/(W)*1 | • When interrupt exception handling is executed while low-level sensing is selected and $\overline{\text{IRQn}}$ input is high |
| 6 | IRQ6F | 0 | R/(W)*1 | |
| 5 | IRQ5F | 0 | R/(W)*1 | • When IRQn interrupt exception handling is executed while falling-, rising-, or both-edge sensing is selected |
| 4 | IRQ4F | 0 | R/(W)*1 | |
| 3 | IRQ3F | 0 | R/(W)*1 | |
| 2 | IRQ2F | 0 | R/(W)*1 | • When the DTC is activated by an IRQn interrupt, and the DISEL bit in MRB of the DTC is cleared to 0 |
| 1 | IRQ1F | 0 | R/(W)*1 | |
| 0 | IRQ0F | 0 | R/(W)*1 | |

Notes: 1. Only 0 can be written, to clear the flag.
2. Supported only by the H8SX/1668M Group.

### 7.3.7 Software Standby Release IRQ Enable Register (SSIER)

SSIER selects the IRQ interrupt used to leave software standby mode.

The IRQ interrupt used to leave software standby mode should not be set as the DTC activation source.

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | SSI15 | — | — | — | SSI11 | SSI10 | SSI9 | SSI8 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | SSI7 | SSI6 | SSI5 | SSI4 | SSI3 | SSI2 | SSI1 | SSI0 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

### (9) DTIF Bit in DMDR

The DTIF bit in DMDR is set to 1 after the total transfer size of transfers is completed. When both the DTIF and DTIE bits in DMDR are set to 1, a transfer end interrupt by the transfer counter is requested to the CPU or DTC.

The DTIF bit is set to 1 when the ACT bit in DMDR is cleared to 0 to stop a transfer after the bus cycle is completed.

The DTIF bit is automatically cleared to 0 and a transfer request is cleared if the transfer is resumed by setting the DTE bit to 1 during interrupt handling.

For details on interrupts, see section 10.8, Interrupt Sources.

## 10.5.8 Priority of Channels

The channels of the DMAC are given following priority levels: channel 0 > channel 1 > channel 2 > channel3. Table 10.6 shows the priority levels among the DMAC channels.

**Table 10.6 Priority among DMAC Channels**

| Channel | Priority |
|---|---|
| Channel 0 | High |
| Channel 1 | |
| Channel 2 | |
| Channel 3 | Low |

The channel having highest priority other than the channel being transferred is selected when a transfer is requested from other channels. The selected channel starts the transfer after the channel being transferred releases the bus. At this time, when a bus master other than the DMAC requests the bus, the cycle for the bus master is inserted.

In a burst transfer or a block transfer, channels are not switched.

### 11.5.10 Bus Cycles in Dual Address Mode

#### (1) Normal Transfer Mode (Cycle Steal Mode)

In cycle steal mode, the bus is released after one byte, word, or longword has been transferred. While the bus is released, one CPU, DMAC, or DTC bus cycle is initiated.

Figure 11.24 shows an example of transfer when $\overline{\text{ETEND}}$ output is enabled, and word-size, normal transfer mode (cycle steal mode) is performed from external 16-bit, 2-state access space to external 16-bit, 2-state access space.

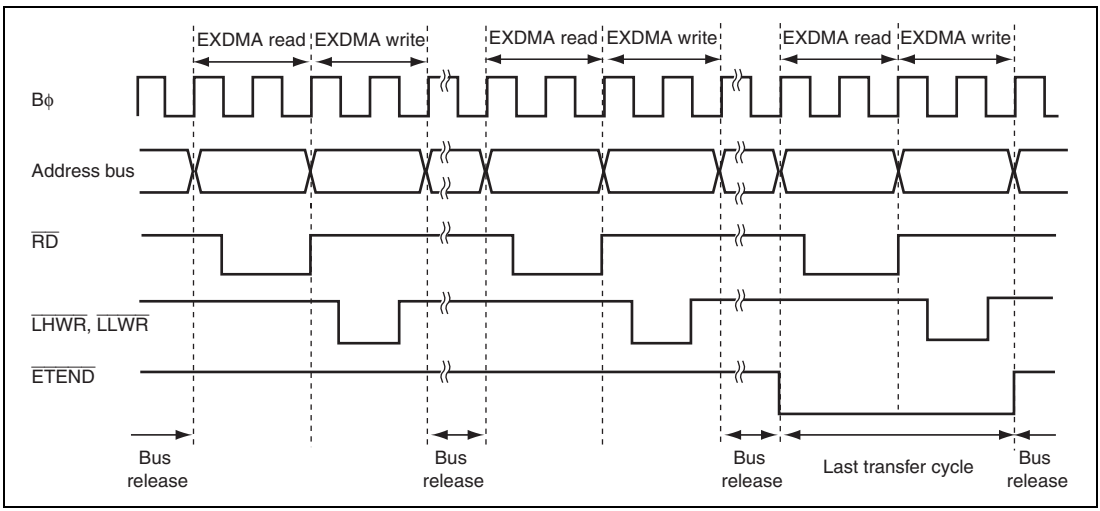



**Figure 11.24 Example of Normal Transfer Mode (Cycle Steal Mode) Transfer**

Figures 11.25 and 11.26 show examples of transfer when $\overline{\text{ETEND}}$ output is enabled, and longword-size, normal transfer mode (cycle steal mode) is performed from external 16-bit, 2-state access space to external 16-bit, 2-state access space.

In figure 11.25, the transfer source (SAR) address is not at a longword boundary and the transfer destination (DAR) address is at the longword boundary.

In figure 11.26, the transfer source (SAR) address is at the longword boundary and the transfer destination (DAR) address is not at the longword boundary.

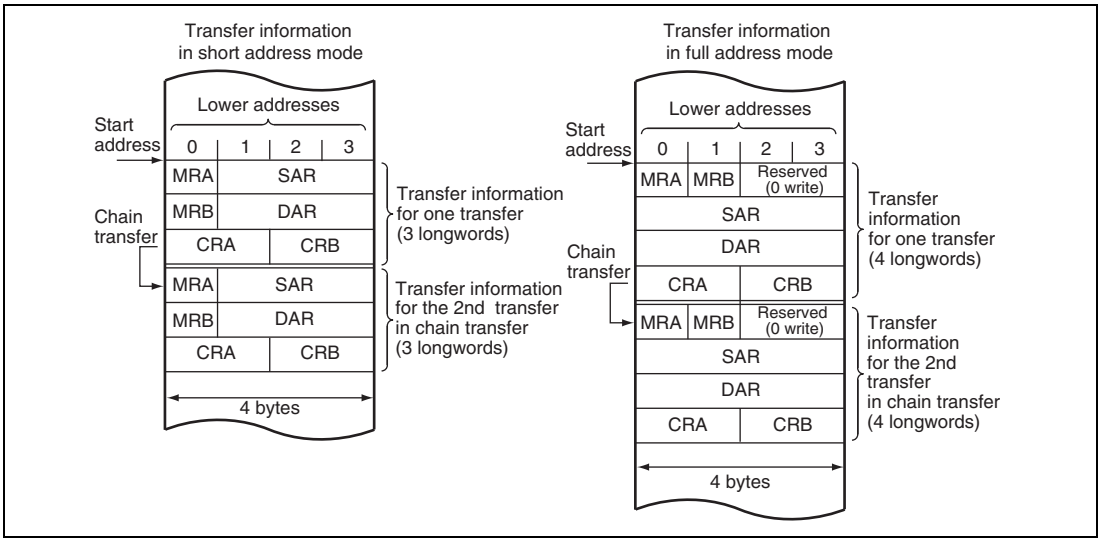



**Figure 12.2 Transfer Information on Data Area**

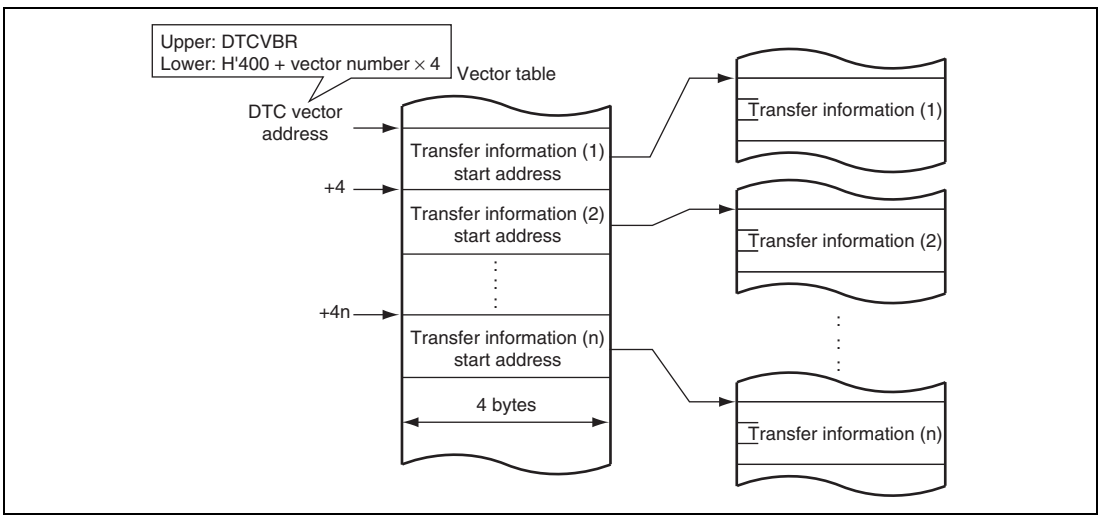



**Figure 12.3 Correspondence between DTC Vector Address and Transfer Information**

**Table 12.7 Register Function in Repeat Transfer Mode**

| | | Written Back Value | |
|---|---|---|---|
| **Register** | **Function** | **CRAL is not 1** | **CRAL is 1** |
| SAR | Source address | Incremented/decremented/fixed * | DTS =0: Incremented/ decremented/fixed*<br>DTS = 1: SAR initial value |
| DAR | Destination address | Incremented/decremented/fixed * | DTS = 0: DAR initial value<br>DTS =1: Incremented/ decremented/fixed* |
| CRAH | Transfer count storage | CRAH | CRAH |
| CRAL | Transfer count A | CRAL – 1 | CRAH |
| CRB | Transfer count B | Not updated | Not updated |

Note: * Transfer information writeback is skipped.

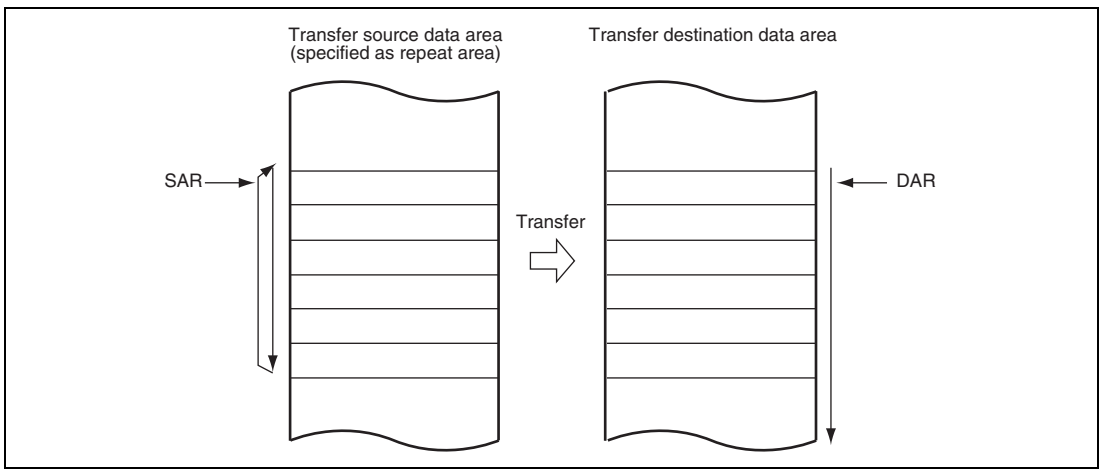



**Figure 12.8 Memory Map in Repeat Transfer Mode (When Transfer Source is Specified as Repeat Area)**

### 13.3.10 Port Function Control Register B (PFCRB)

PFCRB selects the LVD interrupt*, and the input pins for $\overline{\text{IRQ11}}$ to $\overline{\text{IRQ8}}$.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | — | ITS14* | — | — | ITS11 | ITS10 | ITS9 | ITS8 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Note: * Supported only by the H8SX/1668M Group.

- H8SX/1668R Group

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 to 4 | — | All 0 | R/W | Reserved<br>These bits are always read as 0. The write value should always be 0. |

- H8SX/1668M Group

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | — | All 0 | R/W | Reserved<br>This bit is always read as 0. The write value should always be 0. |
| 6 | ITS14 | 0 | R/W | LVD Interrupt Select<br>This bit allows or prohibits LVD interrupt.<br>0: Prohibits LVD interrupt<br>1: Allows LVD interrupt |
| 5, 4 | — | All 0 | R/W | Reserved<br>These bits are always read as 0. The write value should always be 0. |

- Channel 5:
  - Timer control register_5 (TCR_5)
  - Timer mode register_5 (TMDR_5)
  - Timer I/O control register_5 (TIOR_5)
  - Timer interrupt enable register_5 (TIER_5)
  - Timer status register_5 (TSR_5)
  - Timer counter_5 (TCNT_5)
  - Timer general register A_5 (TGRA_5)
  - Timer general register B_5 (TGRB_5)
- Common Registers:
  - Timer start register (TSTR)
  - Timer synchronous register (TSYR)

Unit 1:

- Channel 6:
  - Timer control register_6 (TCR_6)
  - Timer mode register_6 (TMDR_6)
  - Timer I/O control register H_6 (TIORH_6)
  - Timer I/O control register L_6 (TIORL_6)
  - Timer interrupt enable register_6 (TIER_6)
  - Timer status register_6 (TSR_6)
  - Timer counter_6 (TCNT_6)
  - Timer general register A_6 (TGRA_6)
  - Timer general register B_6 (TGRB_6)
  - Timer general register C_6 (TGRC_6)
  - Timer general register D_6 (TGRD_6)

| Bit | Bit Name | Initial value | R/W | Description |
|---|---|---|---|---|
| 7 | TCFD | 1 | R | Count Direction Flag<br>Status flag that shows the direction in which TCNT counts in channels 1, 2, 4, and 5.<br>In channels 0 and 3, bit 7 is reserved. It is always read as 1 and cannot be modified.<br>0: TCNT counts down<br>1: TCNT counts up |
| 6 | — | 1 | — | Reserved<br>This bit is always read as 1 and cannot be modified. |
| 5 | TCFU | 0 | R/(W)* | Underflow Flag<br>Status flag that indicates that a TCNT underflow has occurred when channels 1, 2, 4, and 5 are set to phase counting mode.<br>In channels 0 and 3, bit 5 is reserved. It is always read as 0 and cannot be modified.<br>[Setting condition]<br>When the TCNT value underflows (changes from H'0000 to H'FFFF)<br>[Clearing condition]<br>When a 0 is written to TCFU after reading TCFU = 1<br>(When the CPU is used to clear this flag by writing 0 while the corresponding interrupt is enabled, be sure to read the flag after writing 0 to it.) |
| 4 | TCFV | 0 | R/(W)* | Overflow Flag<br>Status flag that indicates that a TCNT overflow has occurred.<br>[Setting condition]<br>When the TCNT value overflows (changes from H'FFFF to H'0000)<br>[Clearing condition]<br>When a 0 is written to TCFV after reading TCFV = 1<br>(When the CPU is used to clear this flag by writing 0 while the corresponding interrupt is enabled, be sure to read the flag after writing 0 to it.) |

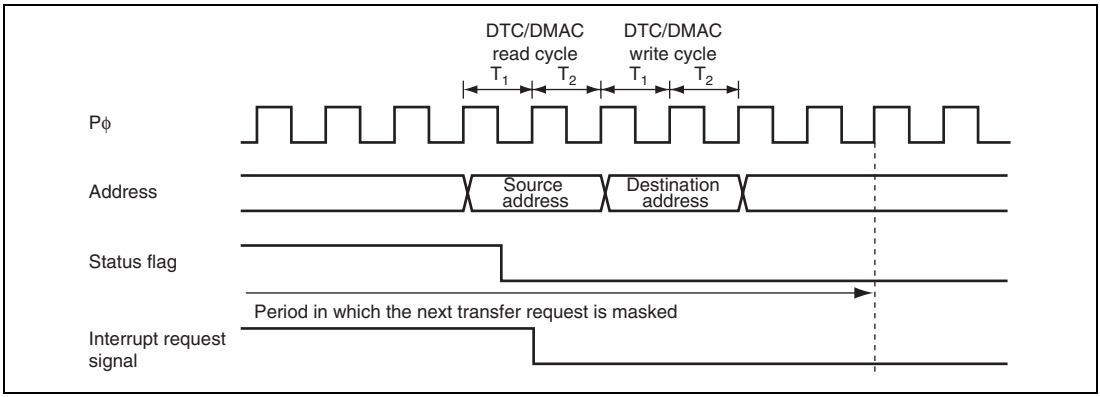



**Figure 14.44 Timing for Status Flag Clearing by DTC/DMAC Activation (1)**

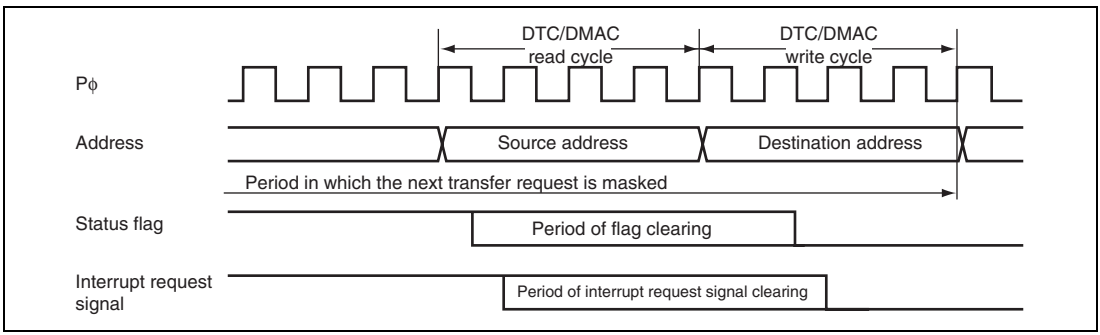



**Figure 14.45 Timing for Status Flag Clearing by DTC/DMAC Activation (2)**

### 18.4.2 Interval Timer Mode

To use the WDT as an interval timer, set the WT/$\overline{IT}$ bit to 0 and the TME bit to 1 in TCSR.

When the WDT is used as an interval timer, an interval timer interrupt (WOVI) is generated each time the TCNT overflows. Therefore, an interrupt can be generated at intervals.

When the TCNT overflows in interval timer mode, an interval timer interrupt (WOVI) is requested at the same time the OVF bit in the TCSR is set to 1.

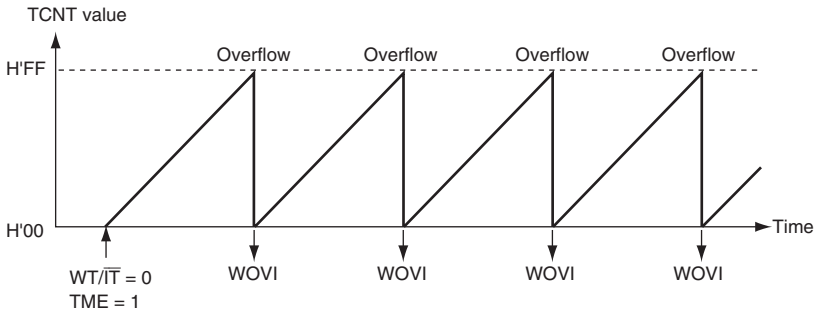



**Figure 18.3 Operation in Interval Timer Mode**

## 18.5 Interrupt Source

During interval timer mode operation, an overflow generates an interval timer interrupt (WOVI). The interval timer interrupt is requested whenever the OVF flag is set to 1 in TCSR. The OVF flag must be cleared to 0 in the interrupt handling routine.

**Table 18.2 WDT Interrupt Source**

| Name | Interrupt Source | Interrupt Flag | DTC Activation |
|---|---|---|---|
| WOVI | TCNT overflow | OVF | Impossible |

### 19.10.7 SCI Operations during Power-Down State

**Transmission:** Before specifying the module stop state or making a transition to software standby mode, stop the transmit operations (TE = TIE = TEIE = 0). TSR, TDR, and SSR are reset. The states of the output pins in the module stop state or in software standby mode depend on the port settings, and the pins output a high-level signal after cancellation. If the transition is made during data transmission, the data being transmitted will be undefined.

To transmit data in the same transmission mode after cancellation of the power-down state, set the TE bit to 1, read SSR, write to TDR, clear TDRE in this order, and then start transmission. To transmit data in a different transmission mode, initialize the SCI first.

Figure 19.39 shows a sample flowchart for transition to software standby mode during transmission. Figures 19.40 and 19.41 show the port pin states during transition to software standby mode.

Before specifying the module stop state or making a transition to software standby mode from the transmission mode using DTC transfer, stop all transmit operations (TE = TIE = TEIE = 0). Setting the TE and TIE bits to 1 after cancellation sets the TXI flag to start transmission using the DTC.

**Reception:** Before specifying the module stop state or making a transition to software standby mode, stop the receive operations (RE = 0). RSR, RDR, and SSR are reset. If transition is made during data reception, the data being received will be invalid.

To receive data in the same reception mode after cancellation of the power-down state, set the RE bit to 1, and then start reception. To receive data in a different reception mode, initialize the SCI first.

For using the IrDA function, set the IrE bit in addition to setting the RE bit.

Figure 19.42 shows a sample flowchart for mode transition during reception.

**Table 20.5 Relationship between Pin Input and TRNTREG1 Monitoring Value**

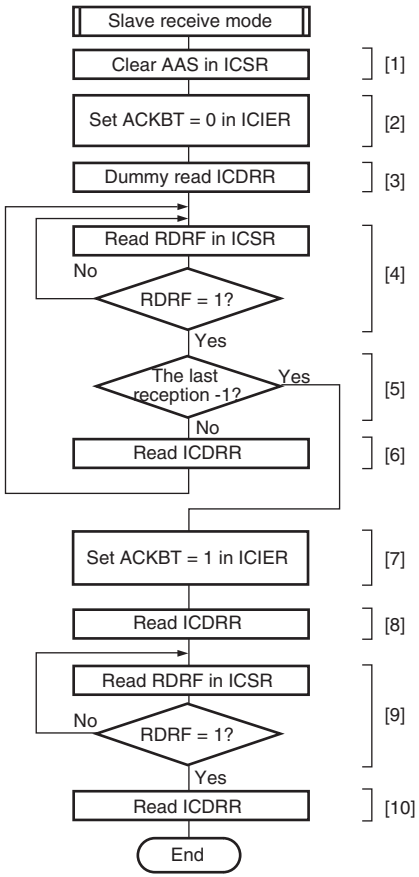
| Register Setting | | Pin Input | | | TRNTREG1 Monitoring Value | | | |
|---|---|---|---|---|---|---|---|---|
| **PTSTE** | **SUSPEND** | **VBUS** | **USD+** | **USD-** | **xver_data** | **dpls** | **dmns** | **Remarks** |
| 0 | X | X | X | X | 0 | 0 | 0 | Cannot be monitored when PTSTE = 0 |
| 1 | 0 | 1 | 0 | 0 | X | 0 | 0 | Can be monitored when PTSTE = 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | |
| 1 | 0 | 1 | 1 | 1 | X | 1 | 1 | |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | |
| 1 | X | 0 | X | X | 0 | 1 | 1 | Can be monitored when VBUS = 0 |

[Legend]

X: Don't care.

The data to be transmitted is written to the data register using this interrupt. After the first transmit data write for one FIFO, the other FIFO is empty, and so the next transmit data can be written to the other FIFO immediately. When both FIFOs are full, EP2 EMPTY is cleared to 0. If at least one FIFO is empty, the EP2EMPTY bit in IFR0 is set to 1. When ACK is returned from the host after data transmission is completed, the FIFO used in the data transmission becomes empty. If the other FIFO contains valid transmit data at this time, transmission can be continued.

When transmission of all data has been completed, write 0 to the EP2EMPTY bit in IER0 and disable interrupt requests.




[1] Clear the AAS flag.*

[2] Set the acknowledge for the transmit device.*

[3] Dummy read ICDRR*

[4] Wait for 1 byte of data to be received*

[5] Detect (last reception -1)*

[6] Read the receive data.*

[7] Set the acknowledge for the last byte.*

[8] Read the receive data of (last byte -1).*

[9] Wait for the reception of the last byte to be completed.

[10] Read the last byte of receive data.

Note: * For one-byte reception, steps [2] to [6] do not need to be executed. After step [1], execute step [7]. In step [8], read ICDRR (dummy read).

**Figure 21.17 Sample Flowchart for Slave Receive Mode**

### (f) Operating Clock Frequency Inquiry

The boot program will return the number of operating clock frequencies, and the maximum and minimum values.

Command

| H'23 |
|---|

- Command, H'23, (one byte): Inquiry regarding operating clock frequencies

Response

| H'33 | Size | Number of operating clock frequencies |
|---|---|---|
| Minimum value of operating clock frequency | | Maximum value of operating clock frequency |
| ... | | |
| SUM | | |

- Response, H'33, (one byte): Response to operating clock frequency inquiry
- Size (one byte): The number of bytes that represents the minimum values, maximum values, and the number of frequencies.
- Number of operating clock frequencies (one byte): The number of supported operating clock frequency types
  (e.g. when there are two operating clock frequency types, which are the main and peripheral clocks, the number of types will be H'02.)
- Minimum value of operating clock frequency (two bytes): The minimum value of the multiplied or divided clock frequency.

  The minimum and maximum values of the operating clock frequency represent the values in MHz, valid to the hundredths place of MHz, and multiplied by 100. (e.g. when the value is 17.00 MHz, it will be 2000, which is H'07D0.)
- Maximum value (two bytes): Maximum value among the multiplied or divided clock frequencies.

  There are as many pairs of minimum and maximum values as there are operating clock frequencies.
- SUM (one byte): Checksum

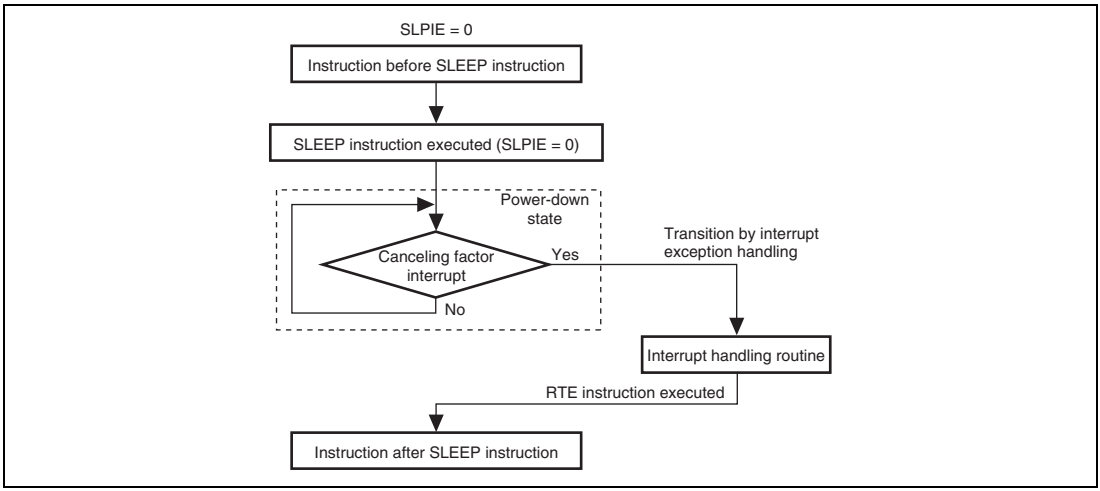



**Figure 28.10 When an Interrupt that Initiates Exit from the Power-Down State is Generated after SLEEP Instruction Execution**

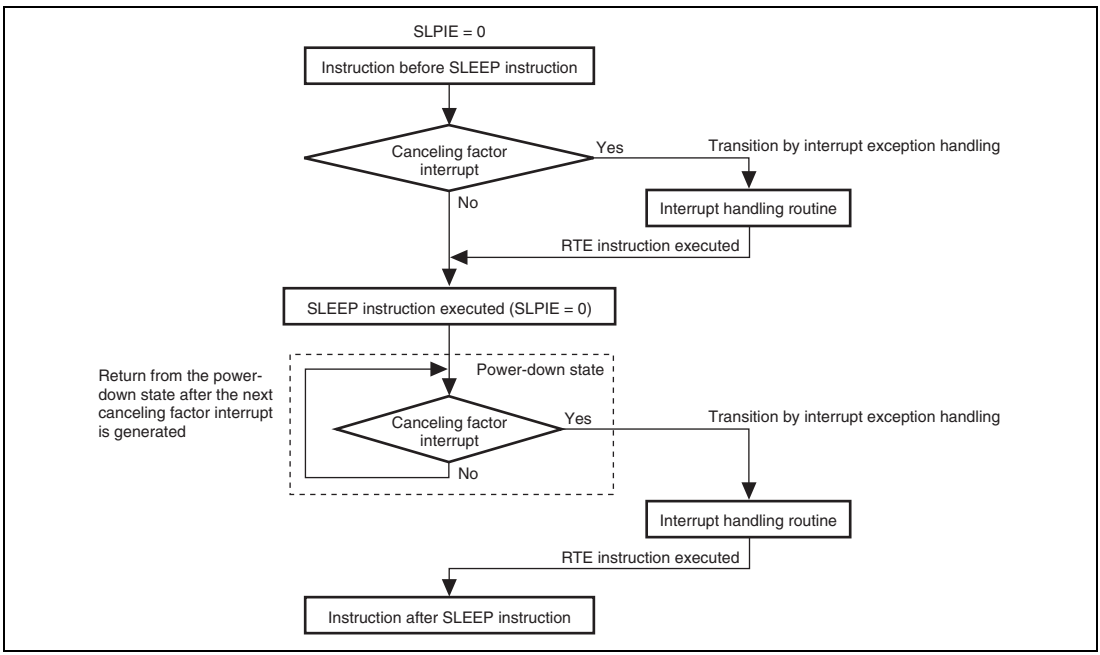



**Figure 28.11 When an Interrupt that Initiates Exit from the Power-Down State is Generated before SLEEP Instruction Execution (Sleep-Instruction Exception Handling does not Proceed)**

# Appendix

## A. Port States in Each Pin State

### Table A.1 Port States in Each Pin State

| Port Name | MCU Operating Mode | Reset | Hardware Standby Mode | Deep Software Standby Mode IOKEEP = 1/0 | | Software Standby Mode | | Bus Released State |
|---|---|---|---|---|---|---|---|---|
| | | | | OPE = 1 | OPE = 0 | OPE = 1 | OPE = 0 | |
| Port 1 | All | Hi-Z | Hi-Z | Keep | Keep | Keep | Keep | Keep |
| Port 2 | All | Hi-Z | Hi-Z | Keep | Keep | Keep | Keep | Keep |
| Port 3 | All | Hi-Z | Hi-Z | Keep | Keep | Keep | Keep | Keep |
| P55 to P50 | All | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Keep |
| P56/ AN6/ DA0/ $\overline{\text{IRQ6}}$-B | All | Hi-Z | Hi-Z | Hi-Z | Hi-Z | [DAOE0 = 1] Keep<br>[DAOE0 = 0] Hi-Z | [DAOE0 = 1] Keep<br>[DAOE0 = 0] Hi-Z | Keep |
| P57/ AN7/ DA1/ $\overline{\text{IRQ7}}$-B | All | Hi-Z | Hi-Z | Hi-Z | Hi-Z | [DAOE1 = 1] Keep<br>[DAOE1 = 0] Hi-Z | [DAOE1 = 1] Keep<br>[DAOE1 = 0] Hi-Z | Keep |
| P65 to P60 | All | Hi-Z | Hi-Z | Keep | Keep | Keep | Keep | Keep |
| PA0/ $\overline{\text{BREQO}}$/ $\overline{\text{BS}}$-A | All | Hi-Z | Hi-Z | [BREQO output]<br>Hi-Z | [BREQO output]<br>Hi-Z | [$\overline{\text{BREQO}}$ output]<br>Hi-Z | [$\overline{\text{BREQO}}$ output]<br>Hi-Z | [$\overline{\text{BREQO}}$ output]<br>$\overline{\text{BREQO}}$ |
| | | | | [$\overline{\text{BS}}$ output]<br>Keep | [$\overline{\text{BS}}$ output]<br>Hi-Z | [$\overline{\text{BS}}$ output]<br>Keep | [$\overline{\text{BS}}$ output]<br>Hi-Z | [$\overline{\text{BS}}$ output]<br>Hi-Z |
| | | | | [Other than above]<br>Keep | [Other than above]<br>Keep | [Other than above]<br>Keep | [Other than above]<br>Keep | [Other than above]<br>Keep |
| PA1/ $\overline{\text{BACK}}$/ (RD/$\overline{\text{WR}}$-A) | All | Hi-Z | Hi-Z | [$\overline{\text{BACK}}$ output]<br>Hi-Z | [$\overline{\text{BACK}}$ output]<br>Hi-Z | [$\overline{\text{BACK}}$ output]<br>Hi-Z | [$\overline{\text{BACK}}$ output]<br>Hi-Z | [$\overline{\text{BACK}}$ output]<br>$\overline{\text{BACK}}$ |
| | | | | [RD/$\overline{\text{WR}}$-A output]<br>Keep | [RD/$\overline{\text{WR}}$-A output]<br>Hi-Z | [RD/$\overline{\text{WR}}$-A output]<br>Keep | [RD/$\overline{\text{WR}}$-A output]<br>Hi-Z | [RD/$\overline{\text{WR}}$-A output]<br>Hi-Z |
| | | | | [Other than above]<br>Keep | [Other than above]<br>Keep | [Other than above]<br>Keep | [Other than above]<br>Keep | [Other than above]<br>Keep |

| Port Name | MCU Operating Mode | Reset | Hardware Standby Mode | Deep Software Standby Mode IOKEEP = 1/0 | | Software Standby Mode | | Bus Released State |
|---|---|---|---|---|---|---|---|---|
| | | | | OPE = 1 | OPE = 0 | OPE = 1 | OPE = 0 | |
| PB6/$\overline{\text{CS6}}$-D/(RD/$\overline{\text{WR}}$)/$\overline{\text{ADTRGH0}}$-B | All | Hi-Z | Hi-Z | [$\overline{\text{CS}}$ output] | [$\overline{\text{CS}}$ output] | [$\overline{\text{CS}}$ output] | [$\overline{\text{CS}}$ output] | [$\overline{\text{CS}}$ output] |
| | | | | H | Hi-Z | H | Hi-Z | Hi-Z |
| | | | | [Other than above] | [Other than above] | [Other than above] | [Other than above] | [Other than above] |
| | | | | Keep | Keep | Keep | Keep | Keep |
| PB7/SDϕ | SDRAM mode | SDϕ output | Hi-Z | [SDϕ output] | [SDϕ output] | [SDϕ output] | [SDϕ output] | [SDϕ output] SDϕ output |
| | | | | H | H | H | H | |
| | Other than SDRAM mode | H | Hi-Z | [Other than above] | [Other than above] | [Other than above] | [Other than above] | [Other than above] |
| | | | | Keep | Keep | Keep | Keep | Keep |
| PC2 to PC3 | All | Hi-Z | Hi-Z | Keep | | Keep | | |