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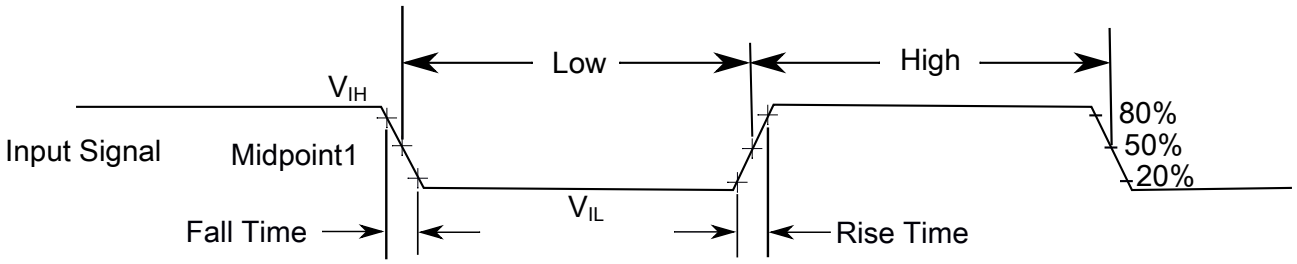
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 5x12b, 3x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk26fn2m0vlq18



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.71 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.71 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICDIO}	Digital[1] input pin negative DC injection current (except RTC_WAKEUP pins) — single pin • V_{IN} < V_{SS}-0.3V	-5	—	mA	2
I_{ICAIO}	Analog[1] input pin DC injection current — single pin • V_{IN} < V_{SS}-0.3V (Negative current injection)	-5	—	mA	2
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pin	-25	—	mA	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• $V_{SS} \le V_{IN} \le V_{DD}$					
$I_{OZ\_RTC\_WAKEUP}$	Hi-Z (off-state) leakage current (per RTC_WAKEUP pin)	—	—	0.25	μA	
R_{PU}	Internal pullup resistors	20	—	50	kΩ	2
R_{PD}	Internal pulldown resistors	20	—	50	kΩ	3

1. Measured at VDD=3.6V
2. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}
3. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx –> RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100MHz
- Bus clock = 50MHz
- FlexBus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode=FEI

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	μs	
	• VLLS0 –> RUN	—	172	μs	
	• VLLS1 –> RUN	—	172	μs	
	• VLLS2 –> RUN	—	94	μs	
	• VLLS3 –> RUN	—	94	μs	
	• LLS2 –> RUN	—	5.8	μs	
	• LLS3 –> RUN	—	5.8	μs	
	• VLPS –> RUN	—	5.4	μs	
	• STOP –> RUN	—	5.4	μs	

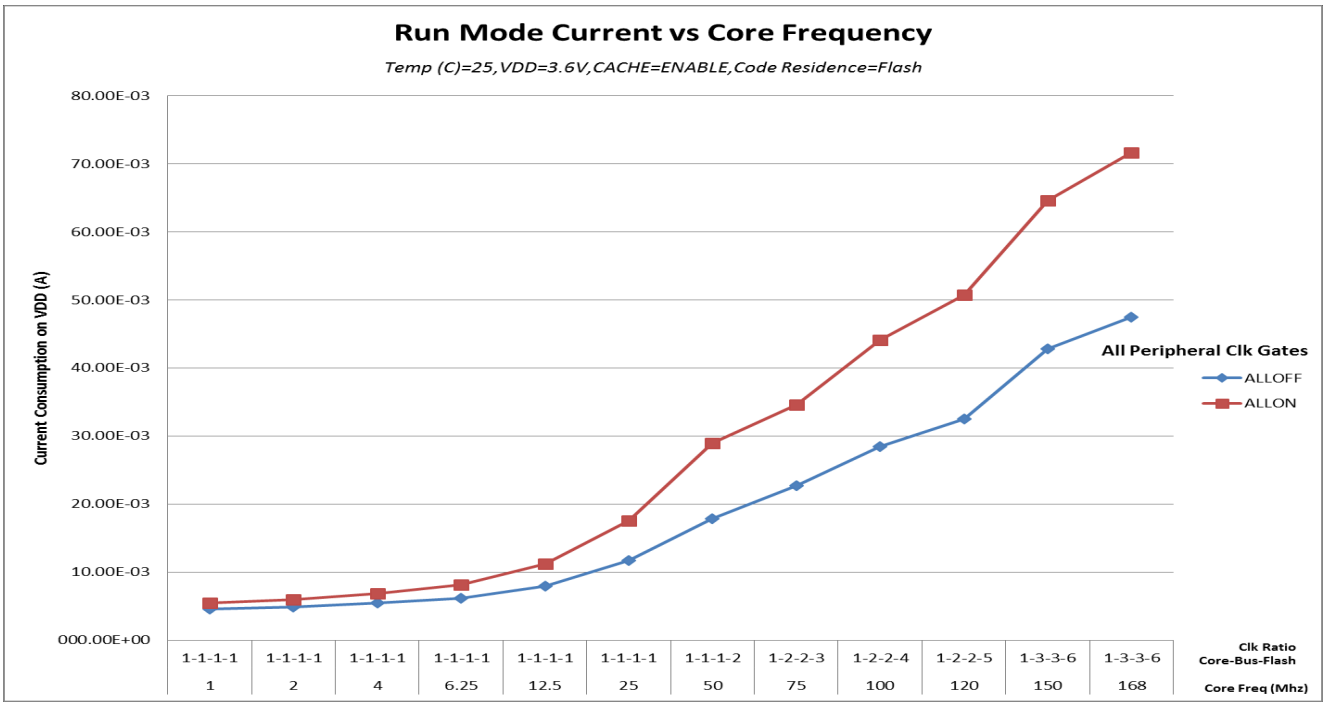


Figure 3. Run mode supply current vs. core frequency

Table 11. General switching specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• $1.71 \le V_{DD} \le 2.7V$	—	7	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	7	ns	
	Port rise and fall time (low drive strength)				5
	• Slew enabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	25	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	15	ns	
	• Slew disabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	7	ns	
	• $2.7 \le V_{DD} \le 3.6V$	—	7	ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. 15 pF load

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 12. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature • For BGA and LQFP package	–40	125	°C	
T_J	Die junction temperature • For CSP package	–40	95	°C	
T_A	Ambient temperature • For BGA and LQFP package	–40	105	°C	1
T_A	Ambient temperature • For CSP package	–40	85	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA}$ x chip power dissipation.

3.1.2 JTAG electricals

Table 14. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	25	
	• Serial Wire Debug	0	50	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	20	—	ns
	• Serial Wire Debug	10	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.0	—	ns
J7	TCLK low to boundary scan output data valid	—	28	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 15. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	20	
	• Serial Wire Debug	0	40	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns

Table continues on the next page...

Table 16. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	10

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. This applies when SCTRIM at value (0x80) and SCFTRIM control bit at value (0x0).
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Excludes any oscillator currents that are also consuming power while PLL is in operation.
9. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
10. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 IRC48M specifications

Table 17. IRC48M specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DD48M}	Supply current	—	520	—	µA	
f_{irc48m}	Internal reference frequency	—	48	—	MHz	
$\Delta f_{irc48m\_ol\_lv}$	Open loop total deviation of IRC48M frequency at low voltage (VDD=1.71V-1.89V) over full temperature • Regulator disable (USB_CLK_RECOVER_IRC_EN[REG_EN]=0) • Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	— —	± 0.4 ± 0.5	± 1.0 ± 1.5	$\%f_{irc48m}$	1
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over 0—70°C • Regulator enable (USB_CLK_RECOVER_IRC_EN[REG_EN]=1)	—	± 0.2	± 0.5	$\%f_{irc48m}$	1
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency at high voltage (VDD=1.89V-3.6V) over full temperature	—	± 0.4	± 1.0	$\%f_{irc48m}$	1

Table continues on the next page...

Table 20. 32kHz oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.4.2 32 kHz oscillator frequency specifications

Table 21. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$f_{ec\_extal32}$	Externally provided input clock frequency	—	32.768	—	kHz	2
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

3.4 Memories and memory interfaces

3.4.1 Flash (FTFE) electrical specifications

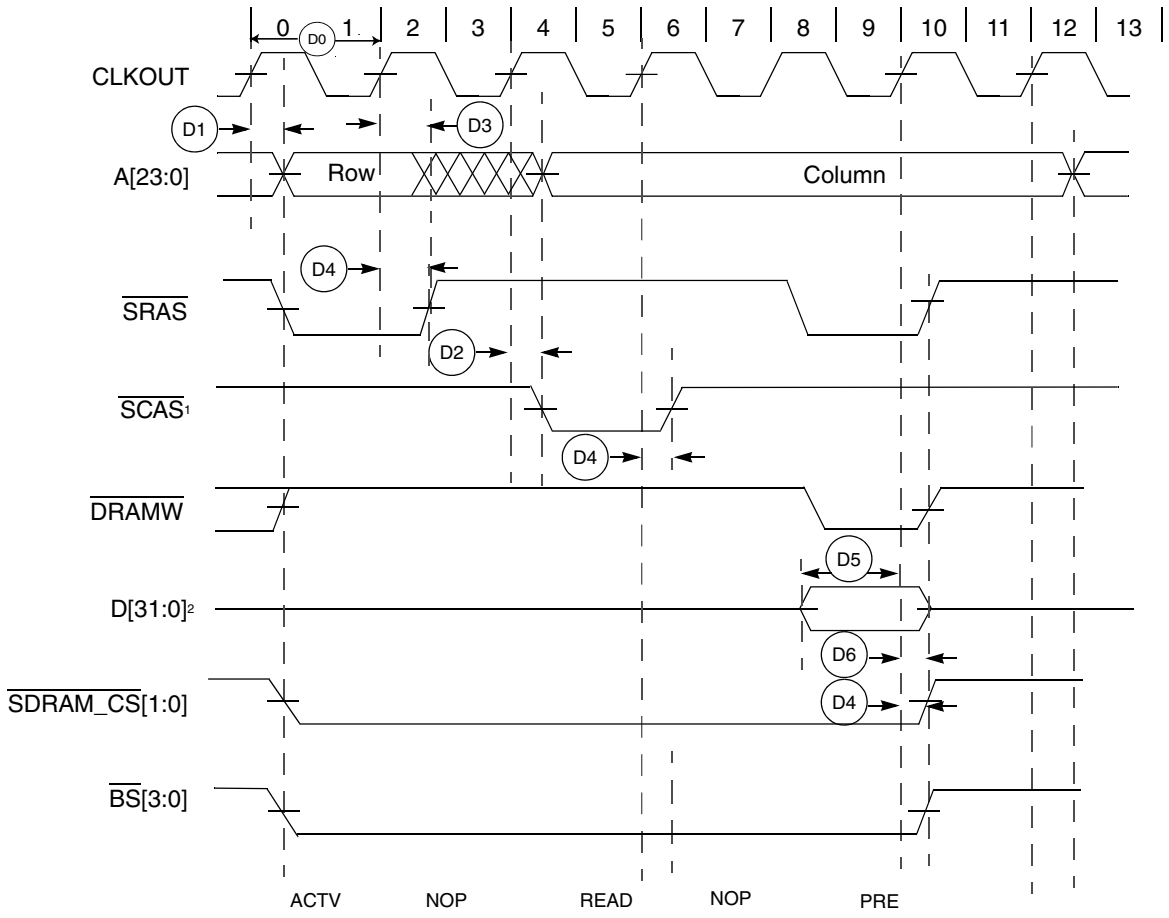
This section describes the electrical characteristics of the FTFE module.

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 22. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm8}	Program Phrase high-voltage time	—	7.5	18	µs	
$t_{hversscr}$	Erase Flash Sector high-voltage time	—	13	113	ms	1
$t_{hversblk256k}$	Erase Flash Block high-voltage time for 256 KB	—	208	1808	ms	1
$t_{hversblk512k}$	Erase Flash Block high-voltage time for 512 KB	—	416	3616	ms	1



1DACR[CASL] = 2
2D[31:16] for 144-pin packages

Figure 15. SDRAM read timing diagram

Table 29. SDRAM Timing (Full voltage range)

NUM	Characteristic [1]	Symbol	Mln	Max	Unit
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	CLKOUT	MHz	
D0	Clock period	1/CLKOUT	—	ns	2
D1	CLKOUT high to SDRAM address valid	t_{CHDAV}	-	11.2	ns
D2	CLKOUT high to SDRAM control valid	t_{CHDCV}		11.1	ns
D3	CLKOUT high to SDRAM address invalid	t_{CHDAI}	1.0	-	ns
D4	CLKOUT high to SDRAM control invalid	t_{CHDCI}	1.0	-	ns
D5	SDRAM data valid to CLKOUT high	t_{DDVCH}	12.0	-	ns
D6	CLKOUT high to SDRAM data invalid	t_{CHDDI}	1.0	-	ns
D7[3]	CLKOUT high to SDRAM data valid	t_{CHDDVW}	-	12.0	ns
D8[3]	CLKOUT high to SDRAM data invalid	t_{CHDDIW}	1.0	-	ns

1. All timing specifications are based on taking into account, a 25pF load on the SDRAM output pins.

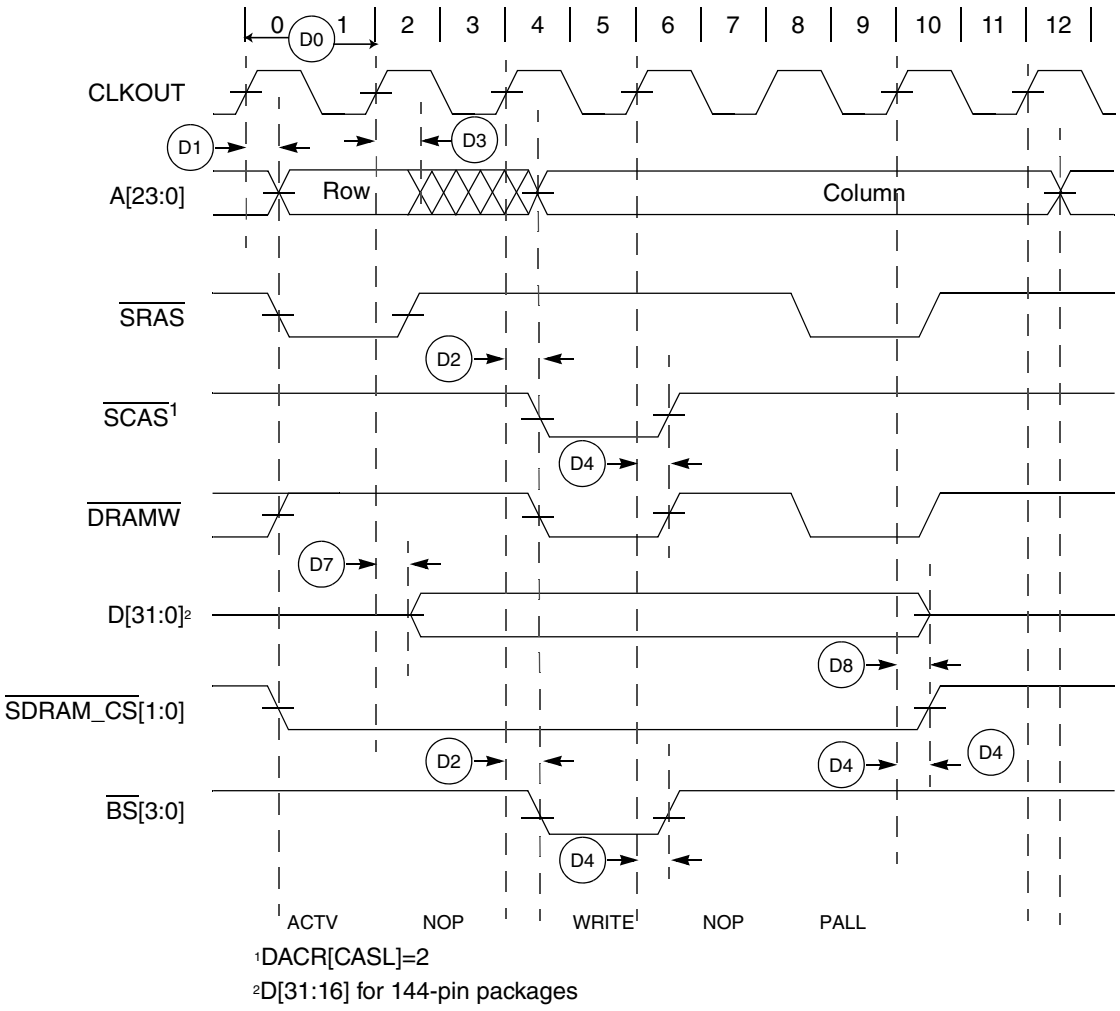


Figure 16. SDRAM write timing diagram

3.5 Analog

3.5.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 31 and Table 32 are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

3.5.2 CMP and 6-bit DAC electrical specifications

Table 33. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

3.7.3 USB DCD electrical specifications

Table 41. USB DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DP_SRC}, V_{DM_SRC}	USB_DP and USB_DM source voltages (up to 250 µA)	0.5	—	0.7	V
V_{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I_{DP_SRC}	USB_DP source current	7	10	13	µA
I_{DM_SINK}, I_{DP_SINK}	USB_DM and USB_DP sink currents	50	100	150	µA
R_{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	kΩ
V_{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

3.7.4 CAN switching specifications

See General switching specifications.

3.7.5 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 42. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	30	MHz	
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 2	—	ns	1
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 2	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	15.0	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	1.0	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15.8	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

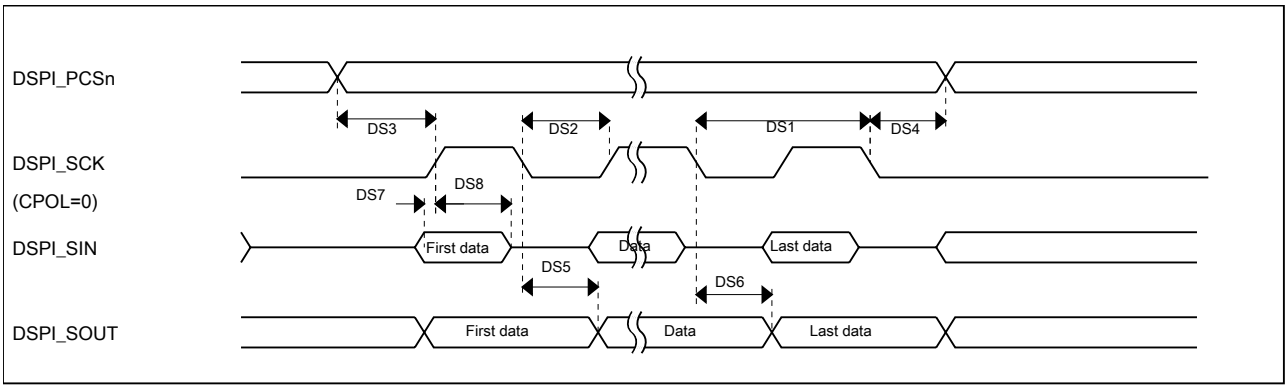


Figure 24. DSPI classic SPI timing — master mode

Table 43. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		15 [1]	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	23.0	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.7	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7.0	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	13	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	13	ns

1. The maximum operating frequency is measured with non-continuous CS and SCK. When DSPI is configured with continuous CS and SCK, there is a constraint that SPI clock should not be greater than 1/6 of bus clock, for example, when bus clock is 60MHz, SPI clock should not be greater than 10MHz.

Table 48. SDHC full voltage range switching specifications (continued)

Num	Symbol	Description	Min.	Max.	Unit
	Card input clock				
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25\50	MHz
	fpp	Clock frequency (MMC full speed\high speed)	0	20\50	MHz
	f_{OD}	Clock frequency (identification mode)	0	400	kHz
SD2	t_{WL}	Clock low time	7	—	ns
SD3	t_{WH}	Clock high time	7	—	ns
SD4	t_{TLH}	Clock rise time	—	3	ns
SD5	t_{THL}	Clock fall time	—	3	ns
	SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD6	t_{OD}	SDHC output delay (output valid)	-5	8.6 8.3	ns
	SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD7	t_{ISU}	SDHC input setup time	5	—	ns
SD8	t_{IH}	SDHC input hold time	0	—	ns

Table 49. SDHC limited voltage range switching specifications

Num	Symbol	Description	Min.	Max.	Unit
		Operating voltage	2.7	3.6	V
	Card input clock				
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25\50	MHz
	fpp	Clock frequency (MMC full speed\high speed)	0	20\50	MHz
	f_{OD}	Clock frequency (identification mode)	0	400	kHz
SD2	t_{WL}	Clock low time	7	—	ns
SD3	t_{WH}	Clock high time	7	—	ns
SD4	t_{TLH}	Clock rise time	—	3	ns
SD5	t_{THL}	Clock fall time	—	3	ns
	SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD6	t_{OD}	SDHC output delay (output valid)	-5	7.6 8.3	ns
	SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD7	t_{ISU}	SDHC input setup time	5	—	ns
SD8	t_{IH}	SDHC input hold time	0	—	ns

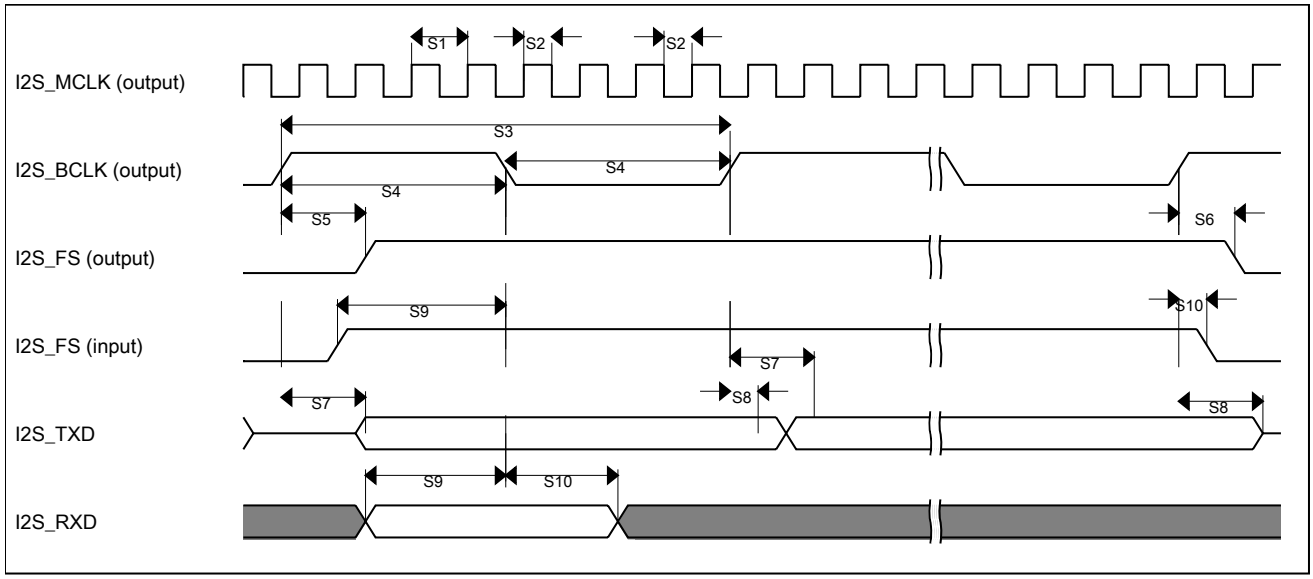


Figure 30. I²S timing — master mode

Table 51. I2S slave mode timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S11	I2S_BCLK cycle time (input)	80	—	ns
S12	I2S_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_FS input setup before I2S_BCLK	4.5	—	ns
S14	I2S_FS input hold after I2S_BCLK	2	—	ns
S15	I2S_BCLK to I2S_TXD/I2S_FS output valid	—	20	ns
S16	I2S_BCLK to I2S_TXD/I2S_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_BCLK	4.5	—	ns
S18	I2S_RXD hold after I2S_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]		25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

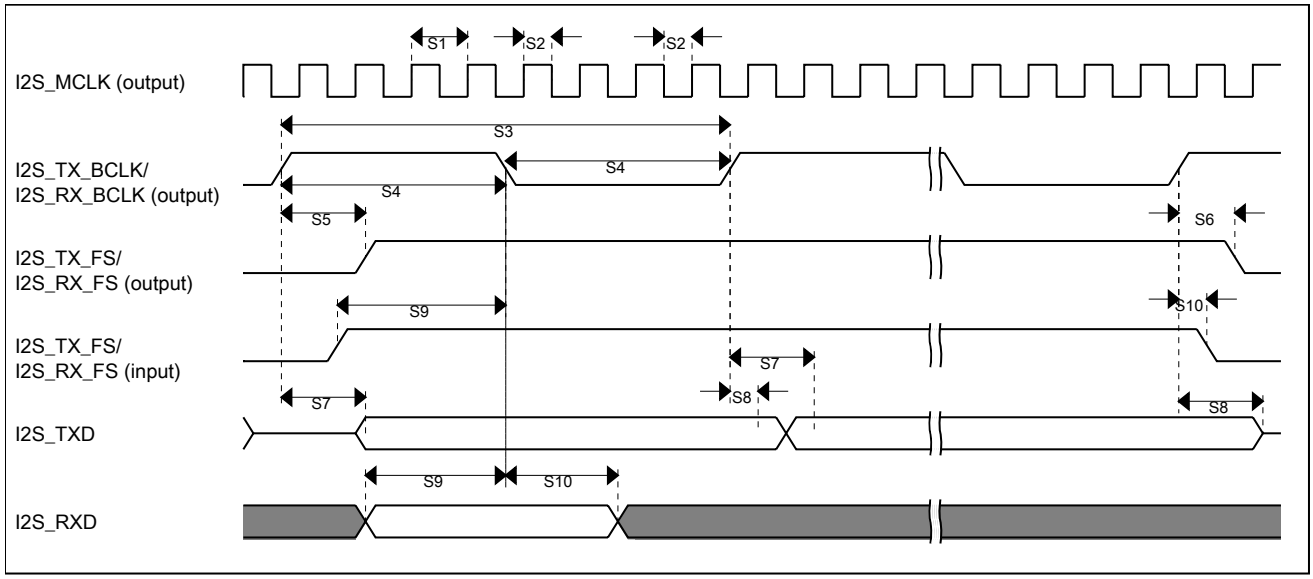


Figure 32. I2S/SAI timing — master modes

Table 53. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	4.5	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	23.1	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	4.5	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

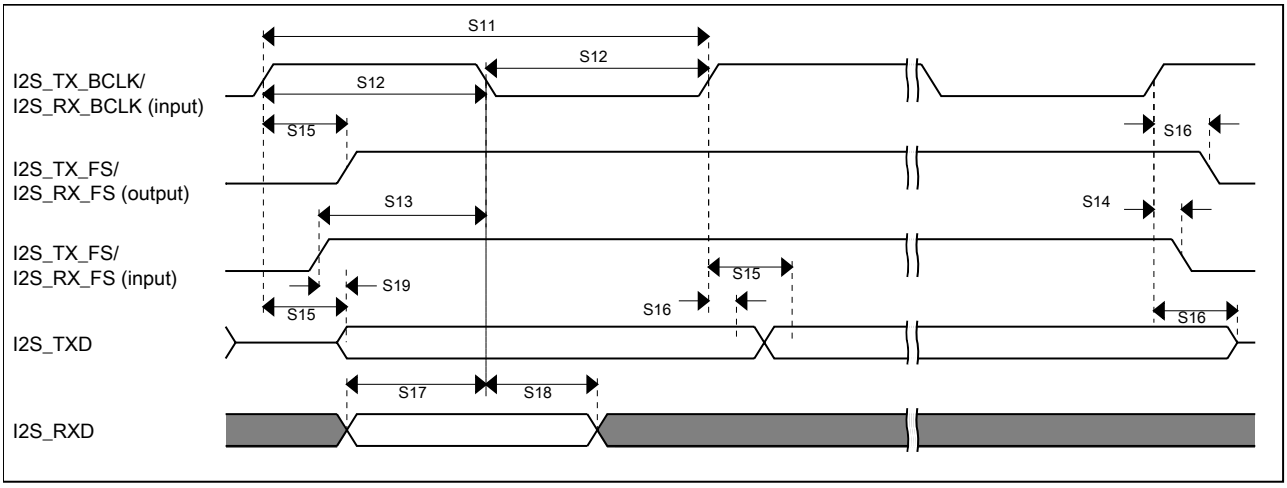


Figure 33. I2S/SAI timing — slave modes

3.7.11.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

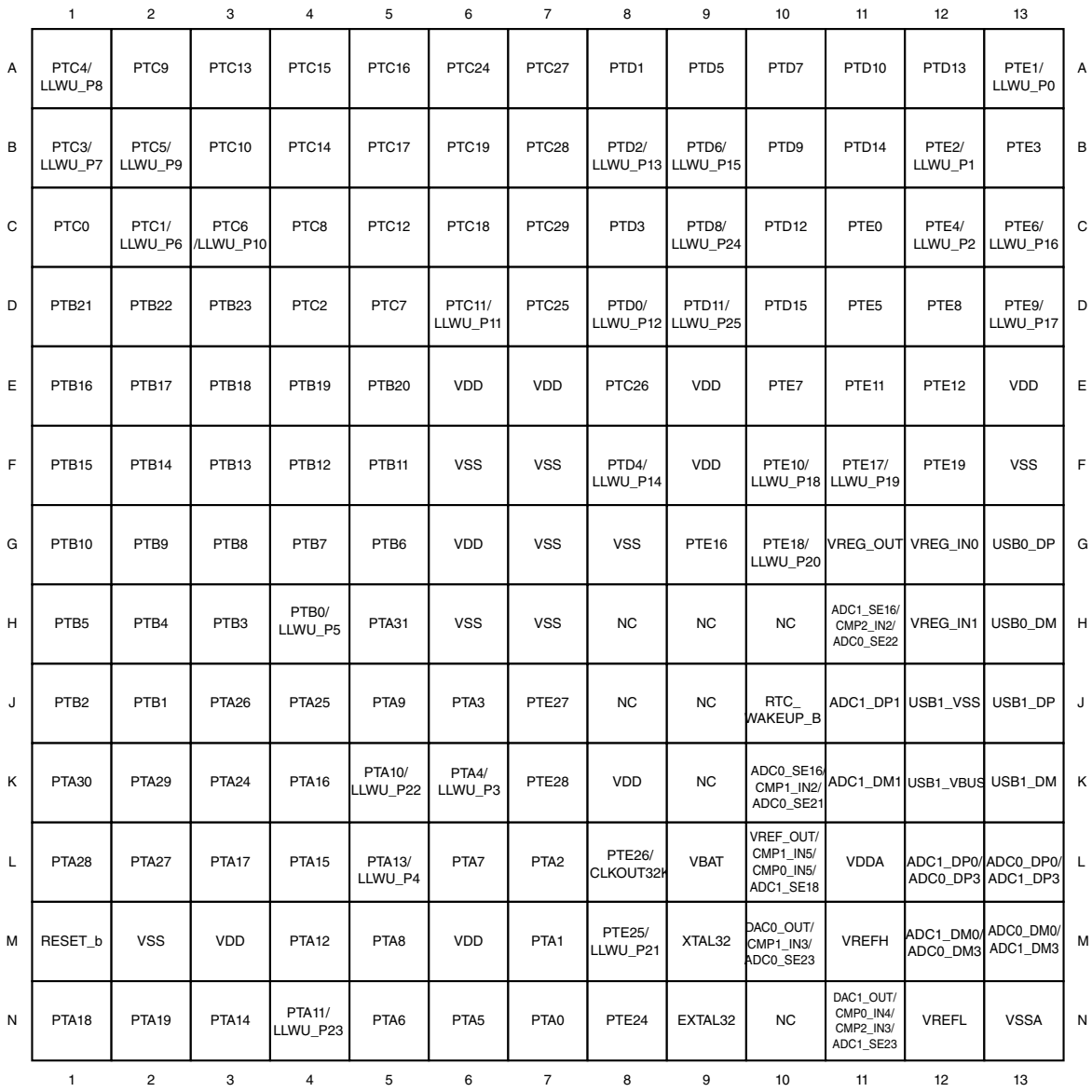
This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 54. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	45	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

169 CSP	169 BGA	144 LQFP	144 BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
H4	G13	81	H10	PTB0/ LLWU_P5	ADC0_SE8/ ADC1_SE8/ TSI0_CH0	ADC0_SE8/ ADC1_SE8/ TSI0_CH0	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0		SDRAM_ CAS_b	FTM1_QD_ PHA/ TPM1_CH0		
J2	G12	82	H9	PTB1	ADC0_SE9/ ADC1_SE9/ TSI0_CH6	ADC0_SE9/ ADC1_SE9/ TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1		SDRAM_ RAS_b	FTM1_QD_ PHB/ TPM1_CH1		
J1	G11	83	G12	PTB2	ADC0_ SE12/ TSI0_CH7	ADC0_ SE12/ TSI0_CH7	PTB2	I2C0_SCL	UART0_ RTS_b		SDRAM_ WE	FTM0_ FLT3		
H3	G10	84	G11	PTB3	ADC0_ SE13/ TSI0_CH8	ADC0_ SE13/ TSI0_CH8	PTB3	I2C0_SDA	UART0_ CTS_b/ UART0_ COL_b		SDRAM_ CS0_b	FTM0_ FLT0		
G7	—	—	—	VSS	VSS	VSS								
G6	—	—	—	VDD	VDD	VDD								
H2	H9	85	G10	PTB4	ADC1_ SE10	ADC1_ SE10	PTB4				SDRAM_ CS1_b	FTM1_ FLT0		
H1	F13	86	G9	PTB5	ADC1_ SE11	ADC1_ SE11	PTB5					FTM2_ FLT0		
G5	F12	87	F12	PTB6	ADC1_ SE12	ADC1_ SE12	PTB6				FB_AD23/ SDRAM_ D23			
G4	F11	88	F11	PTB7	ADC1_ SE13	ADC1_ SE13	PTB7				FB_AD22/ SDRAM_ D22			
G3	F10	89	F10	PTB8	DISABLED		PTB8		UART3_ RTS_b		FB_AD21/ SDRAM_ D21			
G2	F9	90	F9	PTB9	DISABLED		PTB9	SPI1_PCS1	UART3_ CTS_b		FB_AD20/ SDRAM_ D20			
G1	G9	91	E12	PTB10	ADC1_ SE14	ADC1_ SE14	PTB10	SPI1_PCS0	UART3_RX		FB_AD19/ SDRAM_ D19	FTM0_ FLT1		
F5	E13	92	E11	PTB11	ADC1_ SE15	ADC1_ SE15	PTB11	SPI1_SCK	UART3_TX		FB_AD18/ SDRAM_ D18	FTM0_ FLT2		
F4	E12	—	—	PTB12	DISABLED		PTB12	UART3_ RTS_b	FTM1_CH0	FTM0_CH4	FB_A9/ SDRAM_D9	FTM1_QD_ PHA/ TPM1_CH0		
F3	E11	—	—	PTB13	DISABLED		PTB13	UART3_ CTS_b	FTM1_CH1	FTM0_CH5	FB_A8/ SDRAM_D8	FTM1_QD_ PHB/ TPM1_CH1		
F2	E10	—	—	PTB14	DISABLED		PTB14	CAN1_TX			FB_A7/ SDRAM_D7			
F1	E9	—	—	PTB15	DISABLED		PTB15	CAN1_RX			FB_A6/ SDRAM_D6			
—	—	93	H7	VSS	VSS	VSS								

169 CSP	169 BGA	144 LQFP	144 BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
—	—	94	F5	VDD	VDD	VDD								
E1	F8	95	E10	PTB16	TSI0_CH9	TSI0_CH9	PTB16	SPI1_ SOUT	UART0_RX	FTM_ CLKIN0	FB_AD17/ SDRAM_ D17	EWM_IN	TPM_ CLKIN0	
E2	D13	96	E9	PTB17	TSI0_CH10	TSI0_CH10	PTB17	SPI1_SIN	UART0_TX	FTM_ CLKIN1	FB_AD16/ SDRAM_ D16	EWM_ OUT_b	TPM_ CLKIN1	
E3	D12	97	D12	PTB18	TSI0_CH11	TSI0_CH11	PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_ BCLK	FB_AD15/ SDRAM_ A23	FTM2_QD_ PHA/ TPM2_CH0		
E4	D11	98	D11	PTB19	TSI0_CH12	TSI0_CH12	PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_ FS	FB_OE_b	FTM2_QD_ PHB/ TPM2_CH1		
E5	D10	99	D10	PTB20	DISABLED		PTB20	SPI2_PCS0			FB_AD31/ SDRAM_ D31	CMP0_OUT		
D1	D9	100	D9	PTB21	DISABLED		PTB21	SPI2_SCK			FB_AD30/ SDRAM_ D30	CMP1_OUT		
D2	C13	101	C12	PTB22	DISABLED		PTB22	SPI2_ SOUT			FB_AD29/ SDRAM_ D29	CMP2_OUT		
D3	C12	102	C11	PTB23	DISABLED		PTB23	SPI2_SIN	SPI0_PCS5		FB_AD28/ SDRAM_ D28	CMP3_OUT		
C1	B13	103	B12	PTC0	ADC0_ SE14/ TSI0_CH13	ADC0_ SE14/ TSI0_CH13	PTC0	SPI0_PCS4	PDB0_ EXTRG	USB0_ SOF_OUT	FB_AD14/ SDRAM_ A22	I2S0_TXD1		
C2	B12	104	B11	PTC1/ LLWU_P6	ADC0_ SE15/ TSI0_CH14	ADC0_ SE15/ TSI0_CH14	PTC1/ LLWU_P6	SPI0_PCS3	UART1_ RTS_b	FTM0_CH0	FB_AD13/ SDRAM_ A21	I2S0_TXD0		
D4	A13	105	A12	PTC2	ADC0_ SE4b/ CMP1_IN0/ TSI0_CH15	ADC0_ SE4b/ CMP1_IN0/ TSI0_CH15	PTC2	SPI0_PCS2	UART1_ CTS_b	FTM0_CH1	FB_AD12/ SDRAM_ A20	I2S0_TX_ FS		
B1	A12	106	A11	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_ BCLK		
F6	C11	107	H8	VSS	VSS	VSS								
E6	H6	108	—	VDD	VDD	VDD								
A1	B11	109	A9	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11/ SDRAM_ A19	CMP1_OUT		
B2	A11	110	D8	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	I2S0_RXD0	FB_AD10/ SDRAM_ A18	CMP0_OUT	FTM0_CH2	
C3	A10	111	C8	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_ SOUT	PDB0_ EXTRG	I2S0_RX_ BCLK	FB_AD9/ SDRAM_ A17	I2S0_MCLK		



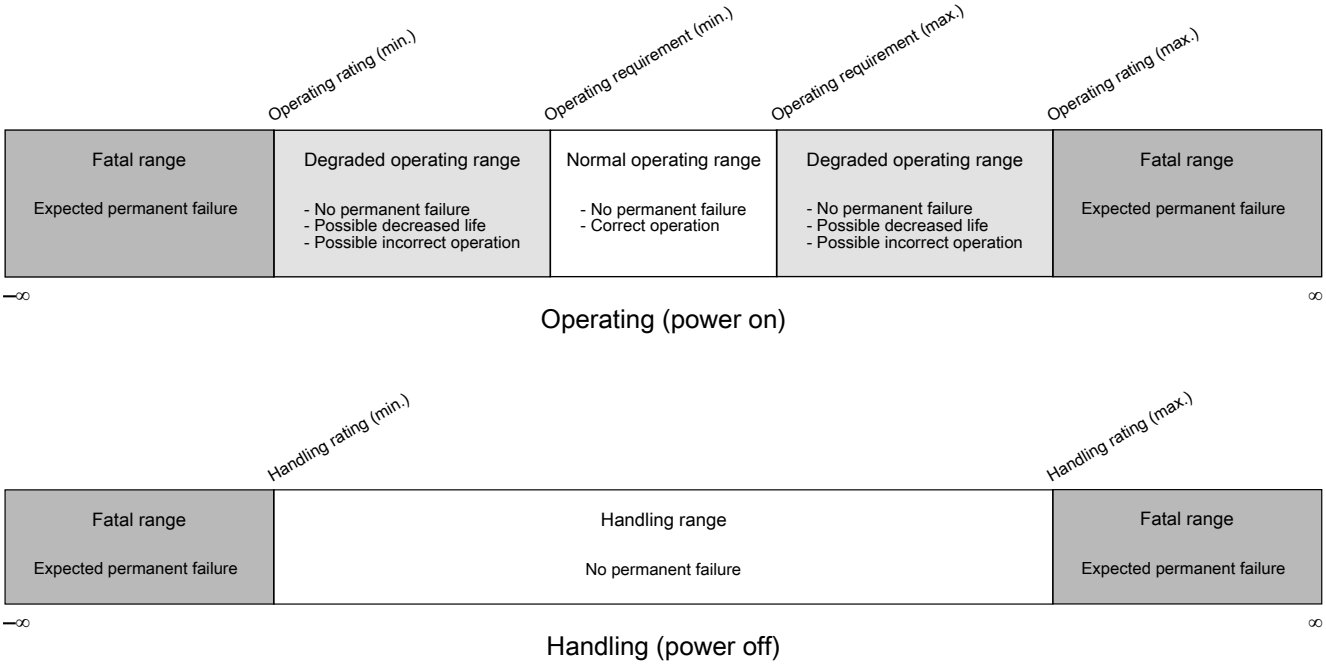
	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	PTC4/ LLWU_P8	PTC9	PTC13	PTC15	PTC16	PTC24	PTC27	PTD1	PTD5	PTD7	PTD10	PTD13	PTE1/ LLWU_P0	A
B	PTC3/ LLWU_P7	PTC5/ LLWU_P9	PTC10	PTC14	PTC17	PTC19	PTC28	PTD2/ LLWU_P13	PTD6/ LLWU_P15	PTD9	PTD14	PTE2/ LLWU_P1	PTE3	B
C	PTC0	PTC1/ LLWU_P6	PTC6 /LLWU_P10	PTC8	PTC12	PTC18	PTC29	PTD3	PTD8/ LLWU_P24	PTD12	PTE0	PTE4/ LLWU_P2	PTE6/ LLWU_P16	C
D	PTB21	PTB22	PTB23	PTC2	PTC7	PTC11/ LLWU_P11	PTC25	PTD0/ LLWU_P12	PTD11/ LLWU_P25	PTD15	PTE5	PTE8	PTE9/ LLWU_P17	D
E	PTB16	PTB17	PTB18	PTB19	PTB20	VDD	VDD	PTC26	VDD	PTE7	PTE11	PTE12	VDD	E
F	PTB15	PTB14	PTB13	PTB12	PTB11	VSS	VSS	PTD4/ LLWU_P14	VDD	PTE10/ LLWU_P18	PTE17/ LLWU_P19	PTE19	VSS	F
G	PTB10	PTB9	PTB8	PTB7	PTB6	VDD	VSS	VSS	PTE16	PTE18/ LLWU_P20	VREG_OUT	VREG_IN0	USB0_DP	G
H	PTB5	PTB4	PTB3	PTB0/ LLWU_P5	PTA31	VSS	VSS	NC	NC	NC	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	VREG_IN1	USB0_DM	H
J	PTB2	PTB1	PTA26	PTA25	PTA9	PTA3	PTE27	NC	NC	RTC_ WAKEUP_B	ADC1_DP1	USB1_VSS	USB1_DP	J
K	PTA30	PTA29	PTA24	PTA16	PTA10/ LLWU_P22	PTA4/ LLWU_P3	PTE28	VDD	NC	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	ADC1_DM1	USB1_VBUS	USB1_DM	K
L	PTA28	PTA27	PTA17	PTA15	PTA13/ LLWU_P4	PTA7	PTA2	PTE26/ CLKOUT32K	VBAT	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VDDA	ADC1_DP0/ ADC0_DP3	ADC0_DP0/ ADC1_DP3	L
M	RESET_b	VSS	VDD	PTA12	PTA8	VDD	PTA1	PTE25/ LLWU_P21	XTAL32	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	VREFH	ADC1_DM0/ ADC0_DM3	ADC0_DM0/ ADC1_DM3	M
N	PTA18	PTA19	PTA14	PTA11/ LLWU_P23	PTA6	PTA5	PTA0	PTE24	EXTAL32	NC	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	VREFL	VSSA	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Figure 39. MK26 169 CSP Pinout Diagram

6 Ordering parts

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	Supply voltage	3.3	V

8.4 Relationship between ratings and operating requirements



8.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

9 Revision History

The following table provides a revision history for this document.