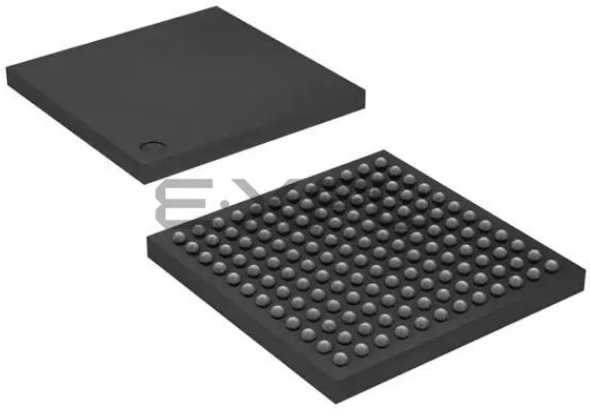

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	100
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 5x12b, 3x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LBGA
Supplier Device Package	144-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk26fn2m0vmd18

1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	• For C-temp variant: 1 • For V-temp variant :3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

2.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{OH}	Output high voltage — normal drive pad					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -10mA	V_{DD} – 0.5	—	—	V	
	• 1.71 V ≤V_{DD} ≤ 2.7 V, I_{OH} = -5mA	V_{DD} – 0.5	—	—	V	
	Output high voltage — High drive pad					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -20mA	V_{DD} – 0.5	—	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -10mA	V_{DD} – 0.5	—	—	V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	
$V_{OH\_RTC\_WAKEUP}$	Output high voltage— normal drive pad				V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -5 mA	V_{BAT} – 0.5	—		V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -2.5 mA	V_{BAT} – 0.5	—			
$I_{OH\_RTC\_WAKEUP}$	Output high current total for RTC_WAKEUP pins	—	—	100	mA	
V_{OL}	Output low voltage — normal drive pad					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 10 mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 5 mA	—	—	0.5	V	
	Output low voltage — high drive pad					
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 20 mA	—	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 10 mA	—	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
$V_{OL\_RTC\_WAKEUP}$	Output low voltage— normal drive pad				V	
	• 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 5 mA	—		0.5	V	
	• 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 2.5mA	—		0.5		
$I_{OL\_RTC\_WAKEUP}$	Output low current total for RTC_WAKEUPpins	—	—	100	mA	
I_{IN}	Input leakage current, analog and digital pins	—	0.002	0.5	µA	1

Table continues on the next page...

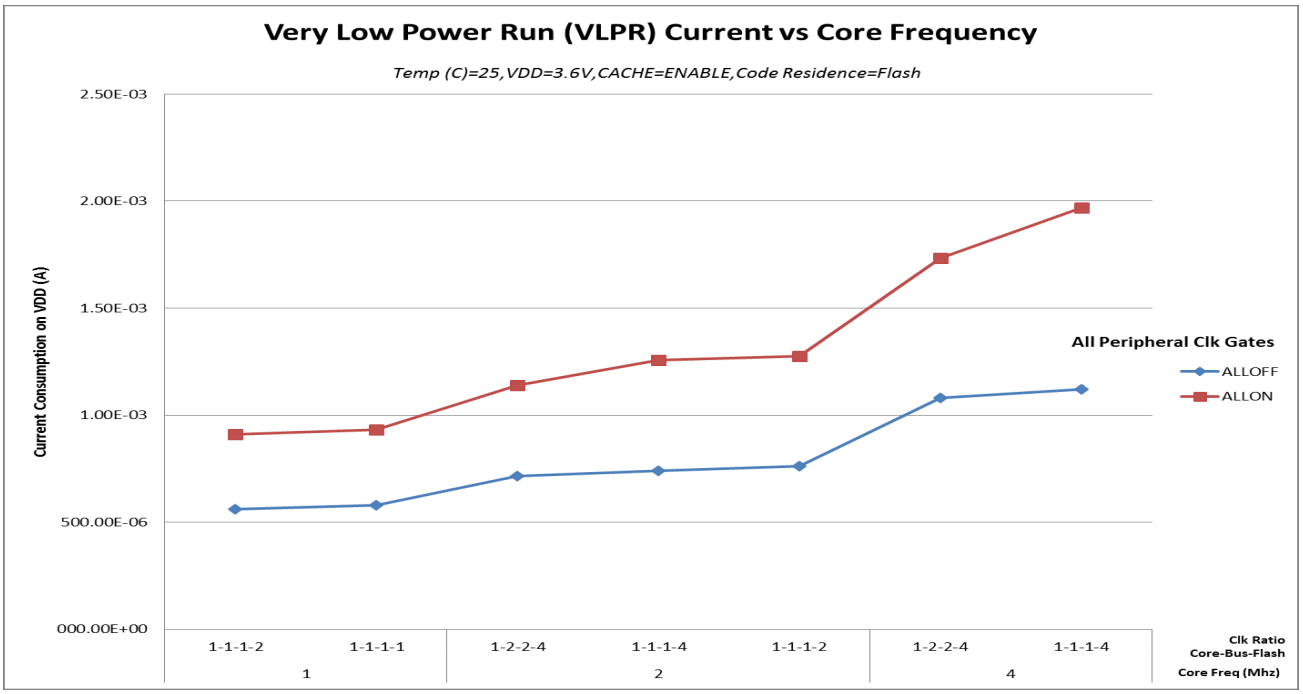

Figure 4. VLPR mode supply current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

Table 8. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	23	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	27	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	28	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	14	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	K	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic

2.4.2 Thermal attributes

Board type	Symbol	Description	144 LQFP	144 MAPBGA	169 MAPBGA	169 WLCSP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	45	48	38	48.3	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	36	29	21.9	24	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	36	38	30	39.8	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	30	25	18.6	19.5	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	24	16	14.4	21.4	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	9	9	8.2	0.1	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	2	0.2	0.2	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.

3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 Debug trace timing specifications

Table 13. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	1.5	—	ns
T_h	Data hold	1.0	—	ns

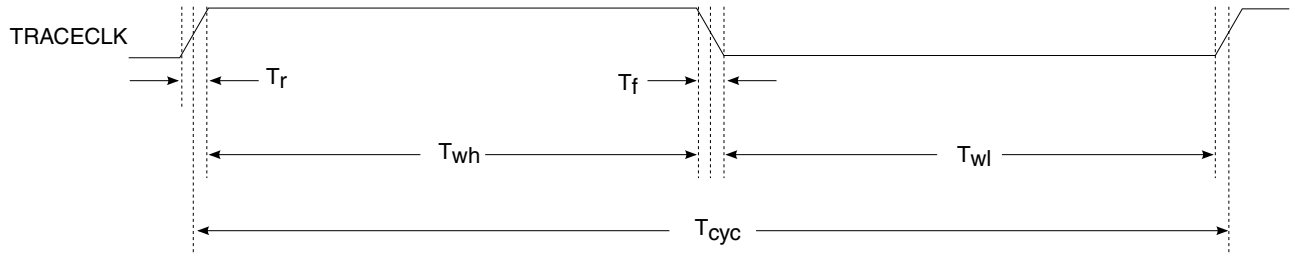

Figure 5. TRACE_CLKOUT specifications

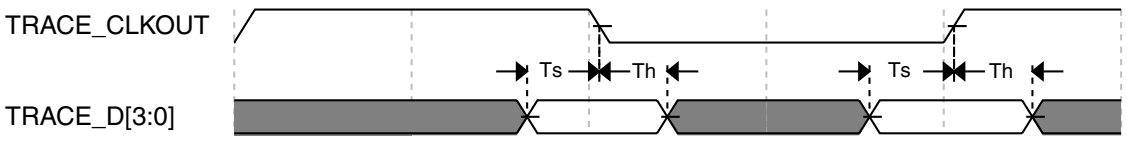

Figure 6. Trace data specifications

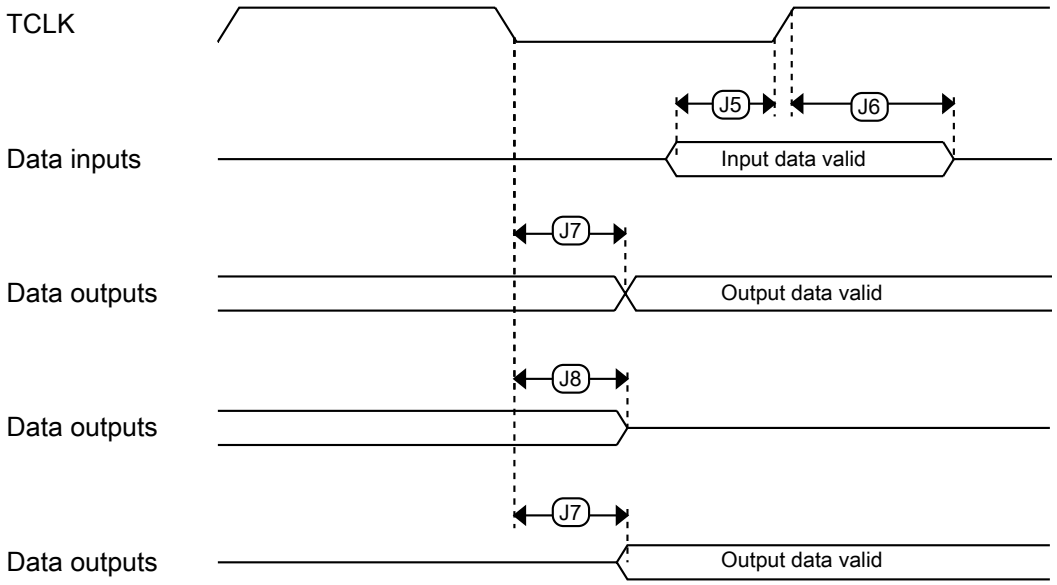

Figure 8. Boundary scan (JTAG) timing

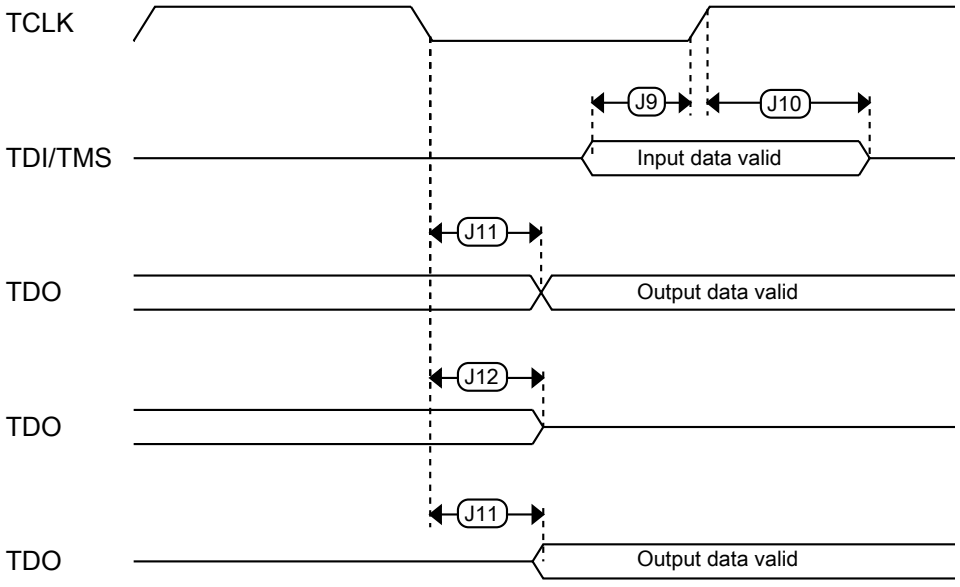

Figure 9. Test Access Port timing

Table 25. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2
Data Flash						
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycd}$	Cycling endurance	10 K	50 K	—	cycles	2
FlexRAM as EEPROM						
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	50	—	years	
$t_{nvmretee10}$	Data retention up to 10% of write endurance	20	100	—	years	
$n_{nvmcycee}$	Cycling endurance for EEPROM backup	20 K	50 K	—	cycles	2
	Write endurance					3
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	140 K	400 K	—	writes	
$n_{nvmwree128}$	• EEPROM backup to FlexRAM ratio = 128	1.26 M	3.2 M	—	writes	
$n_{nvmwree512}$	• EEPROM backup to FlexRAM ratio = 512	5 M	12.8 M	—	writes	
$n_{nvmwree2k}$	• EEPROM backup to FlexRAM ratio = 2,048	20 M	50 M	—	writes	
$n_{nvmwree8k}$	• EEPROM backup to FlexRAM ratio = 8,192	80 M	200 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 125°C.
3. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM and the allocated EEPROM backup per subsystem. Minimum and typical values assume all 16-bit or 32-bit writes to FlexRAM; all 8-bit writes result in 50% less endurance.

3.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the FTFE to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

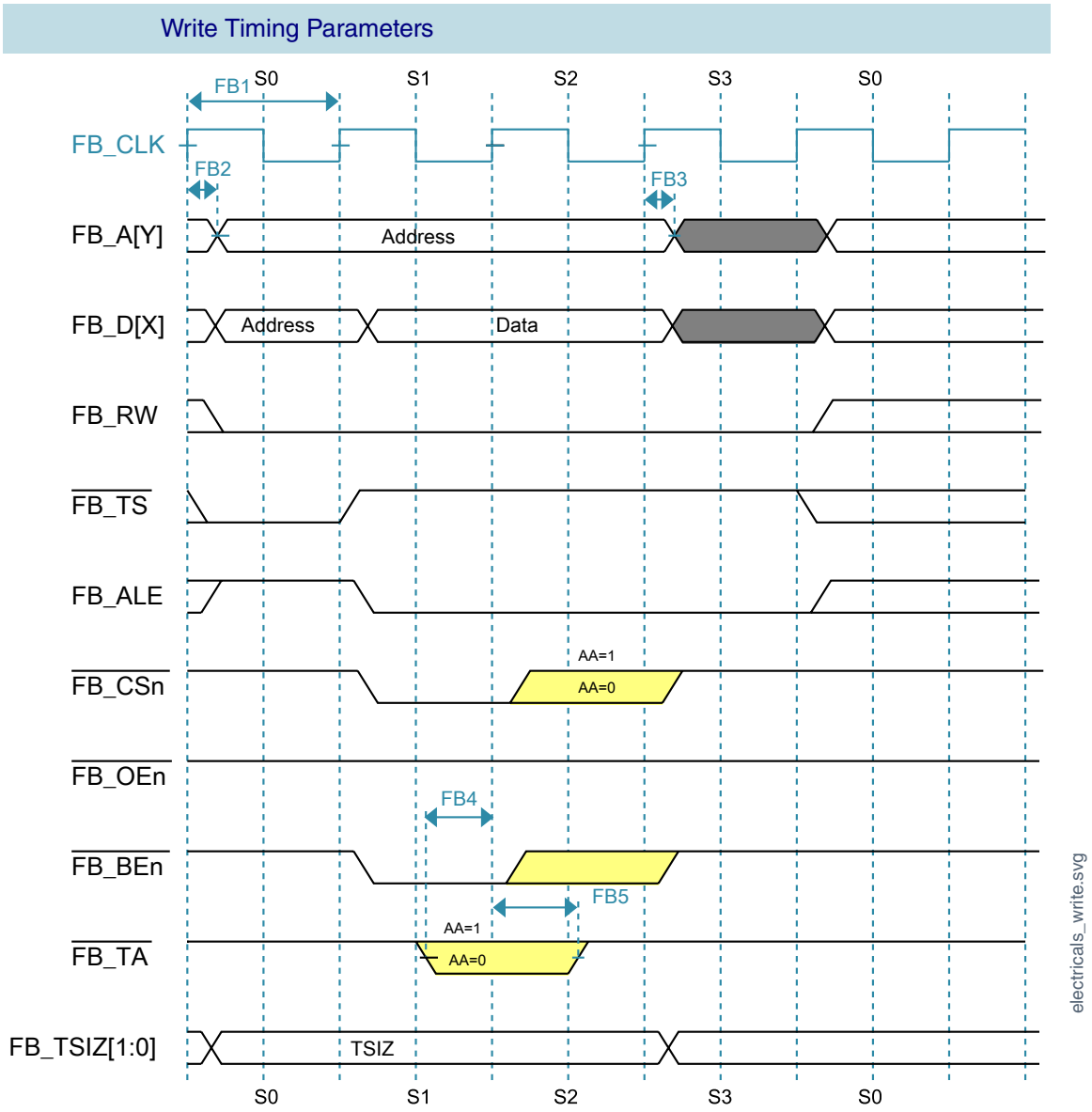

Figure 14. FlexBus write timing diagram

3.4.4 SDRAM controller specifications

Following figure shows SDRAM read cycle.

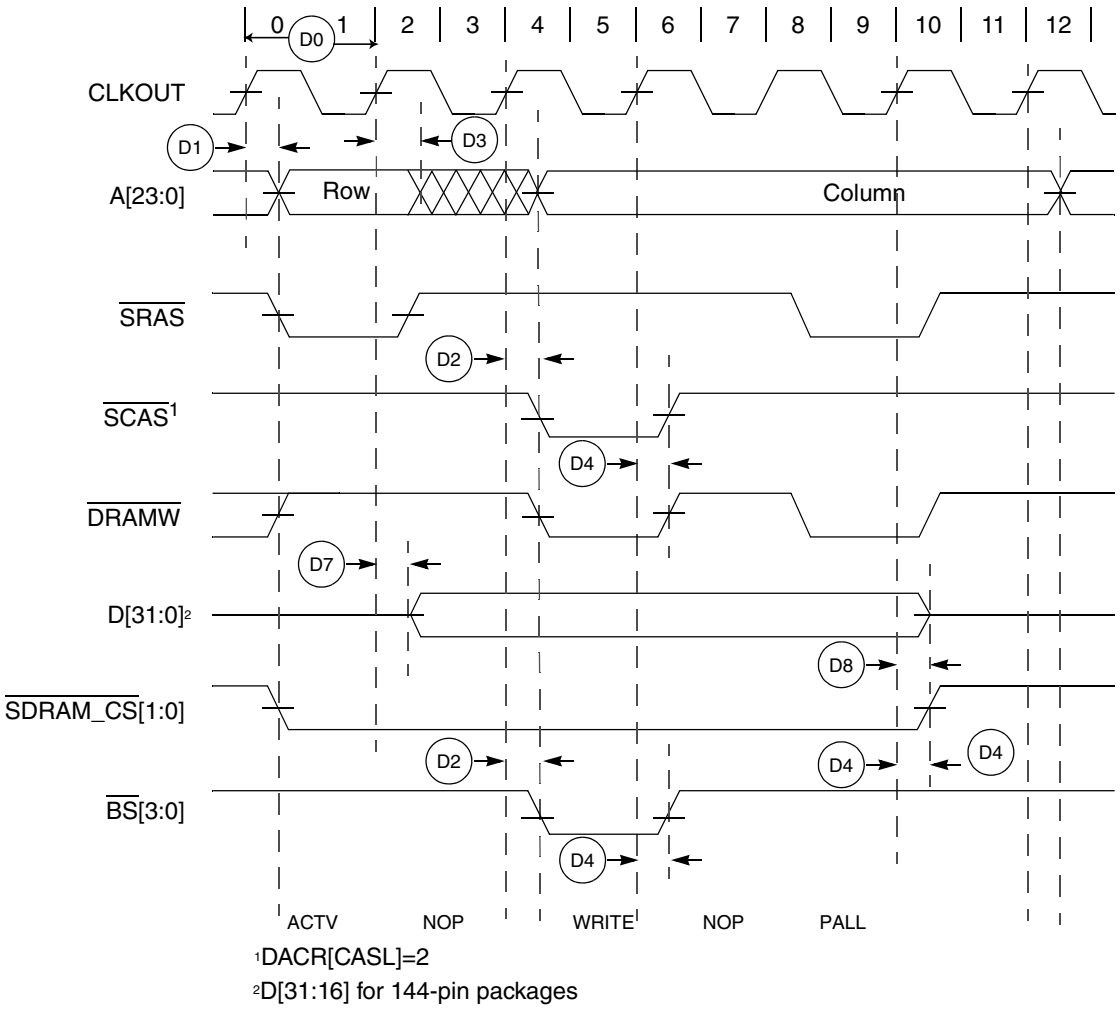

Figure 16. SDRAM write timing diagram

3.5 Analog

3.5.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 31 and Table 32 are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

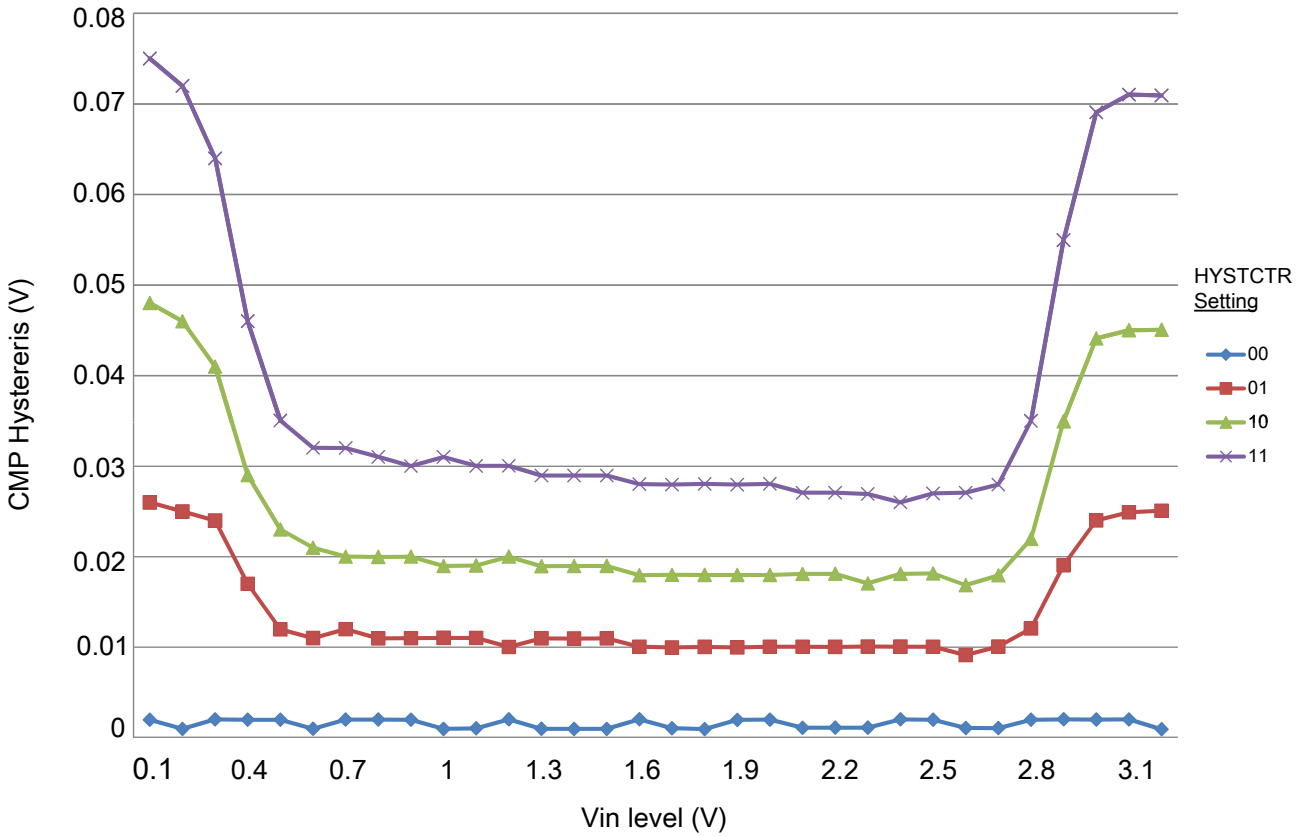

Figure 20. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
144-pin LQFP	98ASS23177W
144-pin MAPBGA	98ASA00222D
169-pin MAPBGA	98ASA00628D
169-pin WLCSP	98ASA00640D

5 Pinout

5.1 MK26 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

The pin functions SDRAM_D12, SDRAM_D13, SDRAM_D14, and SDRAM_D15 don't exist on 144 LQFP and 144 MAPBGA packages.

169 CSP	169 BGA	144 LQFP	144 BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
C11	A1	1	D3	PTE0	ADC1_ SE4a	ADC1_ SE4a	PTE0	SPI1_PCS1	UART1_TX	SDHC0_D1	TRACE_ CLKOUT	I2C1_SDA	RTC_ CLKOUT	
A13	B1	2	D2	PTE1/ LLWU_P0	ADC1_ SE5a	ADC1_ SE5a	PTE1/ LLWU_P0	SPI1_ SOUT	UART1_RX	SDHC0_D0	TRACE_D3	I2C1_SCL	SPI1_SIN	
B12	—	—	—	PTE2/ LLWU_P1	ADC1_ SE6a	ADC1_ SE6a	PTE2/ LLWU_P1	SPI1_SCK	UART1_ CTS_b	SDHC0_ DCLK	TRACE_D2			
B13	—	—	—	PTE3	ADC1_ SE7a	ADC1_ SE7a	PTE3	SPI1_SIN	UART1_ RTS_b	SDHC0_ CMD	TRACE_D1		SPI1_ SOUT	
—	C1	3	D1	PTE2/ LLWU_P1	ADC1_ SE6a	ADC1_ SE6a	PTE2/ LLWU_P1	SPI1_SCK	UART1_ CTS_b	SDHC0_ DCLK	TRACE_D2			
—	D1	4	E4	PTE3	ADC1_ SE7a	ADC1_ SE7a	PTE3	SPI1_SIN	UART1_ RTS_b	SDHC0_ CMD	TRACE_D1		SPI1_ SOUT	
F9	G5	5	E5	VDD	VDD	VDD								
—	C3	6	H3	VSS	VSS	VSS								
C12	E1	7	E3	PTE4/ LLWU_P2	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	UART3_TX	SDHC0_D3	TRACE_D0			
D11	D2	8	E2	PTE5	DISABLED		PTE5	SPI1_PCS2	UART3_RX	SDHC0_D2		FTM3_CH0		

169 CSP	169 BGA	144 LQFP	144 BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
K8	G7	43	—	VDD	VDD	VDD								
H7	N7	44	—	VSS	VSS	VSS								
N8	L7	45	M4	PTE24	ADC0_ SE17	ADC0_ SE17	PTE24	CAN1_TX	UART4_TX		I2C0_SCL	EWM_ OUT_b		
M8	K7	46	K5	PTE25/ LLWU_P21	ADC0_ SE18	ADC0_ SE18	PTE25/ LLWU_P21	CAN1_RX	UART4_RX		I2C0_SDA	EWM_IN		
L8	K8	47	K4	PTE26/ CLKOUT32 K	DISABLED		PTE26/ CLKOUT32 K		UART4_ CTS_b			RTC_ CLKOUT	USB0_ CLKIN	
J7	L8	48	J4	PTE27	DISABLED		PTE27		UART4_ RTS_b					
K7	M7	49	H4	PTE28	DISABLED		PTE28							
N7	N8	50	J5	PTA0	JTAG_ TCLK/ SWD_CLK/ EZP_CLK	TSI0_CH1	PTA0	UART0_ CTS_b/ UART0_ COL_b	FTM0_CH5		LPUART0_ CTS_b		JTAG_ TCLK/ SWD_CLK	EZP_CLK
M7	N9	51	J6	PTA1	JTAG_TDI/ EZP_DI	TSI0_CH2	PTA1	UART0_RX	FTM0_CH6	I2C3_SDA	LPUART0_ RX		JTAG_TDI	EZP_DI
L7	M9	52	K6	PTA2	JTAG_ TDO/ TRACE_ SWO/ EZP_DO	TSI0_CH3	PTA2	UART0_TX	FTM0_CH7	I2C3_SCL	LPUART0_ TX		JTAG_ TDO/ TRACE_ SWO	EZP_DO
J6	M8	53	K7	PTA3	JTAG_ TMS/ SWD_DIO	TSI0_CH4	PTA3	UART0_ RTS_b	FTM0_CH0		LPUART0_ RTS_b		JTAG_ TMS/ SWD_DIO	
K6	L9	54	L7	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
N6	N10	55	M8	PTA5	DISABLED		PTA5	USB0_ CLKIN	FTM0_CH2		CMP2_OUT	I2S0_TX_ BCLK	JTAG_ TRST_b	
M6	H5	56	E7	VDD	VDD	VDD								
H6	H8	57	G7	VSS	VSS	VSS								
N5	M10	58	J7	PTA6	DISABLED		PTA6		FTM0_CH3		CLKOUT		TRACE_ CLKOUT	
L6	L10	59	J8	PTA7	ADC0_ SE10	ADC0_ SE10	PTA7		FTM0_CH4				TRACE_D3	
M5	K9	60	K8	PTA8	ADC0_ SE11	ADC0_ SE11	PTA8		FTM1_CH0			FTM1_QD_ PHA/ TPM1_CH0	TRACE_D2	
J5	K10	61	L8	PTA9	DISABLED		PTA9		FTM1_CH1			FTM1_QD_ PHB/ TPM1_CH1	TRACE_D1	
K5	N11	62	M9	PTA10/ LLWU_P22	DISABLED		PTA10/ LLWU_P22		FTM2_CH0			FTM2_QD_ PHA/ TPM2_CH0	TRACE_D0	

169 CSP	169 BGA	144 LQFP	144 BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
—	—	94	F5	VDD	VDD	VDD								
E1	F8	95	E10	PTB16	TSI0_CH9	TSI0_CH9	PTB16	SPI1_ SOUT	UART0_RX	FTM_ CLKIN0	FB_AD17/ SDRAM_ D17	EWM_IN	TPM_ CLKIN0	
E2	D13	96	E9	PTB17	TSI0_CH10	TSI0_CH10	PTB17	SPI1_SIN	UART0_TX	FTM_ CLKIN1	FB_AD16/ SDRAM_ D16	EWM_ OUT_b	TPM_ CLKIN1	
E3	D12	97	D12	PTB18	TSI0_CH11	TSI0_CH11	PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_ BCLK	FB_AD15/ SDRAM_ A23	FTM2_QD_ PHA/ TPM2_CH0		
E4	D11	98	D11	PTB19	TSI0_CH12	TSI0_CH12	PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_ FS	FB_OE_b	FTM2_QD_ PHB/ TPM2_CH1		
E5	D10	99	D10	PTB20	DISABLED		PTB20	SPI2_PCS0			FB_AD31/ SDRAM_ D31	CMP0_OUT		
D1	D9	100	D9	PTB21	DISABLED		PTB21	SPI2_SCK			FB_AD30/ SDRAM_ D30	CMP1_OUT		
D2	C13	101	C12	PTB22	DISABLED		PTB22	SPI2_ SOUT			FB_AD29/ SDRAM_ D29	CMP2_OUT		
D3	C12	102	C11	PTB23	DISABLED		PTB23	SPI2_SIN	SPI0_PCS5		FB_AD28/ SDRAM_ D28	CMP3_OUT		
C1	B13	103	B12	PTC0	ADC0_ SE14/ TSI0_CH13	ADC0_ SE14/ TSI0_CH13	PTC0	SPI0_PCS4	PDB0_ EXTRG	USB0_ SOF_OUT	FB_AD14/ SDRAM_ A22	I2S0_TXD1		
C2	B12	104	B11	PTC1/ LLWU_P6	ADC0_ SE15/ TSI0_CH14	ADC0_ SE15/ TSI0_CH14	PTC1/ LLWU_P6	SPI0_PCS3	UART1_ RTS_b	FTM0_CH0	FB_AD13/ SDRAM_ A21	I2S0_TXD0		
D4	A13	105	A12	PTC2	ADC0_ SE4b/ CMP1_IN0/ TSI0_CH15	ADC0_ SE4b/ CMP1_IN0/ TSI0_CH15	PTC2	SPI0_PCS2	UART1_ CTS_b	FTM0_CH1	FB_AD12/ SDRAM_ A20	I2S0_TX_ FS		
B1	A12	106	A11	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_ BCLK		
F6	C11	107	H8	VSS	VSS	VSS								
E6	H6	108	—	VDD	VDD	VDD								
A1	B11	109	A9	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11/ SDRAM_ A19	CMP1_OUT		
B2	A11	110	D8	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	I2S0_RXD0	FB_AD10/ SDRAM_ A18	CMP0_OUT	FTM0_CH2	
C3	A10	111	C8	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_ SOUT	PDB0_ EXTRG	I2S0_RX_ BCLK	FB_AD9/ SDRAM_ A17	I2S0_MCLK		

169 CSP	169 BGA	144 LQFP	144 BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
B6	C7	126	B5	PTC19	DISABLED		PTC19		UART3_ CTS_b		FB_CS3_b/ FB_BE7_0_ BLS31_24_ b/ SDRAM_ DQM0	FB_TA_b		
A6	B7	—	—	PTC24	DISABLED		PTC24		LPUART0_ TX		FB_A5/ SDRAM_D5			
D7	A7	—	—	PTC25	DISABLED		PTC25		LPUART0_ RX		FB_A4/ SDRAM_D4			
E8	E6	—	—	PTC26	DISABLED		PTC26		LPUART0_ CTS_b		FB_A3/ SDRAM_D3			
A7	D6	—	—	PTC27	DISABLED		PTC27		LPUART0_ RTS_b		FB_A2/ SDRAM_D2			
B7	C6	—	—	PTC28	DISABLED		PTC28	I2C3_SDA			FB_A1/ SDRAM_D1			
C7	B6	—	—	PTC29	DISABLED		PTC29	I2C3_SCL			FB_A0/ SDRAM_D0			
D8	A6	127	A5	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART2_ RTS_b	FTM3_CH0	FB_ALE/ FB_CS1_b/ FB_TS_b			
A8	A5	128	D4	PTD1	ADC0_ SE5b	ADC0_ SE5b	PTD1	SPI0_SCK	UART2_ CTS_b	FTM3_CH1	FB_CS0_b			
B8	A4	129	C4	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_ SOUT	UART2_RX	FTM3_CH2	FB_AD4/ SDRAM_ A12		I2C0_SCL	
C8	B4	130	B4	PTD3	DISABLED		PTD3	SPI0_SIN	UART2_TX	FTM3_CH3	FB_AD3/ SDRAM_ A11		I2C0_SDA	
F8	B5	131	A4	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_ RTS_b	FTM0_CH4	FB_AD2/ SDRAM_ A10	EWM_IN	SPI1_PCS0	
A9	C4	132	A3	PTD5	ADC0_ SE6b	ADC0_ SE6b	PTD5	SPI0_PCS2	UART0_ CTS_b/ UART0_ COL_b	FTM0_CH5	FB_AD1/ SDRAM_A9	EWM_ OUT_b	SPI1_SCK	
B9	C5	133	A2	PTD6/ LLWU_P15	ADC0_ SE7b	ADC0_ SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FTM0_ FLT0	SPI1_ SOUT	
—	J8	134	M10	VSS	VSS	VSS								
E9	H7	135	F8	VDD	VDD	VDD								
A10	E5	136	A1	PTD7	DISABLED		PTD7	CMT_IRO	UART0_TX	FTM0_CH7	SDRAM_ CKE	FTM0_ FLT1	SPI1_SIN	
C9	D5	137	C9	PTD8/ LLWU_P24	DISABLED		PTD8/ LLWU_P24	I2C0_SCL			LPUART0_ RX	FB_A16		
B10	D4	138	B9	PTD9	DISABLED		PTD9	I2C0_SDA			LPUART0_ TX	FB_A17		
A11	D3	139	B3	PTD10	DISABLED		PTD10				LPUART0_ RTS_b	FB_A18		

169 CSP	169 BGA	144 LQFP	144 BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EZPORT
D9	C2	140	B2	PTD11/ LLWU_P25	DISABLED		PTD11/ LLWU_P25	SPI2_PCS0		SDHC0_ CLKIN	LPUART0_ CTS_b	FB_A19		
C10	B2	141	B1	PTD12	DISABLED		PTD12	SPI2_SCK	FTM3_ FLT0	SDHC0_D4		FB_A20		
A12	B3	142	C3	PTD13	DISABLED		PTD13	SPI2_ SOUT		SDHC0_D5		FB_A21		
B11	A2	143	C2	PTD14	DISABLED		PTD14	SPI2_SIN		SDHC0_D6		FB_A22		
D10	A3	144	C1	PTD15	DISABLED		PTD15	SPI2_PCS1		SDHC0_D7		FB_A23		
—	K2	—	—	NC	NC	NC								
—	J7	—	M5	NC	NC	NC								
—	—	—	A10	NC	NC	NC								
—	—	—	B10	NC	NC	NC								
—	—	—	C10	NC	NC	NC								

5.2 Recommended connection for unused analog and digital pins

Table 57 shows the recommended connections for analog interface pins if those analog interfaces are not used in the customer's application

Table 57. Recommended connection for unused analog interfaces

Pin Type	K26	Short recommendation	Detailed recommendation
Analog/non GPIO	ADCx/CMPx	Float	Analog input - Float
Analog/non GPIO	VREF_OUT	Float	Analog output - Float
Analog/non GPIO	DAC0_OUT, DAC1_OUT	Float	Analog output - Float
Analog/non GPIO	RTC_WAKEUP_B	Float	Analog output - Float
Analog/non GPIO	XTAL32	Float	Analog output - Float
Analog/non GPIO	EXTAL32	Float	Analog input - Float
GPIO/Analog	PTA18/EXTAL0	Float	Analog input - Float
GPIO/Analog	PTA19/XTAL0	Float	Analog output - Float
GPIO/Analog	PTx/ADCx	Float	Float (default is analog input)
GPIO/Analog	PTx/CMPx	Float	Float (default is analog input)
GPIO/Analog	PTx/TSIOx	Float	Float (default is analog input)
GPIO/Digital	PTA0/JTAG_TCLK	Float	Float (default is JTAG with pulldown)
GPIO/Digital	PTA1/JTAG_TDI	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA2/JTAG_TDO	Float	Float (default is JTAG with pullup)

Table continues on the next page...

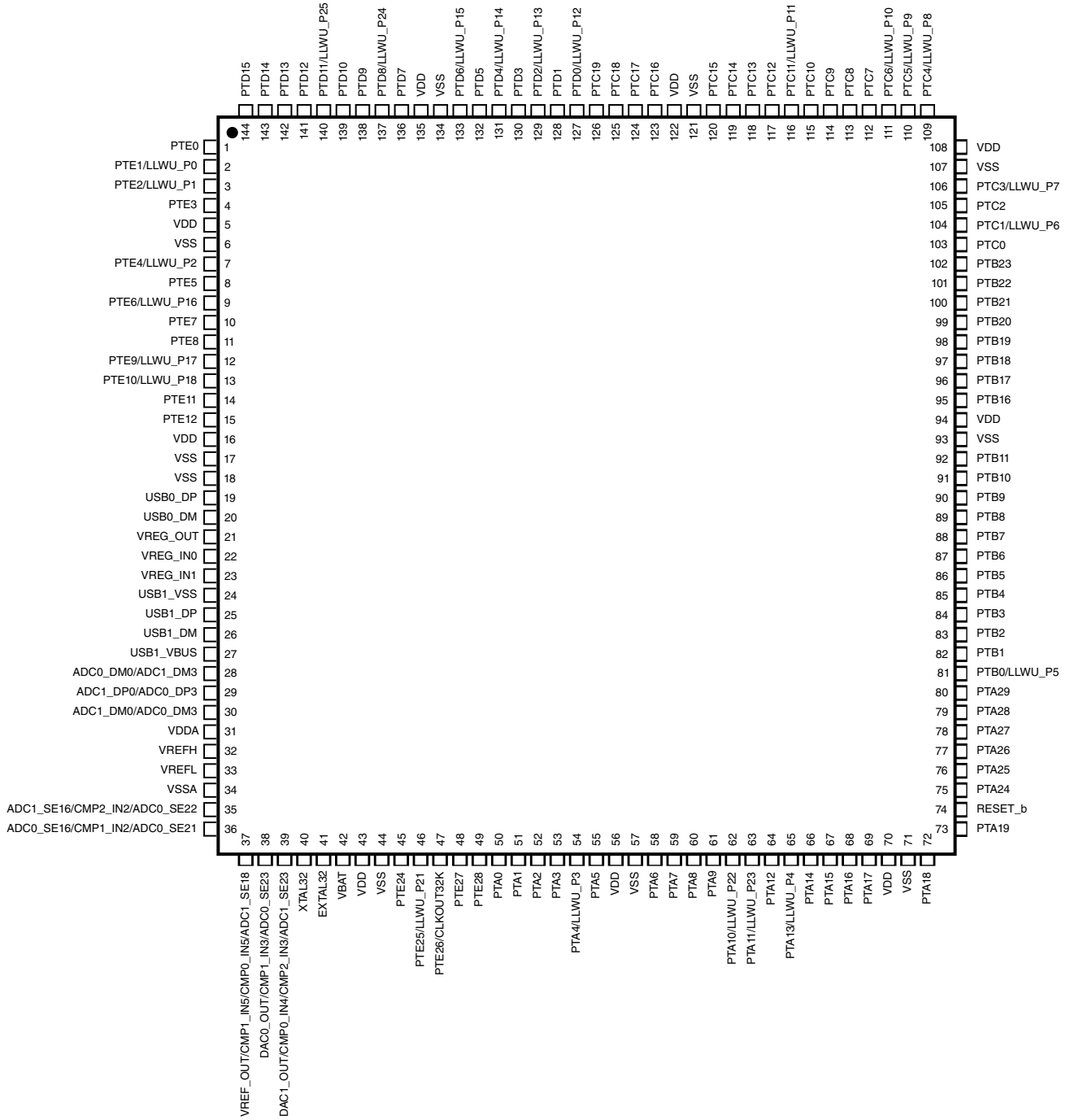

Figure 36. MK26 144 LQFP Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	
A	PTD7	PTD6/ LLWU_P15	PTD5	PTD4/ LLWU_P14	PTD0/ LLWU_P12	PTC16	PTC12	PTC8	PTC4/ LLWU_P8	NC	PTC3/ LLWU_P7	PTC2	A
B	PTD12	PTD11/ LLWU_P25	PTD10	PTD3	PTC19	PTC15	PTC11/ LLWU_P11	PTC7	PTD9	NC	PTC1/ LLWU_P6	PTC0	B
C	PTD15	PTD14	PTD13	PTD2/ LLWU_P13	PTC18	PTC14	PTC10	PTC6/ LLWU_P10	PTD8/ LLWU_P24	NC	PTB23	PTB22	C
D	PTE2/ LLWU_P1	PTE1/ LLWU_P0	PTE0	PTD1	PTC17	PTC13	PTC9	PTC5/ LLWU_P9	PTB21	PTB20	PTB19	PTB18	D
E	PTE6/ LLWU_P16	PTE5	PTE4/ LLWU_P2	PTE3	VDD	VDD	VDD	VDD	PTB17	PTB16	PTB11	PTB10	E
F	PTE10/ LLWU_P18	PTE9/ LLWU_P17	PTE8	PTE7	VDD	VSS	VSS	VDD	PTB9	PTB8	PTB7	PTB6	F
G	VREG_OUT	VREG_IN0	PTE12	PTE11	VREFH	VREFL	VSS	VSS	PTB5	PTB4	PTB3	PTB2	G
H	USB0_DP	USB0_DM	VSS	PTE28	VDDA	VSSA	VSS	VSS	PTB1	PTB0/ LLWU_P5	PTA29	PTA28	H
J	USB1_DP	VREG_IN1	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	PTE27	PTA0	PTA1	PTA6	PTA7	PTA13/ LLWU_P4	PTA27	PTA26	PTA25	J
K	USB1_DM	USB1_VSS	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	PTE26/ CLKOUT32K	PTE25/ LLWU_P21	PTA2	PTA3	PTA8	PTA12	PTA16	PTA17	PTA24	K
L	USB1_VBUS	ADC0_DM0/ ADC1_DM3	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	RTC_ WAKEUP_B	VBAT	PTA4/ LLWU_P3	PTA9	PTA11/ LLWU_P23	PTA14	PTA15	RESET_b	L
M	ADC1_DP0/ ADC0_DP3	ADC1_DM0/ ADC0_DM3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	PTE24	NC	EXTAL32	XTAL32	PTA5	PTA10/ LLWU_P22	VSS	PTA19	PTA18	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 37. MK26 144 BGA Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	PTE0	PTD14	PTD15	PTD2/ LLWU_P13	PTD1	PTD0/ LLWU_P12	PTC25	PTC10	PTC11/ LLWU_P11	PTC6/ LLWU_P10	PTC5/ LLWU_P9	PTC3/ LLWU_P7	PTC2	A
B	PTE1/ LLWU_P0	PTD12	PTD13	PTD3	PTD4/ LLWU_P14	PTC29	PTC24	PTC13	PTC12	PTC7	PTC4/ LLWU_P8	PTC1/ LLWU_P6	PTC0	B
C	PTE2/ LLWU_P1	PTD11/ LLWU_P25	VSS	PTD5	PTD6/ LLWU_P15	PTC28	PTC19	PTC14	PTC9	PTC8	VSS	PTB23	PTB22	C
D	PTE3	PTE5	PTD10	PTD9	PTD8/ LLWU_P24	PTC27	PTC18	PTC15	PTB21	PTB20	PTB19	PTB18	PTB17	D
E	PTE4/ LLWU_P2	PTE6/ LLWU_P16	PTE7	PTE8	PTD7	PTC26	PTC17	PTC16	PTB15	PTB14	PTB13	PTB12	PTB11	E
F	USB0_DM	VREG_IN0	PTE9/ LLWU_P17	PTE10/ LLWU_P18	PTE17/ LLWU_P19	PTE18/ LLWU_P20	PTE19	PTB16	PTB9	PTB8	PTB7	PTB6	PTB5	F
G	USB0_DP	VREG_OUT	VSS	PTE11	VDD	VDD	VDD	VSS	PTB10	PTB3	PTB2	PTB1	PTB0/ LLWU_P5	G
H	USB1_DM	VREG_IN1	PTE16	PTE12	VDD	VDD	VDD	VSS	PTB4	PTA30	PTA29	PTA28	PTA27	H
J	USB1_DP	USB1_VBUS	VDDA	VSSA	NC	NC	NC	VSS	PTA31	PTA26	PTA25	PTA17	PTA16	J
K	USB1_VSS	NC	VREFH	VREFL	NC	NC	PTE25/ LLWU_P21	PTE26/ CLKOUT32K	PTA8	PTA9	PTA24	PTA15	PTA14	K
L	ADC1_DP1	ADC0_DM0/ ADC1_DM3	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	NC	NC	NC	PTE24	PTE27	PTA4/ LLWU_P3	PTA7	PTA13/ LLWU_P4	PTA12	RESET_b	L
M	ADC1_DM1	ADC0_DP0/ ADC1_DP3	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	RTC_ WAKEUP_B	VBAT	PTE28	PTA3	PTA2	PTA6	PTA11/ LLWU_P23	VSS	PTA19	M
N	ADC1_DP0/ ADC0_DP3	ADC1_DM0/ ADC0_DM3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	XTAL32	EXTAL32	VSS	PTA0	PTA1	PTA5	PTA10/ LLWU_P22	VDD	PTA18	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

Figure 38. MK26 169 BGA Pinout Diagram

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to nxp.com and perform a part number search for the following device numbers: MK26

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
K##	Kinetis family	• K26
A	Key attribute	• D = Cortex-M4 w/ DSP • F = Cortex-M4 w/ DSP and FPU
M	Flash memory type	• N = Program flash only • X = Program flash and FlexMemory
FFF	Program flash memory size	• 32 = 32 KB • 64 = 64 KB • 128 = 128 KB • 256 = 256 KB • 512 = 512 KB • 1M0 = 1 MB • 2M0 = 2 MB

Table continues on the next page...

Field	Description	Values
R	Silicon revision	• Z = Initial • (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105 • C = –40 to 85
PP	Package identifier	• FM = 32 QFN (5 mm x 5 mm) • FT = 48 QFN (7 mm x 7 mm) • LF = 48 LQFP (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm) • MP = 64 MAPBGA (5 mm x 5 mm) • LK = 80 LQFP (12 mm x 12 mm) • LL = 100 LQFP (14 mm x 14 mm) • MC = 121 MAPBGA (8 mm x 8 mm) • LQ = 144 LQFP (20 mm x 20 mm) • MD = 144 MAPBGA (13 mm x 13 mm)
CC	Maximum CPU frequency (MHz)	• 5 = 50 MHz • 7 = 72 MHz • 10 = 100 MHz • 12 = 120 MHz • 15 = 150 MHz • 16 = 168 MHz • 18 = 180 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

7.4 Example

This is an example part number:

MK26FN2M0CAC18R

8 Terminology and guidelines

8.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered.

Table continues on the next page...