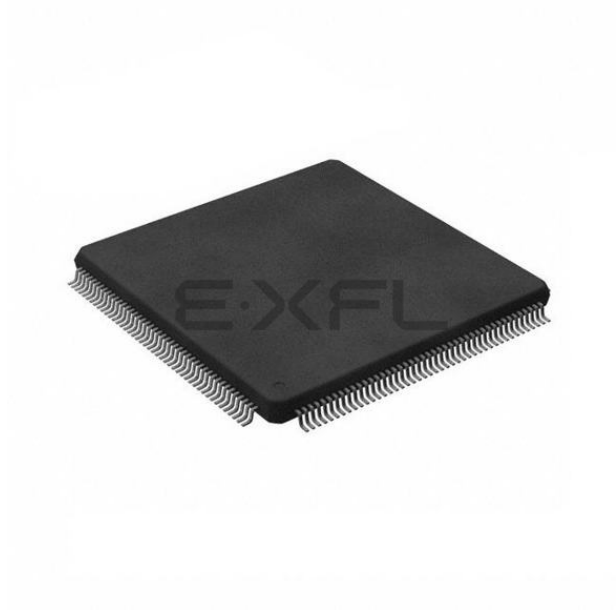
Infineon Technologies - MB91F467SAPMC-GSK5E2 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR60 RISC
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	133
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	72K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f467sapmc-gsk5e2

1. Product Lineup

Feature	MB91V460B	MB91F467SA
Max. core frequency (CLKB)	80MHz	100MHz
Max. resource frequency (CLKP)	40MHz	50MHz
Max. external bus freq. (CLKT)	40MHz	50MHz
Max. CAN frequency (CLKCAN)	20MHz	40MHz
Max. FlexRay frequency (SCLK)	-	-
Technology	0.35µm	0.18µm
Watchdog	yes	yes
Watchdog (RC osc. based)	yes (disengageable)	yes
Bit Search	yes	yes
Reset input (INITX)	yes	yes
Hardware Standby input (HSTX)	yes	no
Clock Modulator	yes	yes
Clock Monitor	yes	yes
Low Power Mode	yes	yes
DMA	5 ch	5 ch
MAC (µDSP)	no	no
MMU/MPU	MPU (16 ch) [1)]	MPU (8 ch) [1)]
Flash	Emulation SRAM 32bit read data	1088 KByte
Satellite Flash	-	no
Flash Protection	-	yes
D-RAM	64 KByte	32 KByte
ID-RAM	64 KByte	32 KByte
Flash-Cache (Instruction cache)	16 KByte	8 KByte
Boot-ROM / BI-ROM	4 KByte fixed	4 KByte
RTC	1 ch	1 ch
Free Running Timer	8 ch	8 ch
ICU	8 ch	8 ch
OCU	8 ch	4 ch
Reload Timer	8 ch	8 ch
PPG 16-bit	16 ch	16 ch
PFM 16-bit	1 ch	1 ch
Sound Generator	1 ch	1 ch
Up/Down Counter (8/16-bit)	4 ch (8-bit) / 2 ch (16-bit)	4 ch (8-bit) / 2 ch (16-bit)

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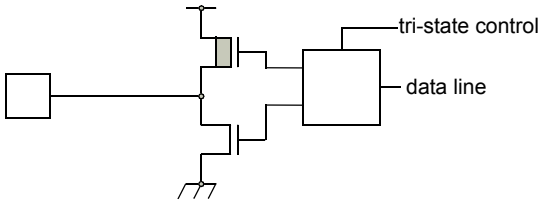
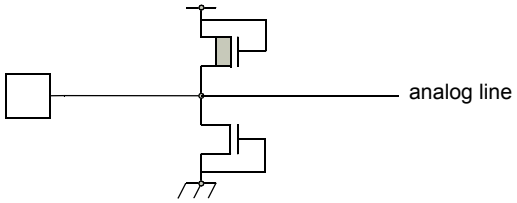
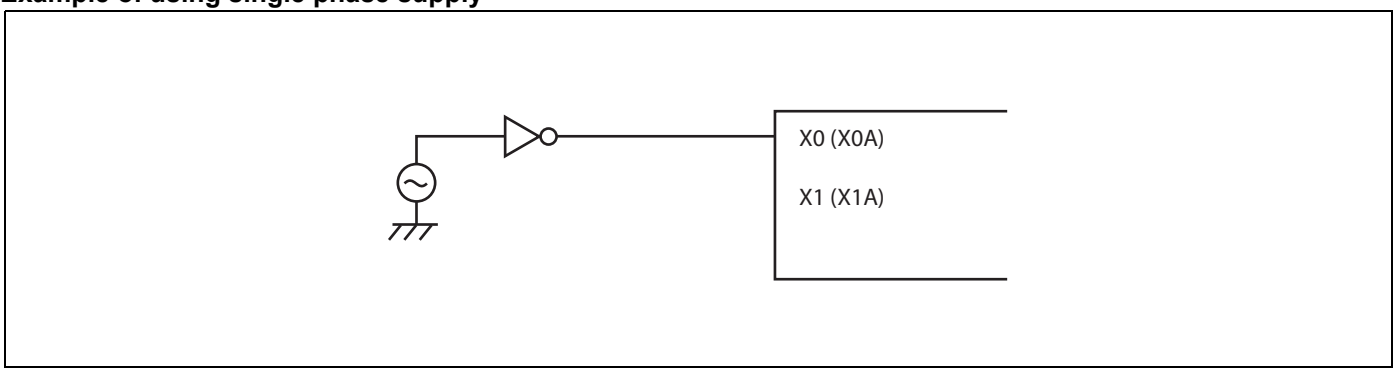
Pin no.	Pin name	I/O	I/O circuit type*	Function
151	P23_6	I/O	A	General-purpose input/output port
	INT11			External interrupt input pin
152	P22_0	I/O	A	General-purpose input/output port
	INT12			External interrupt input pin
153	P22_2	I/O	A	General-purpose input/output port
	INT13			External interrupt input pin
156	P22_4	I/O	C	General-purpose input/output port
	SDA0			I^2C bus data input/output pin
	INT14			External interrupt input pin
157	P22_5	I/O	C	General-purpose input/output port
	SCL0			I^2C bus clock input/output pin
158	P22_6	I/O	C	General-purpose input/output port
	SDA1			I^2C bus data input/output pin
	INT15			External interrupt input pin
159	P22_7	I/O	C	General-purpose input/output port
	SCL1			I^2C bus clock input/output pin
160 to 163	P15_0 to P15_3	I/O	A	General-purpose input/output ports
	OCU0 to OCU3			Output compare output pins
	TOT0 to TOT3			Reload timer output pins
164 to 171	P14_0 to P14_7	I/O	A	General-purpose input/output ports
	ICU0 to ICU7			Input capture input pins
	TIN8/0 to TIN 15/7			External trigger input pins of reload timer
	TTG24/16/8/0 to TTG31/23/15/7			External trigger input pins of PPG timer
172 to 175	P07_0 to P07_3	I/O	A	General-purpose input/output ports
	A0 to A3			Signal pins of external address bus (bit0 to bit3)

Type	Circuit	Remarks
M		CMOS level tri-state output (I_{OL} = 5mA, I_{OH} = -5mA)
N1/N2		Analog terminal Type N1: Analog input pin with protection Type N2: Analog output line with protection

5.5.2 Single phase clock supply

For lower frequencies, up to 4 MHz, it is possible to supply a single phase clock at X0 (X0A).

Example of using single phase supply



5.6 Mode pins (MD_x)

These pins should be connected directly to the power supply or ground pins. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or ground pin on the printed circuit board as possible and connect them with low impedance.

MD_3 pin should be connected directly to ground.

5.7 Notes on operating in PLL clock mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

5.8 Pull-up control

The AC standard is not guaranteed in case a pull-up resistor is connected to the pin serving as an external bus pin.

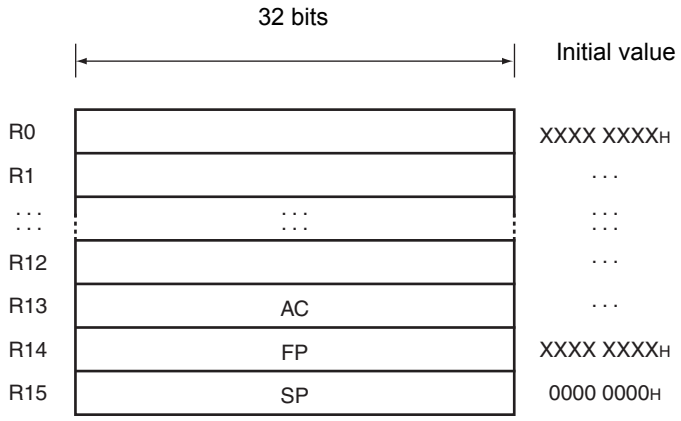
5.9 Notes on PS register

As the PS register is processed in advance by some instructions, when the debugger is being used, the exception handling may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated.
As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, the operation before and after the EIT always proceeds according to specification.

1. The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction: (a) a user interrupt or NMI is accepted; (b) single-step execution is performed; or (c) execution breaks due to a data event or from the emulator menu.
   - D0 and D1 flags are updated in advance.
   - An EIT handling routine (user interrupt/NMI or emulator) is executed.
   - Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1).
2. The following behavior occurs when an ORCCR, STILM, MOV Ri, PS instruction is executed to enable a user interrupt or NMI source while that interrupt is in the active state.
   - The PS register is updated in advance.
   - An EIT handling routine (user interrupt/NMI or emulator) is executed.
   - Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in 1).

8.4 Registers

8.4.1 General-purpose register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13 : Virtual accumulator

R14 : Frame pointer

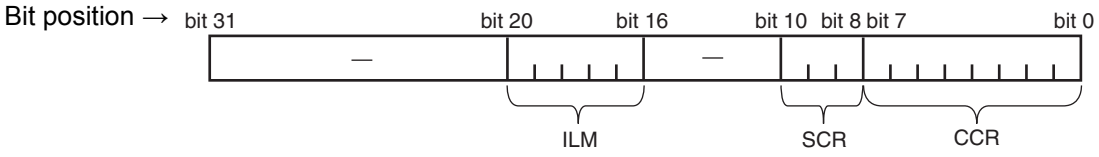
R15 : Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000_H (SSP value).

8.4.2 PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

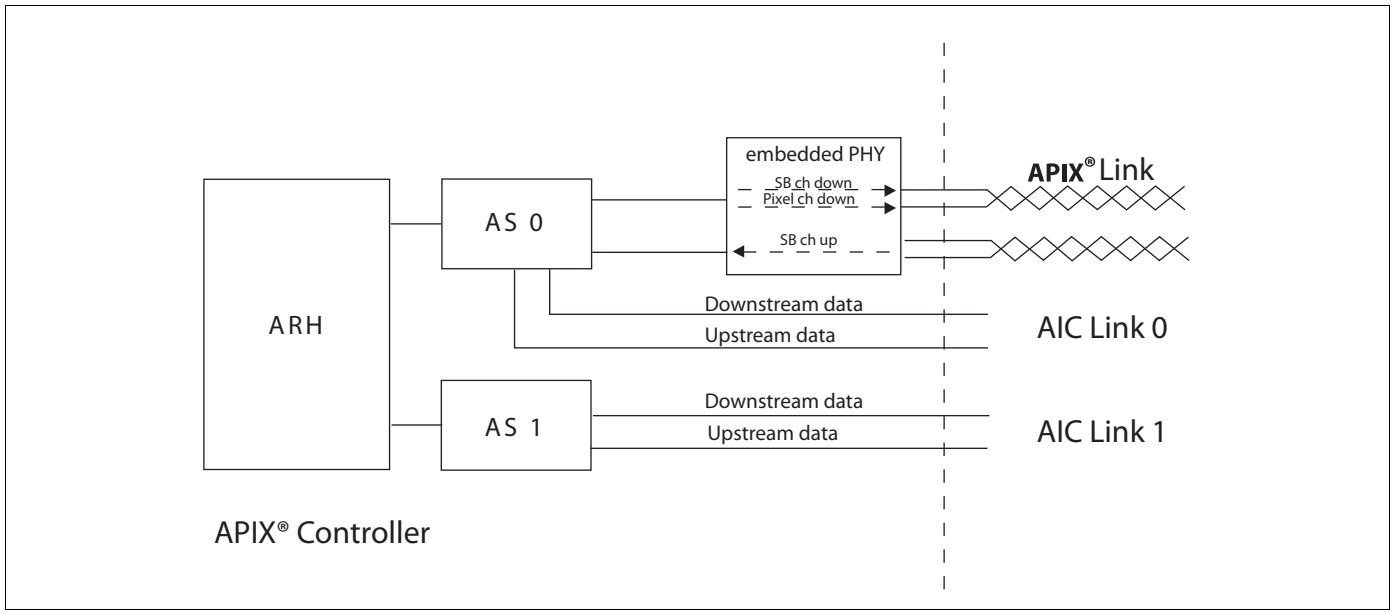
All undefined bits (-) in the diagram are reserved bits. The read values are always “0”. Write access to these bits is invalid.



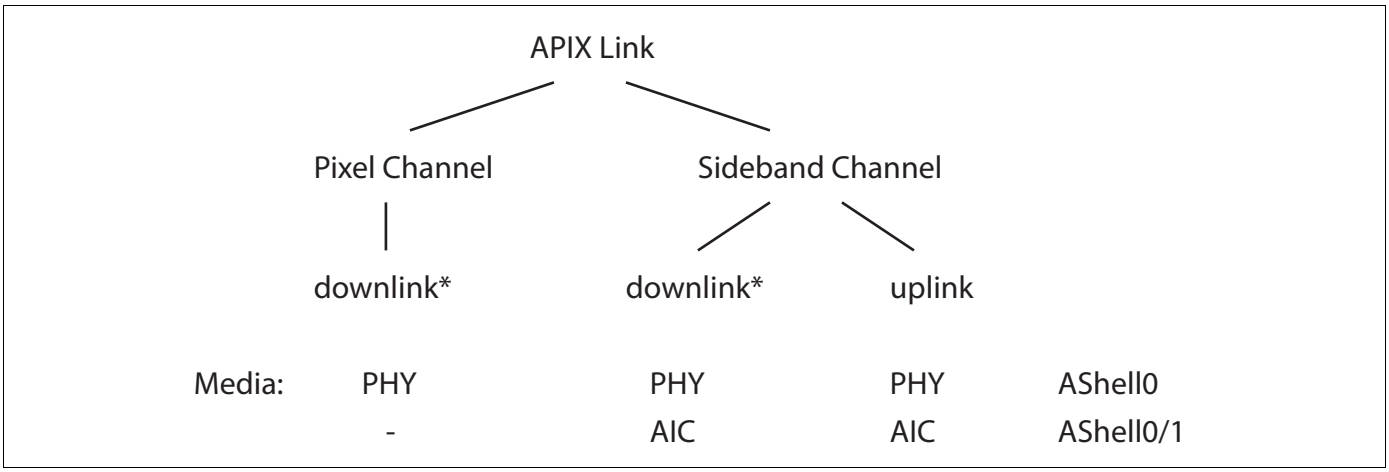
10. APIX® Controller

10.1 Overview

The integrated APIX® controller provides 2 links. Link 0 can be configured as an APIX® link or an Automotive Interconnect (AIC) link. Link 1 only supports AIC link.



*Remark: Link 1 can be used only if Link 0 is activated (CHCTRL: TXCFG = 0)



*Remark: MB91460S series provides either downlink over Pixelchannel or over Sidebandchannel

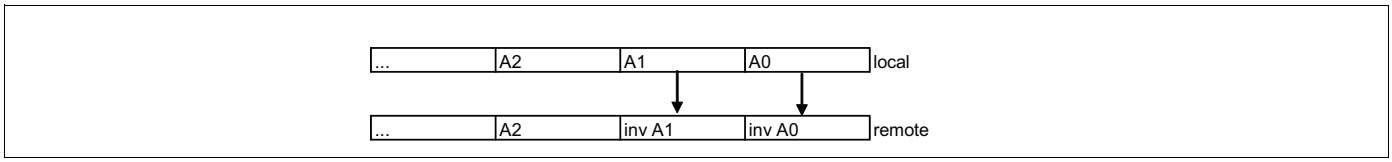
Transaction Frame

- TFCTRL00 (Transaction Buffer 00): Address 07250h
- TFCTRL01 (Transaction Buffer 01): Address 07252h
- TFCTRL02 (Transaction Buffer 02): Address 07254h
- TFCTRL03 (Transaction Buffer 03): Address 07256h
- TFCTRL04 (Transaction Buffer 04): Address 07258h
- TFCTRL05 (Transaction Buffer 05): Address 0725Ah
- TFCTRL06 (Transaction Buffer 06): Address 0725Ch
- TFCTRL07 (Transaction Buffer 07): Address 0725Eh
- TFCTRL08 (Transaction Buffer 08): Address 07260h
- TFCTRL09 (Transaction Buffer 09): Address 07262h
- TFCTRL10 (Transaction Buffer 10): Address 07264h
- TFCTRL11 (Transaction Buffer 11): Address 07266h
- TFCTRL12 (Transaction Buffer 12): Address 07268h
- TFCTRL13 (Transaction Buffer 13): Address 0726Ah
- TFCTRL14 (Transaction Buffer 14): Address 0726Ch
- TFCTRL15 (Transaction Buffer 15): Address 0726Eh

	7	6	5	4	3	2	1	0
TFCTRL00-15	TFDSWP	TFAINV	-	ERROR	SZ[1]	SZ[0]	OAEN	RW
	R/W	R/W	R0	R	R/W	R/W	R/W	R/W

RW	0	Read
	1	Write
OAEN	0	Offset address disabled
	1	Offset address enabled
SZ[1:0]	00	Byte
	01	Halfword
	10	Word
	11	-
ERROR	0	Normal operation
	1	Remote Handler RX bus error occurred
TFAINV	0	Normal mode
	1	Address inversion

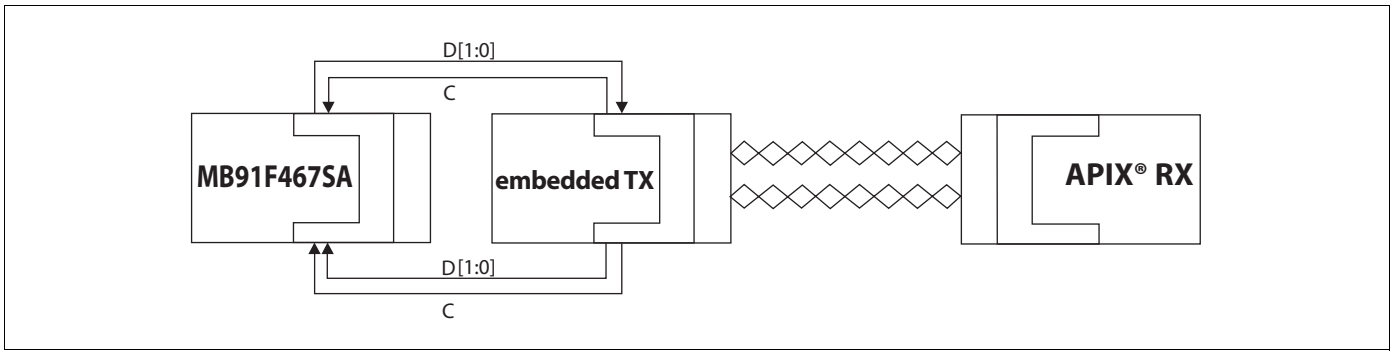
In address inversion mode the two least significant bits of the address are inverted



TFDSWP	0	Normal mode
	1	Byte swapping

In swapping mode depending on the configured size the following byte swapping of the data is performed

2Bit Datawidth



Register	Bit	Default	Value	Description
APCFGn1	31	1	0	0: disable data mode / enable pixel stream mode 1: enable data mode / disable pixel stream mode
APCFGn1	29	1	0	1: enable core clock of APIX® PHY 0: disable
APCFGn3	18	0	1	AShell: connect internal Ashell to external APIX® PHY through GPIO interface 1: enable 0: disable

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000140_H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXX XXXXXXXX		PPG 6
000144_H	PDUT06 [W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 000000 - 0	
000148_H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXX XXXXXXXX		PPG 7
$00014C_H$	PDUT07 [W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 000000 - 0	
000150_H	PTMR08 [R] 11111111 11111111		PCSR08 [W] XXXXXXXX XXXXXXXX		PPG 8
000154_H	PDUT08 [W] XXXXXXXX XXXXXXXX		PCNH08 [R/W] 0000000 -	PCNL08 [R/W] 000000 - 0	
000158_H	PTMR09 [R] 11111111 11111111		PCSR09 [W] XXXXXXXX XXXXXXXX		PPG 9
$00015C_H$	PDUT09 [W] XXXXXXXX XXXXXXXX		PCNH09 [R/W] 0000000 -	PCNL09 [R/W] 000000 - 0	
000160_H	PTMR10 [R] 11111111 11111111		PCSR10 [W] XXXXXXXX XXXXXXXX		PPG 10
000164_H	PDUT10 [W] XXXXXXXX XXXXXXXX		PCNH10 [R/W] 0000000 -	PCNL10 [R/W] 000000 - 0	
000168_H	PTMR11 [R] 11111111 11111111		PCSR11 [W] XXXXXXXX XXXXXXXX		PPG 11
$00016C_H$	PDUT11 [W] XXXXXXXX XXXXXXXX		PCNH11 [R/W] 0000000 -	PCNL11 [R/W] 000000 - 0	
000170_H	P0TMCSRH [R/W] - 0 - 000 - 0	P0TMCSRL [R/W] - - - 00000	P1TMCSRH [R/W] - 0 - 000 - 0	P1TMCSRL [R/W] - - - 00000	Pulse Frequency Modulator
000174_H	P0TMRLR [W] XXXXXXXX XXXXXXXX		P0TMR [R] XXXXXXXX XXXXXXXX		
000178_H	P1TMRLR [W] XXXXXXXX XXXXXXXX		P1TMR [R] XXXXXXXX XXXXXXXX		
$00017C_H$	Reserved				
000180_H	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0 to 3
000184_H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188_H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000640_H	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 1111**00 00100000*4		External Bus
000644_H	ASR1 [R/W] XXXXXXXX XXXXXXXX		ACR1 [R/W] XXXXXXXX XXXXXXXX		
000648_H	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXXXXXX XXXXXXXX		
$00064C_H$	ASR3 [R/W] XXXXXXXX XXXXXXXX		ACR3 [R/W] XXXXXXXX XXXXXXXX		
000650_H	ASR4 [R/W] XXXXXXXX XXXXXXXX		ACR4 [R/W] XXXXXXXX XXXXXXXX		
000654_H	ASR5 [R/W] XXXXXXXX XXXXXXXX		ACR5 [R/W] XXXXXXXX XXXXXXXX		
000658_H	ASR6 [R/W] XXXXXXXX XXXXXXXX		ACR6 [R/W] XXXXXXXX XXXXXXXX		
$00065C_H$	ASR7 [R/W] XXXXXXXX XXXXXXXX		ACR7 [R/W] XXXXXXXX XXXXXXXX		
000660_H	AWR0 [R/W] 01001111 11111011		AWR1 [R/W] XXXXXXXX XXXXXXXX		
000664_H	AWR2 [R/W] XXXXXXXX XXXXXXXX		AWR3 [R/W] XXXXXXXX XXXXXXXX		
000668_H	AWR4 [R/W] XXXXXXXX XXXXXXXX		AWR5 [R/W] XXXXXXXX XXXXXXXX		
$00066C_H$	AWR6 [R/W] XXXXXXXX XXXXXXXX		AWR7 [R/W] XXXXXXXX XXXXXXXX		
000670_H	MCRA [R/W] XXXXXXXX	MCRB [R/W] XXXXXXXX	Reserved		
000674_H	Reserved				
000678_H	IORW0 [R/W] XXXXXXXX	IORW1 [R/W] XXXXXXXX	IORW2 [R/W] XXXXXXXX	Reserved	
$00067C_H$	Reserved				
000680_H	CSER [R/W] 00000001	CHER [R/W] 11111111	Reserved	TCR [R/W] 0000**** *5	
000684_H	RCRH [R/W] 00XXXXXX	RCRL [R/W] XXXX0XXX	Reserved		
000688_H to $0007F8_H$	Reserved				
$0007FC_H$	Reserved	MODR [W] XXXXXXXX	Reserved		Mode Register

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$000D80_H$	PFR00 [R/W] 00000000	PFR01 [R/W] 00000000	Reserved		R-bus Port Function Register
$000D84_H$	Reserved	PFR05 [R/W] 00000000	PFR06 [R/W] 00000000	PFR07 [R/W] 00000000	
$000D88_H$	PFR08 [R/W] 0 - - 0 - - 00	PFR09 [R/W] - - - - 0000	PFR10 [R/W] - - - - 0 - 00	Reserved	
$000D8C_H$	Reserved		PFR14 [R/W] 00000000	PFR15 [R/W] - - - - 0000	
$000D90_H$	PFR16 [R/W] 00000000	PFR17 [R/W] 00000000	PFR18 [R/W] - 000 - 000	PFR19 [R/W] - 000 - 000	
$000D94_H$	PFR20 [R/W] - 000 - 000	Reserved	PFR22 [R/W] 0000 - 0 - 0	PFR23 [R/W] - 0 - 00000	
$000D98_H$	PFR24 [R/W] 00000000	Reserved			
$000D9C_H$	PFR28 [R/W] 00000000	PFR29 [R/W] 00000000	Reserved		
$000DA0_H$ to $000DBC_H$	Reserved				
$000DC0_H$	EPFR00 [R/W] - - - - - - - -	EPFR01 [R/W] - - - - - - - -	Reserved		R-bus Extra Port Function Register
$000DC4_H$	Reserved	EPFR05 [R/W] - - - - - - - -	EPFR06 [R/W] - - - - - - - -	EPFR07 [R/W] - - - - - - - -	
$000DC8_H$	EPFR08 [R/W] - - - - - - - -	EPFR09 [R/W] - - - - - - - -	EPFR10 [R/W] - - - - - - - 0	Reserved	
$000DCC_H$	Reserved		EPFR14 [R/W] 00000000	EPFR15 [R/W] - - - - 0000	
$000DD0_H$	EPFR16 [R/W] 0000 - - - -	EPFR17 [R/W] - 000 - 000	EPFR18 [R/W] - 000 - 000	EPFR19 [R/W] - 0- - - 0- -	
$000DD4_H$	EPFR20 [R/W] - 000 - 000	Reserved	EPFR22 [R/W] - - - - - - - -	EPFR23 [R/W] - - - - - - - -	
$000DD8_H$	EPFR24 [R/W] - - - - - - - -	Reserved			
$000DDC_H$	EPFR28 [R/W] - 000 - 000	EPFR29 [R/W] - - - - - - - -	Reserved		
$000DE0_H$ to $000DFC_H$	Reserved				

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
007278_H	TFADDR02[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
$00727C_H$	TFADDR03[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
007280_H	TFADDR04[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
007284_H	TFADDR05[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
007288_H	TFADDR06[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
$00728C_H$	TFADDR07[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
007290_H	TFADDR08[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
007294_H	TFADDR09[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
007298_H	TFADDR10[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
$00729C_H$	TFADDR11[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
$0072A0_H$	TFADDR12[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
$0072A4_H$	TFADDR13[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
$0072A8_H$	TFADDR14[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
$0072AC_H$	TFADDR15[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
$0072B0_H$	TFDATA00[R/W] 00000000 00000000 00000000 00000000				
$0072B4_H$	TFDATA01[R/W] 00000000 00000000 00000000 00000000				
$0072B8_H$	TFDATA02[R/W] 00000000 00000000 00000000 00000000				
$0072BC_H$	TFDATA03[R/W] 00000000 00000000 00000000 00000000				
$0072C0_H$	TFDATA04[R/W] 00000000 00000000 00000000 00000000				
$0072C4_H$	TFDATA05[R/W] 00000000 00000000 00000000 00000000				
$0072C8_H$	TFDATA06[R/W] 00000000 00000000 00000000 00000000				

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
$00C040_H$	IF2CREQ0 [R/W] 00000000 00000001		IF2CMSK0 [R/W] 00000000 00000000		CAN 0 IF 2 Register
$00C044_H$	IF2MSK20 [R/W] 11111111 11111111		IF2MSK10 [R/W] 11111111 11111111		
$00C048_H$	IF2ARB20 [R/W] 00000000 00000000		IF2ARB10 [R/W] 00000000 00000000		
$00C04C_H$	IF2MCTR0 [R/W] 00000000 00000000		Reserved		
$00C050_H$	IF2DTA10 [R/W] 00000000 00000000		IF2DTA20 [R/W] 00000000 00000000		
$00C054_H$	IF2DTB10 [R/W] 00000000 00000000		IF2DTB20 [R/W] 00000000 00000000		
$00C058_H$, $00C05C_H$	Reserved				
$00C060_H$	IF2DTA20 [R/W] 00000000 00000000		IF2DTA10 [R/W] 00000000 00000000		
$00C064_H$	IF2DTB20 [R/W] 00000000 00000000		IF2DTB10 [R/W] 00000000 00000000		
$00C068_H$ to $00C07C_H$	Reserved				
$00C080_H$	TREQR20 [R] 00000000 00000000		TREQR10 [R] 00000000 00000000		CAN 0 Status Flags
$00C084_H$ to $00C08C_H$	Reserved				
$00C090_H$	NEWDT20 [R] 00000000 00000000		NEWDT10 [R] 00000000 00000000		
$00C094_H$ to $00C09C_H$	Reserved				
$00C0A0_H$	INTPND20 [R] 00000000 00000000		INTPND10 [R] 00000000 00000000		
$00C0A4_H$ to $00C0AC_H$	Reserved				
$00C0B0_H$	MSGVAL20 [R] 00000000 00000000		MSGVAL10 [R] 00000000 00000000		
$00C0B4_H$ to $00C0FC_H$	Reserved				

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Interrupt	Interrupt number		Interrupt level*1		Interrupt vector*2		DMA	
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	RN*5	Stop*6
PPG12	124	7C	ICR54	476_H	$20C_H$	$000FFE0C_H$	108	—
PPG13	125	7D			208_H	$000FFE08_H$	109	—
PPG14	126	7E	ICR55	477_H	204_H	$000FFE04_H$	110	—
PPG15	127	7F			200_H	$000FFE00_H$	111	—
Up/Down Counter 0	128	80	ICR56	478_H	$1FC_H$	$000FFDFC_H$	—	—
Up/Down Counter 1	129	81			$1F8_H$	$000FFDF8_H$	—	—
Up/Down Counter 2	130	82	ICR57	479_H	$1F4_H$	$000FFDF4_H$	—	—
Up/Down Counter 3	131	83			$1F0_H$	$000FFDF0_H$	—	—
Real Time Clock	132	84	ICR58	$47A_H$	$1EC_H$	$000FFDEC_H$	—	—
Calibration Unit	133	85			$1E8_H$	$000FFDE8_H$	—	—
A/D Converter 0	134	86	ICR59	$47B_H$	$1E4_H$	$000FFDE4_H$	14, 112	—
System reserved	135	87			$1E0_H$	$000FFDE0_H$	—	—
Alarm Comparator 0	136	88	ICR60	$47C_H$	$1DC_H$	$000FFDDC_H$	—	—
System reserved	137	89			$1D8_H$	$000FFDD8_H$	—	—
Low Voltage Detection	138	8A	ICR61	$47D_H$	$1D4_H$	$000FFDD4_H$	—	—
SMC Comparator 0 to 5	139	8B			$1D0_H$	$000FFDD0_H$	—	—
Timebase Overflow	140	8C	ICR62	$47E_H$	$1CC_H$	$000FFDCC_H$	—	—
PLL Clock Gear	141	8D			$1C8_H$	$000FFDC8_H$	—	—
DMA Controller	142	8E	ICR63	$47F_H$	$1C4_H$	$000FFDC4_H$	—	—
Main/Sub OSC stability wait	143	8F			$1C0_H$	$000FFDC0_H$	—	—
Security vector	144	90	—	—	$1BC_H$	$000FFDBC_H$	—	—
Used by the INT instruction.	145 to 255	91 to FF	—	—	$1B8_H$ to 000_H	$000FFDB8_H$ to $000FFC00_H$	—	—

*1 : The ICRs are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.

*2 : The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR) . The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value ($000FFC00_H$) . The TBR is initialized to this value by a reset. The TBR is set to $000FFC00_H$ after the internal boot ROM is executed.

*3 : ICR23 and ICR47 can be exchanged by setting the REALOS compatibility bit (addr $0C03_H$: IOS[0])

*4 : Used by REALOS

*5 : DMA RN is the resource number used for DMA operation. No number means that this resource interrupt cannot be used to trigger a DMA transfer.

*6 : DMA Stop shows the DMA Transfer Stop Request feature.

*7 : Memory Protection Unit (MPU) support

15. Recommended Settings

15.1 PLL and Clockgear settings

Please note that for MB91F467SA the core base clock frequencies are valid in both 1.8 V and 1.9 V nominal operation modes of the Main regulator and Flash.

Recommended PLL divider and clockgear settings

PLL Input (CLK) [MHz]	Frequency Parameter		Clockgear Parameter		PLL Output (X) [MHz]	Core Base Clock [MHz]	Remarks
	DIVM	DIVN	DIVG	MULG	MULG		
4	2	25	16	24	200	100	
4	2	24	16	24	192	96	
4	2	23	16	24	184	92	
4	2	22	16	24	176	88	
4	2	21	16	20	168	84	
4	2	20	16	20	160	80	
4	2	19	16	20	152	76	
4	2	18	16	20	144	72	
4	2	17	16	16	136	68	
4	2	16	16	16	128	64	
4	2	15	16	16	120	60	
4	2	14	16	16	112	56	
4	2	13	16	12	104	52	
4	2	12	16	12	96	48	
4	2	11	16	12	88	44	
4	4	10	16	24	160	40	
4	4	9	16	24	144	36	
4	4	8	16	24	128	32	
4	4	7	16	24	112	28	
4	6	6	16	24	144	24	
4	8	5	16	28	160	20	
4	10	4	16	32	160	16	
4	12	3	16	32	144	12	

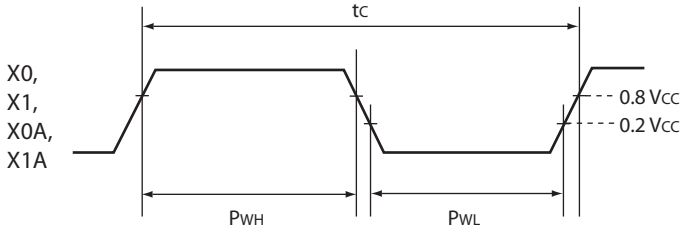
16.7 AC characteristics

16.7.1 Clock timing

($V_{DD}5$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = −40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Condition
			Min	Typ	Max		
Clock frequency	f_C	X0 X1	3.5	4	16	MHz	Opposite phase external supply or crystal
		X0A X1A	32	32.768	100	kHz	

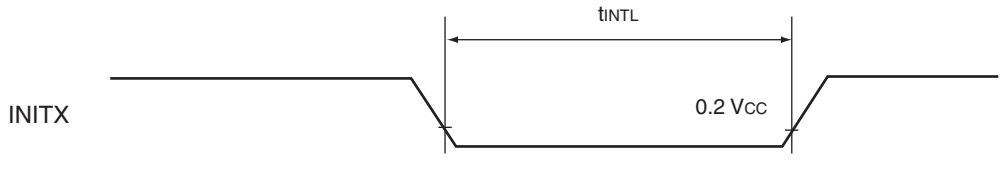
Clock timing condition



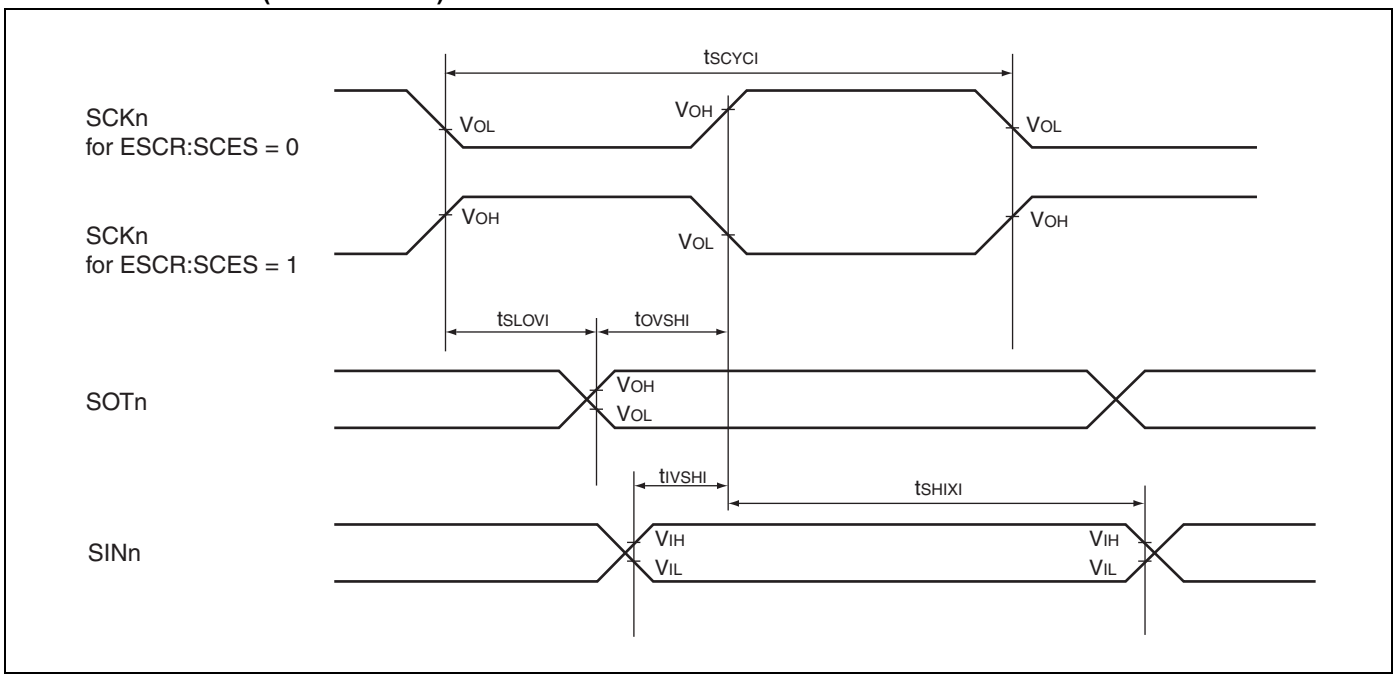
16.7.2 Reset input ratings

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = −40°C to + 105°C)

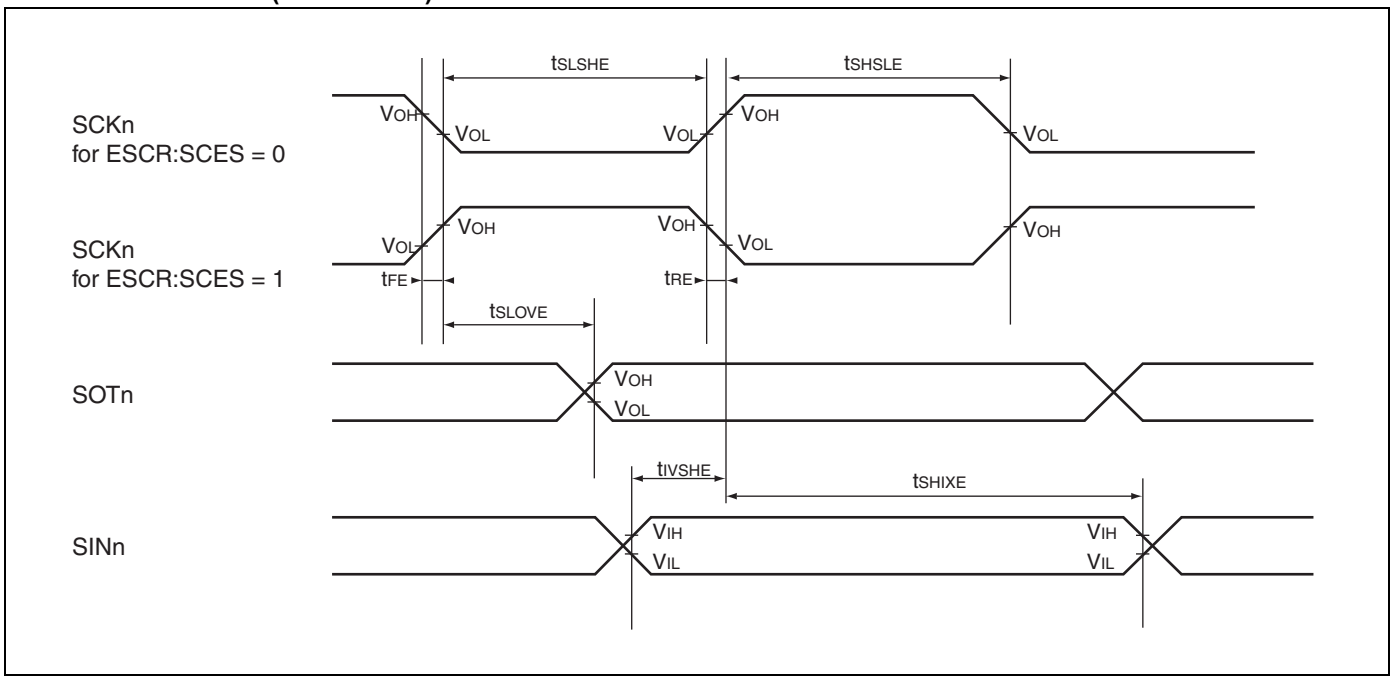
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
INITX input time (at power-on)	t_{INTL}	INITX	—	8	—	ms
INITX input time (other than the above)				20	—	µs



Internal clock mode (master mode)



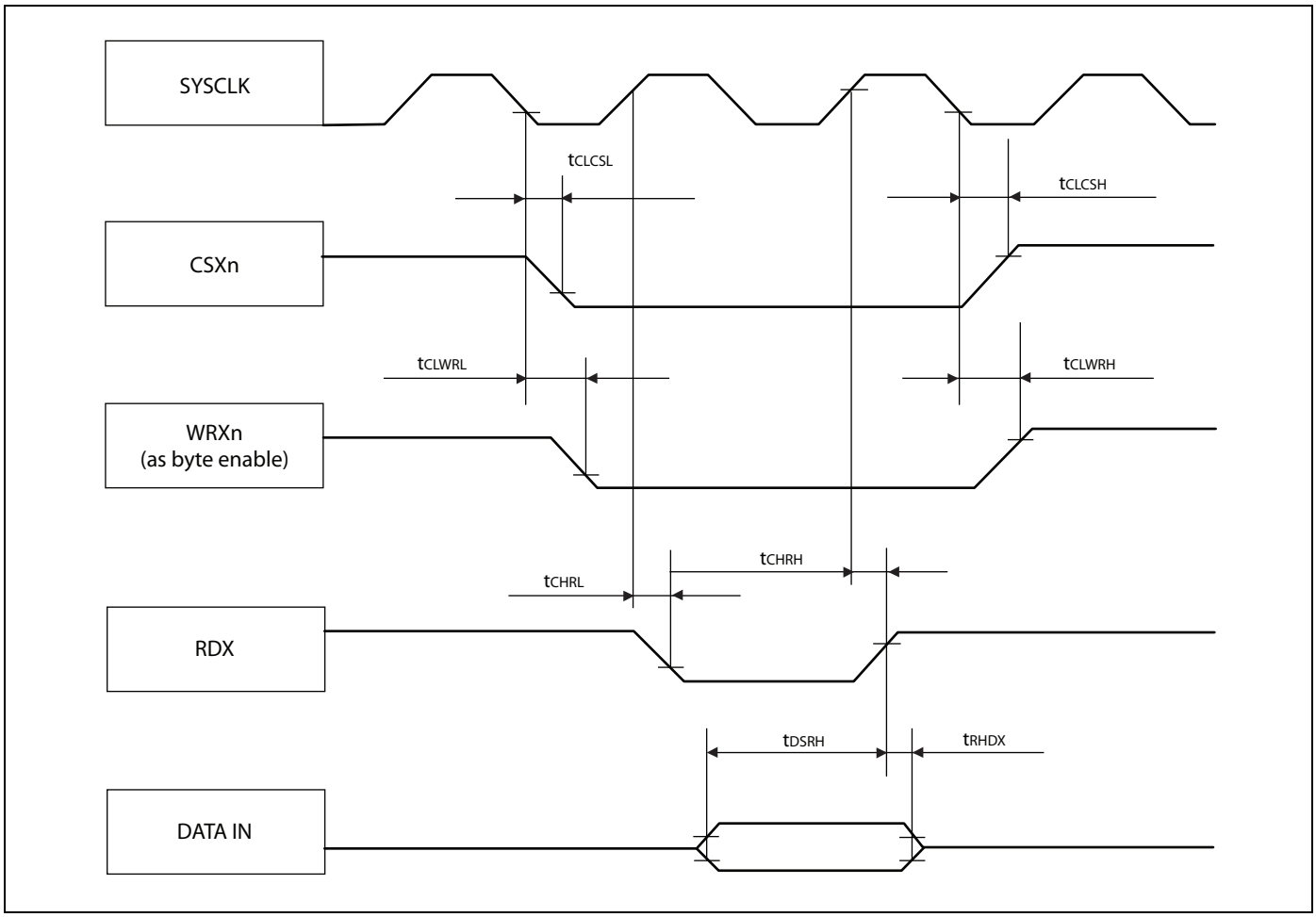
External clock mode (slave mode)



Synchronous/Asynchronous read access

(V_{DD}35 = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = −40°C to + 105°C)

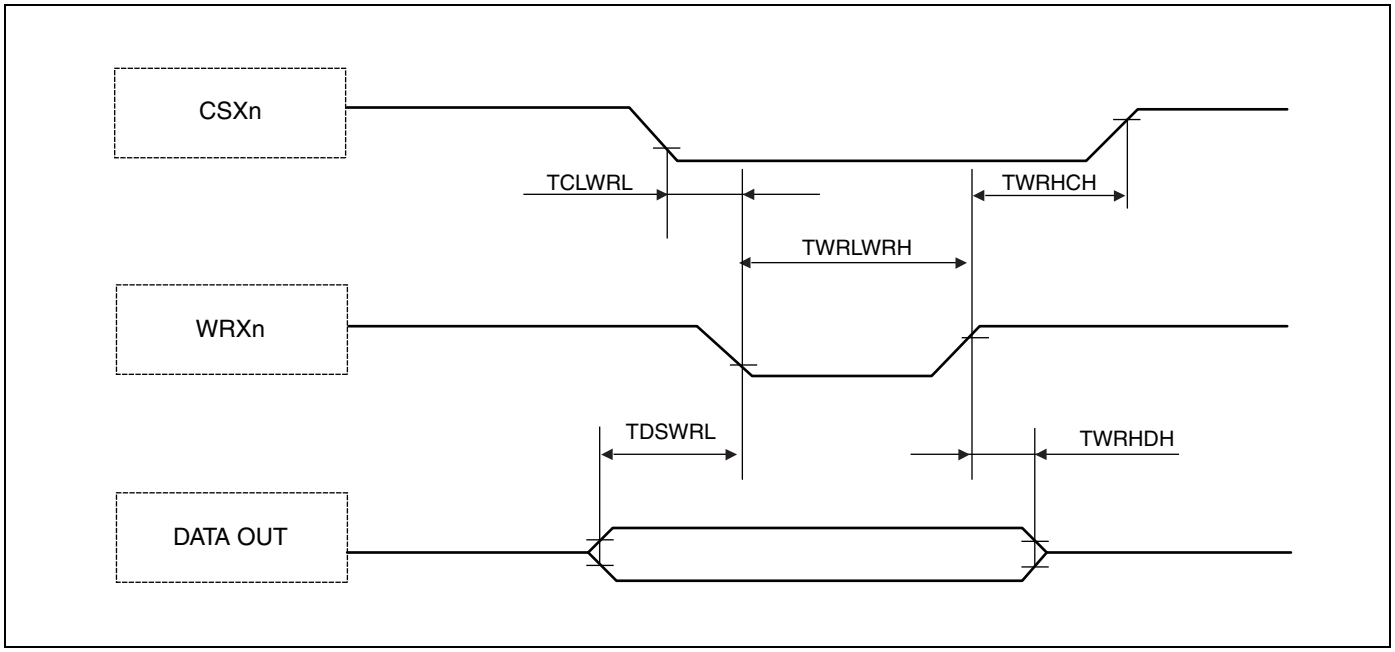
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↑ to RDX delay time	TCHRL	SYSCLK RDX	2	5	ns
	TCHRH		2	5	ns
Data valid to RDX ↑ setup time	TDSRH	RDX D31 to D16	12	—	ns
RDX ↑ to Data valid hold time	TRHDX	RDX D31 to D16	0	—	ns
SYSCLK ↓ to WRXn (as byte enable) delay time	TCLWRL	SYSCLK WRXn	—	5	ns
	TCLWRH		2	—	ns
SYSCLK ↓ to CSXn delay time	TCLCSL	SYSCLK CSXn	—	5	ns
	TCLCSH		—	5	ns



Asynchronous write access - no byte control type

(V_{DD}35 = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = −40°C to + 105°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WRXn ↓ to WRXn ↑ pulse width	TWRLWRH	WRXn	t_{CLKT} - 1	—	ns
Data valid to WRXn ↓ setup time	TDSWRL	WRXn D31 to D16	1/2 × t_{CLKT} - 1	—	ns
WRXn ↑ to Data valid hold time	TWRHDH	WRXn D31 to D16	1/2 × t_{CLKT} - 1	—	ns
WRXn to CSXn delay time	TCLWRL	WRXn CSXn	—	1/2 × t_{CLKT} + 1	ns
	TWRHCH		1/2 × t_{CLKT} - 1	—	ns



Asynchronous write access - byte control type

(V_{DD}35 = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = −40°C to + 105°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WEX ↓ to WEX ↑ pulse width	TWLWH	WEX	t_{CLKT}	—	ns
Data valid to WEX ↓ setup time	TDSWL	WEX D31 to D16	1/2 × t_{CLKT} - 7	—	ns
WEX ↑ to Data valid hold time	TWHDH	WEX D31 to D16	1/2 × t_{CLKT} - 3	—	ns
WEX to WRXn delay time	TWRLWL	WEX WRXn	—	1/2 × t_{CLKT} + 1	ns
	TWHWRH		1/2 × t_{CLKT} - 1	—	ns
WEX to CSXn delay time	TCLWL	WEX CSXn	—	1/2 × t_{CLKT} - 1	ns
	TWHCH		1/2 × t_{CLKT} - 1	—	ns