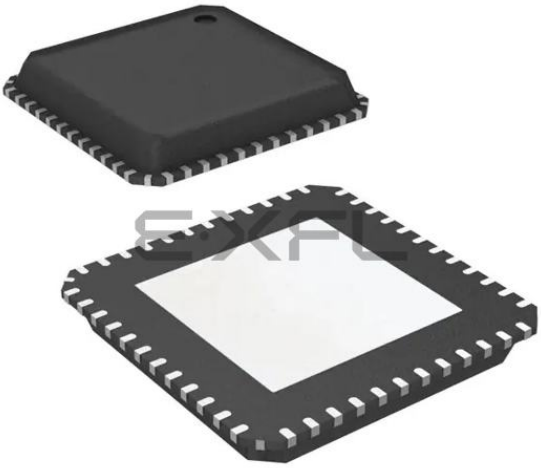
Infineon Technologies - XC2220U8F40VAAKXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	40MHz
Connectivity	I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-54
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2220u8f40vaakxuma1

XC2220U Data Sheet

Revision History: V1.2 2012-07

Previous Versions: V1.0 2010-12, V1.1 2011-09

Page	Subjects (major changes since last revision)
50, **51**	The value of absolute sum of overload currents parameter in absolute maximum rating parameter and operating conditions tables are switched.
72	Table description on coding of bit field LEVxV is updated.

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2.1 Pin Configuration and Definition

The pins of the XC2220U are described in detail in **Table 6**, which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. The following figure summarizes all pins, showing their locations on the four sides of the package.

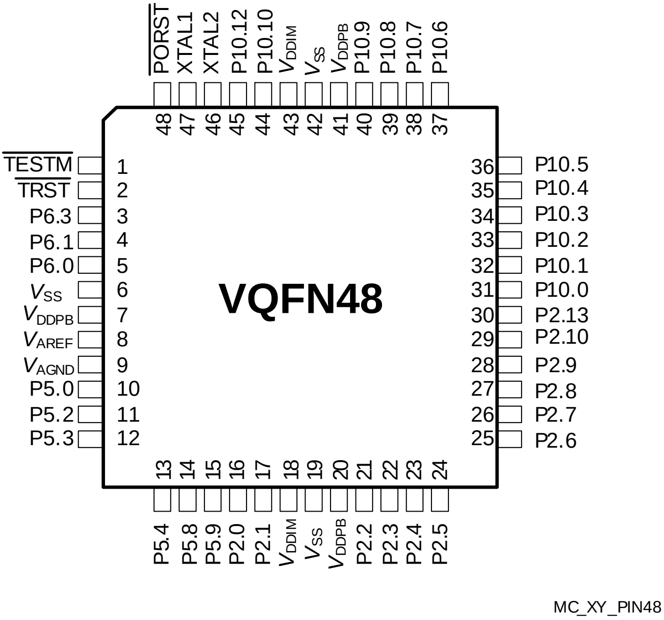

Figure 2 XC2220U Pin Configuration (top view)

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
33	P10.2	O0 / I	St/B	**Bit 2 of Port 10, General Purpose Input/Output**
	U0C0_SCLKOUT	O1	St/B	**USIC0 Channel 0 Shift Clock Output**
	CCU60_CC62	O2	St/B	**CCU60 Channel 2 Output**
	CCU60_CC62INA	I	St/B	**CCU60 Channel 2 Input**
	U0C0_DX1B	I	St/B	**USIC0 Channel 0 Shift Clock Input**
34	P10.3	O0 / I	St/B	**Bit 3 of Port 10, General Purpose Input/Output**
	CCU60_COUT60	O2	St/B	**CCU60 Channel 0 Output**
	U0C0_DX2A	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2A	I	St/B	**USIC0 Channel 1 Shift Control Input**
35	P10.4	O0 / I	St/B	**Bit 4 of Port 10, General Purpose Input/Output**
	U0C0_SELO3	O1	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CCU60_COUT61	O2	St/B	**CCU60 Channel 1 Output**
	U0C0_DX2B	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2B	I	St/B	**USIC0 Channel 1 Shift Control Input**
	ESR1_9	I	St/B	**ESR1 Trigger Input 9**
36	P10.5	O0 / I	St/B	**Bit 5 of Port 10, General Purpose Input/Output**
	U0C1_SCLKOUT	O1	St/B	**USIC0 Channel 1 Shift Clock Output**
	CCU60_COUT62	O2	St/B	**CCU60 Channel 2 Output**
	U0C1_DX1B	I	St/B	**USIC0 Channel 1 Shift Clock Input**
37	P10.6	O0 / I	St/B	**Bit 6 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	U0C0_DX0C	I	St/B	**USIC0 Channel 0 Shift Data Input**
	CCU60_CTRAPA	I	St/B	**CCU60 Emergency Trap Input**

3.1 Memory Subsystem and Organization

The memory space of the XC2220U is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

Table 8 XC2220U **Memory Map 1)**

Address Area	**Start Loc.**	**End Loc.**	**Area Size2)**	**Notes**
IMB register space	FF’FF00$_H$	FF’FFFF$_H$	256 bytes	
Reserved	F0’0000$_H$	FF’FEFF$_H$	< 1 Mbyte	Minus IMB registers.
Reserved for EPSRAM	E8’1000$_H$	EF’FFFF$_H$	508 Kbytes	Mirrors EPSRAM
Emulated PSRAM	E8’0000$_H$	E8’0FFF$_H$	up to 4 Kbytes	With Flash timing.
Reserved for PSRAM	E0’1000$_H$	E7’FFFF$_H$	508 Kbytes	Mirrors PSRAM
PSRAM	E0’0000$_H$	E0’0FFF$_H$	up to 4 Kbytes	Program SRAM.
Reserved for Flash	C1’1000$_H$	DF’FFFF$_H$	1980 Kbytes	
Flash 0	C0’0000$_H$	C1’0FFF$_H$	68 Kbytes3)	
External memory area	40’0000$_H$	BF’FFFF$_H$	8 Mbytes	
External IO area4)	21’0000$_H$	3F’FFFF$_H$	1984 Kbytes	
Reserved	20’B400$_H$	20’FFFF$_H$	19 Kbytes	
USIC0 alternate regs.	20’B000$_H$	20’B3FF$_H$	1 Kbytes	Accessed via LXBus controller
Reserved	20’4800$_H$	20’AFFF$_H$	26 Kbytes	
USIC0 registers	20’4000$_H$	20’47FF$_H$	2 Kbytes	Accessed via LXBus controller
Reserved	20’0000$_H$	20’3FFF$_H$	16 Kbytes	
External memory area	01’0000$_H$	1F’FFFF$_H$	1984 Kbytes	
SFR area	00’FE00$_H$	00’FFFF$_H$	0.5 Kbytes	
Dual-port RAM (DPRAM)	00’F600$_H$	00’FDFF$_H$	2 Kbytes	
Reserved for DPRAM	00’F200$_H$	00’F5FF$_H$	1 Kbytes	
ESFR area	00’F000$_H$	00’F1FF$_H$	0.5 Kbytes	
XSFR area	00’E000$_H$	00’EFFF$_H$	4 Kbytes	
Data SRAM (DSRAM)	00’D800$_H$	00’DFFF$_H$	2 Kbytes	

3.2 Central Processing Unit (CPU)

The core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply-and-divide unit, a bit-mask generator, and a barrel shifter.

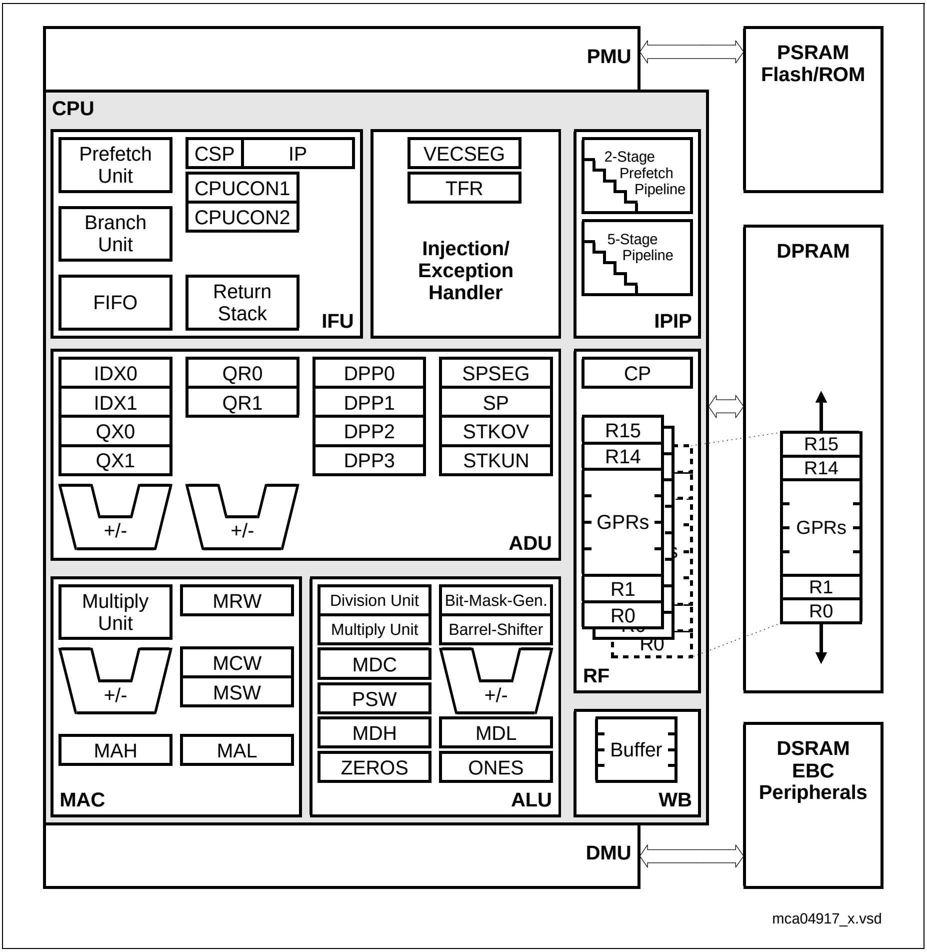

Figure 4 CPU Block Diagram

3.3 Memory Protection Unit (MPU)

The XC2220U's Memory Protection Unit (MPU) protects user-specified memory areas from unauthorized read, write, or instruction fetch accesses. The MPU can protect the whole address space including the peripheral area. This completes established mechanisms such as the register security mechanism or stack overrun/underrun detection.

Four Protection Levels support flexible system programming where operating system, low level drivers, and applications run on separate levels. Each protection level permits different access restrictions for instructions and/or data.

Every access is checked (if the MPU is enabled) and an access violating the permission rules will be marked as invalid and leads to a protection trap.

A set of protection registers for each protection level specifies the address ranges and the access permissions. Applications requiring more than 4 protection levels can dynamically re-program the protection registers.

3.4 Memory Checker Module (MCHK)

The XC2220U's Memory Checker Module calculates a checksum (fractional polynomial division) on a block of data, often called Cyclic Redundancy Code (CRC). It is based on a 32-bit linear feedback shift register and may, therefore, also be used to generate pseudo-random numbers.

The Memory Checker Module is a 16-bit parallel input signature compression circuitry which enables error detection within a block of data stored in memory, registers, or communicated e.g. via serial communication lines. It reduces the probability of error masking due to repeated error patterns by calculating the signature of blocks of data.

The polynomial used for operation is configurable, so most of the commonly used polynomials may be used. Also, the block size for generating a CRC result is configurable via a local counter. An interrupt may be generated if testing the current data block reveals an error.

An autonomous CRC compare circuitry is included to enable redundant error detection, e.g. to enable higher safety integrity levels.

The Memory Checker Module provides enhanced fault detection (beyond parity or ECC) for data and instructions in volatile and non volatile memories. This is especially important for the safety and reliability of embedded systems.

3.5 Interrupt System

The architecture of the XC2220U supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Using a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed. With the PEC just one cycle is ‘stolen’ from the current CPU activity to perform the PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XC2220U has eight PEC channels, each with fast interrupt-driven data transfer capabilities.

With a minimum interrupt response time of 7/11¹⁾ CPU clocks, the XC2220U can react quickly to the occurrence of non-deterministic events.

Interrupt Nodes and Source Selection

The interrupt system provides 46 physical nodes with separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bit field. Most interrupt sources are assigned to a dedicated node. A particular subset of interrupt sources shares a set of nodes. The source selection can be programmed using the interrupt source selection (ISSR) registers.

External Request Unit (ERU)

A dedicated External Request Unit (ERU) is provided to route and preprocess selected on-chip peripheral and external interrupt requests. The ERU features 4 programmable input channels with event trigger logic (ETL) a routing matrix and 4 output gating units (OGU). The ETL features rising edge, falling edge, or both edges event detection. The OGU combines the detected interrupt events and provides filtering capabilities depending on a programmable pattern match or miss.

Trap Processing

The XC2220U provides efficient mechanisms to identify and process exceptions or error conditions that arise during run-time, the so-called ‘Hardware Traps’. A hardware trap causes an immediate system reaction similar to a standard interrupt service (branching

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1) Depending if the jump cache is used or not.

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The counting direction (up/down) for each timer can be programmed by software or altered dynamically with an external signal on a port pin (TxEUD). Concatenation of the timers is supported with the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can also be used to clock the CAPCOM2 timers and to initiate a reload from the CAPREL register.

The CAPREL register can capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN); timer T5 may optionally be cleared after the capture procedure. This allows the XC2220U to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) can also be generated upon transitions of GPT1 timer T3 inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

3.11 A/D Converters

For analog signal measurement, a 12-bit A/D converters (ADC0) with 10 multiplexed input channels and a sample and hold circuit have been integrated on-chip. Conversions use the successive approximation method. The sample time (to charge the capacitors) and the conversion time are programmable so that they can be adjusted to the external circuit. The A/D converters can also operate in 8-bit and 10-bit conversion mode, further reducing the conversion time.

Several independent conversion result registers, selectable interrupt requests, and highly flexible conversion sequences provide a high degree of programmability to meet the application requirements.

For applications that require more analog input channels, external analog multiplexers can be controlled automatically. For applications that require fewer analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converters of the XC2220U support two types of request sources which can be triggered by several internal and external events.

- Parallel requests are activated at the same time and then executed in a predefined sequence.
- Queued requests are executed in a user-defined sequence.

In addition, the conversion of a specific channel can be inserted into a running sequence without disturbing that sequence. All requests are arbitrated according to the priority level assigned to them.

Data reduction features reduce the number of required CPU access operations allowing the precise evaluation of analog inputs (high conversion rate) even at a low CPU speed. Result data can be reduced by limit checking or accumulation of results. Two cascadable filters build the hardware to generate a configurable moving average.

The Peripheral Event Controller (PEC) can be used to control the A/D converters or to automatically store conversion results to a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer. Each A/D converter contains eight result registers which can be concatenated to build a result FIFO. Wait-for-read mode can be enabled for each result register to prevent the loss of conversion data.

In order to decouple analog inputs from digital noise and to avoid input trigger noise, those pins used for analog input can be disconnected from the digital input stages. This can be selected for each pin separately with the Port x Digital Input Disable registers.

The Auto-Power-Down feature of the A/D converters minimizes the power consumption when no conversion is in progress.

Broken wire detection for each channel and a multiplexer test mode provide information to verify the proper operation of the analog signal sources (e.g. a sensor system).

8) Value is controlled by on-chip regulator.

4.2 Voltage Range definitions

The XC2220U timing depends on the supply voltage. If such a dependency exists the timing values are given for 2 voltage areas commonly used. The voltage areas are defined in the following tables.

Table 14 Upper Voltage Range Definition

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	4.5	5.0	5.5	V	

Table 15 Lower Voltage Range Definition

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	3.0	3.3	4.5	V	

4.2.1 Parameter Interpretation

The parameters listed in the following include both the characteristics of the XC2220U and its demands on the system. To aid in correctly interpreting the parameters when evaluating them for a design, they are marked accordingly in the column “Symbol”:

CC (**C**ontroller **C**haracteristics):
The logic of the XC2220U provides signals with the specified characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the specified characteristics to the XC2220U.

Conversion 8-bit:

t_{C8} $= 10 \times t_{ADCI} + 2 \times t_{SYS} = 10 \times 50\text{ ns} + 2 \times 25\text{ ns} = 0.55\ \mu\text{s}$

Table 27 Flash Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Number of erase cycles	N_{ER} SR	–	–	15000	cycles	$t_{\mathrm{RET}} \geq$ 5 years; Valid for up to 64 user selected sectors (data storage)
		–	–	1000	cycles	$t_{\mathrm{RET}} \geq$ 20 years

1) All Flash module(s) can be erased/programmed while code is executed and/or data is read from only one Flash module or from PSRAM. The Flash module that delivers code/data can, of course, not be erased/programmed.

2) Value of IMB_IMBCTRL.WSFLASH.

3) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This increases the stated durations noticably only at extremely low system clock frequencies.

Access to the XC2220U Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.

4.7.2 Definition of Internal Timing

The internal operation of the XC2220U is controlled by the internal system clock f_{SYS}.

Because the system clock signal f_{SYS} can be generated from a number of internal and external sources using different mechanisms, the duration of the system clock periods (TCSs) and their variation (as well as the derived external timing) depend on the mechanism used to generate f_{SYS}. This must be considered when calculating the timing for the XC2220U.

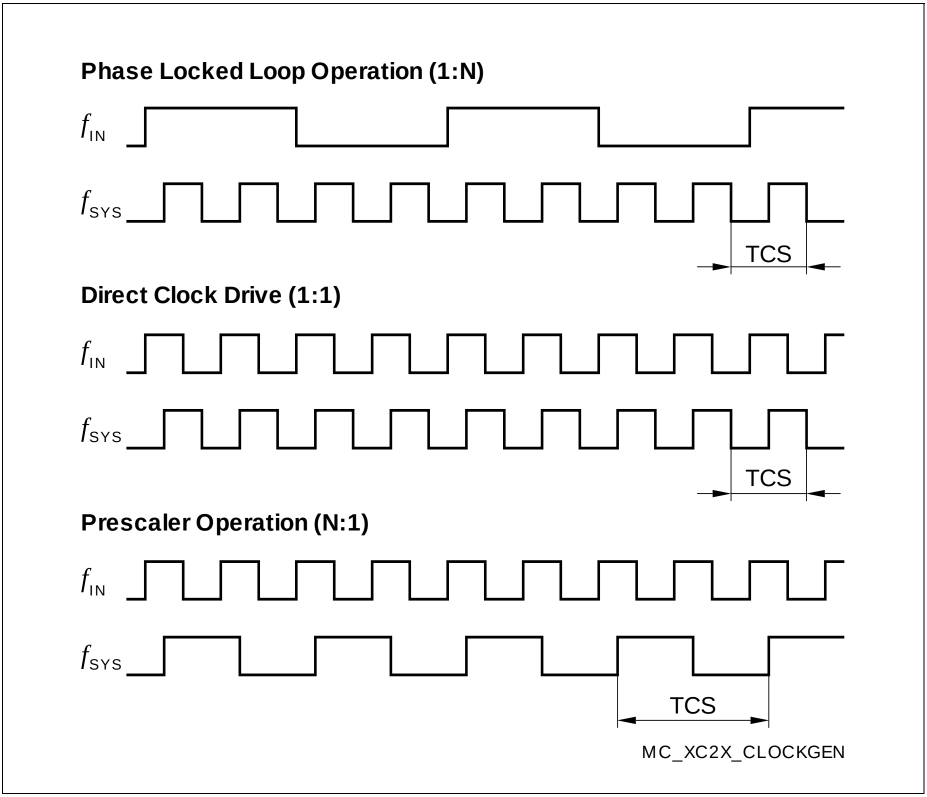

Figure 17 Generation Mechanisms for the System Clock

Note: The example of PLL operation shown in ***Figure 17*** *uses a PLL factor of 1:4; the example of prescaler operation uses a divider factor of 2:1.*

The specification of the external timing (AC Characteristics) depends on the period of the system clock (TCS).

4.7.3 External Clock Input Parameters

These parameters specify the external clock generation for the XC2220U. The clock can be generated in two ways:

- By connecting a **crystal or ceramic resonator** to pins XTAL1/XTAL2.
- By supplying an **external clock signal**. This clock signal can be supplied either to pin XTAL1 (core voltage domain) or to pin CLKIN1 (IO voltage domain).

If connected to CLKIN1, the input signal must reach the defined input levels V_{IL} and V_{IH}. If connected to XTAL1, a minimum amplitude V_{AX1} (peak-to-peak voltage) is sufficient for the operation of the on-chip oscillator.

Note: The given clock timing parameters (t_1 … t_4) are only valid for an external clock input signal.

Note: Operating Conditions apply.

Table 29 External Clock Input Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Oscillator frequency	f_{OSC} SR	4	–	40	MHz	Input= Clock Signal
		4	–	16	MHz	Input= Crystal or Resonator
XTAL1 input current absolute value	$\|I_{IL}\|$ CC	–	–	20	μA	
Input clock high time	t_1 SR	6	–	–	ns	
Input clock low time	t_2 SR	6	–	–	ns	
Input clock rise time	t_3 SR	–	8	8	ns	
Input clock fall time	t_4 SR	–	8	8	ns	
Input voltage amplitude on XTAL1[1]	V_{AX1} SR	0.3 x V_{DDIM}	–	–	V	$f_{OSC} \geq$ 4 MHz; $f_{OSC} \leq$ 16 MHz
		0.4 x V_{DDIM}	–	–	V	$f_{OSC} \geq$ 16 MHz; $f_{OSC} \leq$ 25 MHz
		0.5 x V_{DDIM}	–	–	V	$f_{OSC} \geq$ 25 MHz; $f_{OSC} \leq$ 40 MHz
Input voltage range limits for signal on XTAL1	V_{IX1} SR	-1.7 + V_{DDIM}	–	1.7	V	[2]

[1] The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF}. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1}.

Table 30 Standard Pad Parameters for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise and Fall times (10% - 90%)	t_{RF} CC	–	–	38 + 0.6 x C_L	ns	$C_L \geq 20$ pF; $C_L \leq 100$ pF; Driver_Strength = Medium
		–	–	1 + 0.45 x C_L	ns	$C_L \geq 20$ pF; $C_L \leq 100$ pF; Driver_Strength = Strong ; Driver_Edge= Soft
		–	–	16 + 0.45 x C_L	ns	$C_L \geq 20$ pF; $C_L \leq 100$ pF; Driver_Strength = Strong ; Driver_Edge= Slow
		–	–	200 + 2.5 x C_L	ns	$C_L \geq 20$ pF; $C_L \leq 100$ pF; Driver_Strength = Weak

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1) The total output current that may be drawn at a given time must be limited to protect the supply rails from damage. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and ΣI_{OH}) must remain below 25 mA.

Table 31 Standard Pad Parameters for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum output driver current (absolute value)[1]	I_{Omax} CC	–	–	1.8	mA	Driver_Strength = Medium
		–	–	3.0	mA	Driver_Strength = Strong
		–	–	0.3	mA	Driver_Strength = Weak

4.7.5 Synchronous Serial Interface Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: These parameters are not subject to production test but verified by design and/or characterization.

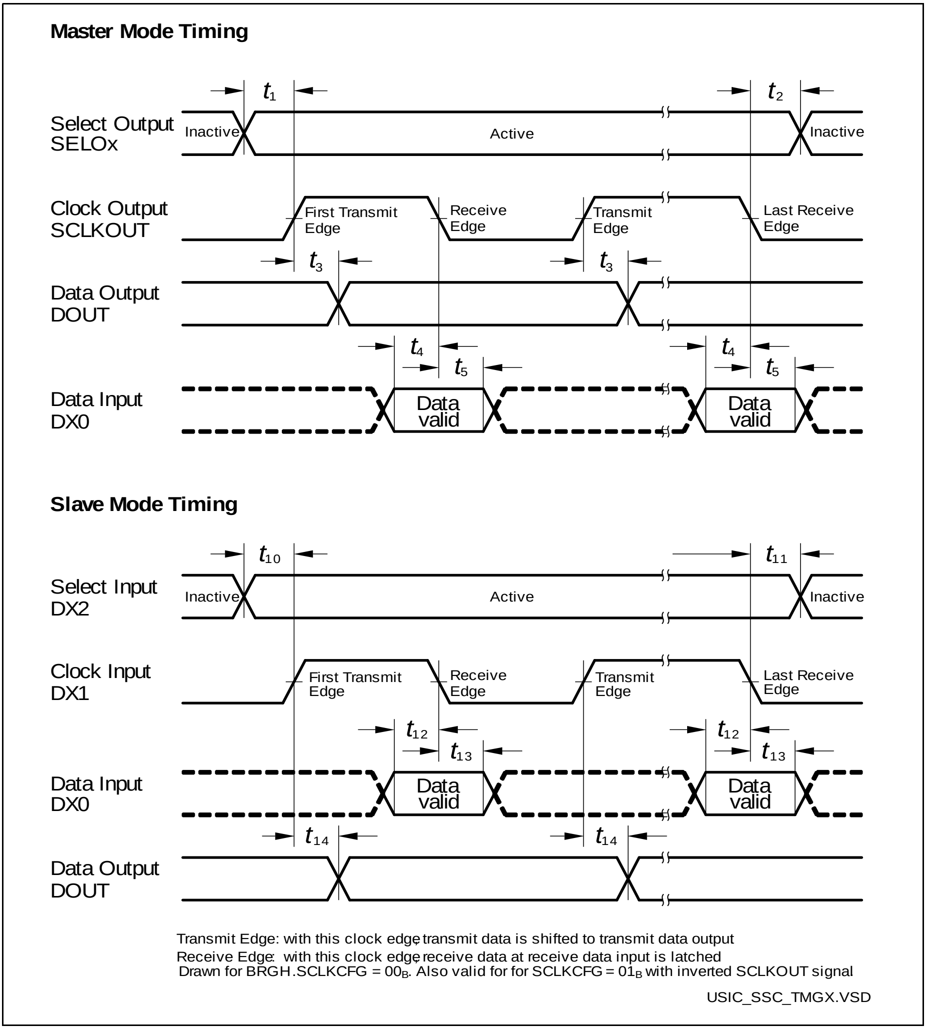
Note: Operating Conditions apply.

Table 32 is valid under the following conditions: C_L= 20 pF; SSC= master ; voltage_range= upper

Table 32 USIC SSC Master Mode Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	t_{SYS} - 8[1]	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	t_{SYS} - 6[1]	–	–	ns	
Data output DOUT valid time	t_3 CC	-6	–	9	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	31	–	–	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-4	–	–	ns	

1) $t_{SYS} = 1 / f_{SYS}$



Transmit Edge: with this clock edge, transmit data is shifted to transmit data output
Receive Edge: with this clock edge, receive data at receive data input is latched
Drawn for BRGH.SCLKCFG = 00_B. Also valid for for SCLKCFG = 01_B with inverted SCLKOUT signal

Figure 20 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.

Table 39 is valid under the following conditions: C_L= 20 pF; voltage_range= lower

Table 39 JTAG Interface Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	100[1]	–	–	ns	
TCK high time	t_2 SR	16	–	–	ns	
TCK low time	t_3 SR	16	–	–	ns	
TCK clock rise time	t_4 SR	–	–	8	ns	
TCK clock fall time	t_5 SR	–	–	8	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	
TDO valid from TCK falling edge (propagation delay)[2]	t_8 CC	–	39	43	ns	
TDO high impedance to valid output from TCK falling edge[3][2]	t_9 CC	–	39	43	ns	
TDO valid output to high impedance from TCK falling edge[2]	t_{10} CC	–	39	43	ns	
TDO hold after TCK falling edge[2]	t_{18} CC	5	–	–	ns	

1) The debug interface cannot operate faster than the overall system, therefore $t_1 \geq t_{SYS}$.

2) The falling edge on TCK is used to generate the TDO timing.

3) The setup time for TDO is given implicitly by the TCK cycle time.

5 Package and Reliability

The XC2000 Family devices use the package type:

- PG-VQFN (Plastic Green - Very Thin Profile Quad Flat Non-Leaded Package)

The following specifications must be regarded to ensure proper integration of the XC2220U in its target environment.

5.1 Packaging

These parameters specify the packaging rather than the silicon.

Table 40 Package Parameters (PG-VQFN-48-54)

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Exposed Pad Dimension	Ex × Ey	–	5.2 x 5.2	mm	–
Power Dissipation	P_{DISS}	–	0.6	W	–
Thermal resistance Junction-Ambient	$R_{\Theta\text{JA}}$	–	75	K/W	No thermal via, 2-layer[1]
			51	K/W	No thermal via, 4-layer[2]
			46	K/W	4-layer, no pad[3]
			36	K/W	4-layer, pad[4]

1) Device mounted on a 2-layer JEDEC board (according to JESD 51-3) without thermal vias; exposed pad not soldered.

2) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) without thermal vias; exposed pad not soldered.

3) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad not soldered.

4) Device mounted on a 4-layer JEDEC board (according to JESD 51-7) with thermal vias; exposed pad soldered to the board.

Note: To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground, independent of the thermal requirements.
Board layout examples are given in an application note.

Package Compatibility Considerations

The XC2220U is a member of the XC2000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In

5.2 Thermal Considerations

When operating the XC2220U in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 150 °C.

The difference between junction temperature and ambient temperature is determined by
$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$
The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).
The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$
The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers