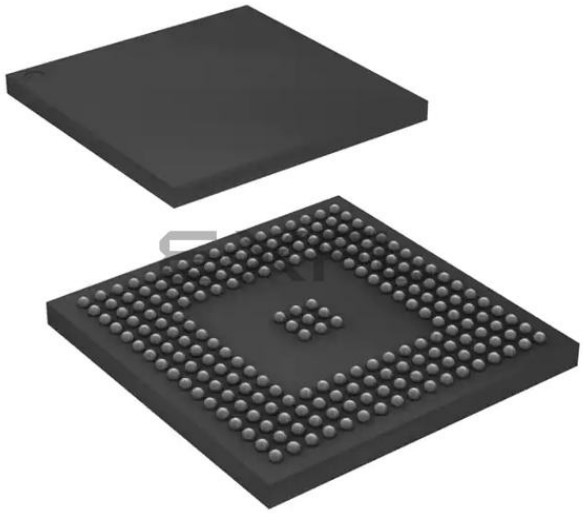

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

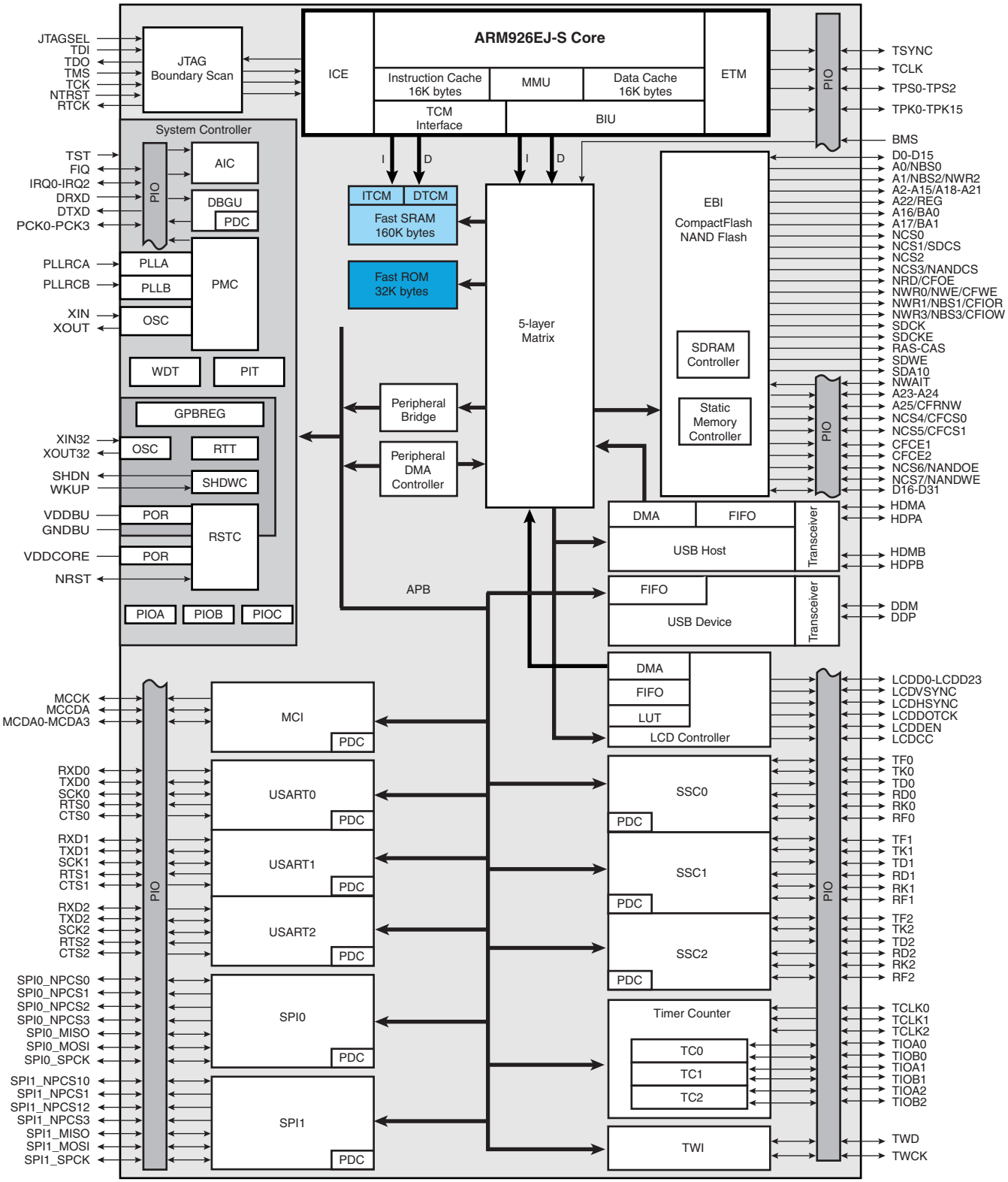
## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM926EJ-S |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 190MHz |
| Co-Processors/DSP | - |
| RAM Controllers | SDRAM, SRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | LCD |
| Ethernet | - |
| SATA | - |
| USB | USB 2.0 (2) |
| Voltage - I/O | 3.0V, 3.3V |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Security Features | - |
| Package / Case | 217-LFBGA |
| Supplier Device Package | 217-LFBGA (15x15) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/at91sam9261b-cu |

# 2. Block Diagram

**Figure 2-1.** AT91SAM9261 Block Diagram



# 3. Signal Description

**Table 3-1.** Signal Description by Peripheral

| Signal Name | Function | Type | Active Level | Comments |
|---|---|---|---|---|
| **Power** | | | | |
| VDDIOM | EBI I/O Lines Power Supply | Power | | 1.65 V to 1.95V and 3.0V to 3.6V |
| VDDIOP | Peripherals I/O Lines Power Supply | Power | | 2.7V to 3.6V |
| VDDBU | Backup I/O Lines Power Supply | Power | | 1.08V to 1.32V |
| VDDPLL | PLL Power Supply | Power | | 3.0V to 3.6V |
| VDDOSC | Oscillator Power Supply | Power | | 3.0V to 3.6V |
| VDDCORE | Core Chip Power Supply | Power | | 1.08V to 1.32V |
| GND | Ground | Ground | | |
| GNDPLL | PLL Ground | Ground | | |
| GNDOSC | Oscillator Ground | Ground | | |
| GNDBU | Backup Ground | Ground | | |
| **Clocks, Oscillators and PLLs** | | | | |
| XIN | Main Oscillator Input | Input | | |
| XOUT | Main Oscillator Output | Output | | |
| XIN32 | Slow Clock Oscillator Input | Input | | |
| XOUT32 | Slow Clock Oscillator Output | Output | | |
| PLLRCA | PLL Filter | Input | | |
| PLLRCB | PLL Filter | Input | | |
| PCK0 - PCK3 | Programmable Clock Output | Output | | |
| **Shutdown, Wakeup Logic** | | | | |
| SHDN | Shutdown Control | Output | | Do not tie over VDDBU. |
| WKUP | Wake-Up Input | Input | | Accepts between 0V and VDDBU. |
| **ICE and JTAG** | | | | |
| TCK | Test Clock | Input | | No pull-up resistor. |
| RTCK | Returned Test Clock | Output | | No pull-up resistor. |
| TDI | Test Data In | Input | | No pull-up resistor. |
| TDO | Test Data Out | Output | | |
| TMS | Test Mode Select | Input | | No pull-up resistor. |
| NTRST | Test Reset Signal | Input | Low | Pull-up resistor. |
| JTAGSEL | JTAG Selection | Input | | Pull-down resistor. Accepts between 0V and VDDBU. |
| **ETM™** | | | | |
| TSYNC | Trace Synchronization Signal | Output | | |
| TCLK | Trace Clock | Output | | |
| TPS0 - TPS2 | Trace ARM Pipeline Status | Output | | |
| TPK0 - TPK15 | Trace Packet Port | Output | | |

**Table 3-1.** Signal Description by Peripheral (Continued)

| Signal Name | Function | Type | Active Level | Comments |
|---|---|---|---|---|
| **Reset/Test** | | | | |
| NRST | Microcontroller Reset | I/O | Low | Pull-up resistor |
| TST | Test Mode Select | Input | | Pull-down resistor. |
| BMS | Boot Mode Select | Input | | |
| **Debug Unit** | | | | |
| DRXD | Debug Receive Data | Input | | |
| DTXD | Debug Transmit Data | Output | | |
| **AIC** | | | | |
| IRQ0 - IRQ2 | External Interrupt Inputs | Input | | |
| FIQ | Fast Interrupt Input | Input | | |
| **PIO** | | | | |
| PA0 - PA31 | Parallel IO Controller A | I/O | | Pulled-up input at reset |
| PB0 - PB31 | Parallel IO Controller B | I/O | | Pulled-up input at reset |
| PC0 - PC31 | Parallel IO Controller C | I/O | | Pulled-up input at reset |
| **EBI** | | | | |
| D0 - D31 | Data Bus | I/O | | Pulled-up input at reset |
| A0 - A25 | Address Bus | Output | | 0 at reset |
| NWAIT | External Wait Signal | Input | Low | |
| **SMC** | | | | |
| NCS0 - NCS7 | Chip Select Lines | Output | Low | |
| NWR0 - NWR3 | Write Signal | Output | Low | |
| NRD | Read Signal | Output | Low | |
| NWE | Write Enable | Output | Low | |
| NBS0 - NBS3 | Byte Mask Signal | Output | Low | |
| **CompactFlash Support** | | | | |
| CFCE1 - CFCE2 | CompactFlash Chip Enable | Output | Low | |
| CFOE | CompactFlash Output Enable | Output | Low | |
| CFWE | CompactFlash Write Enable | Output | Low | |
| CFIOR | CompactFlash IO Read | Output | Low | |
| CFIOW | CompactFlash IO Write | Output | Low | |
| CFRNW | CompactFlash Read Not Write | Output | | |
| CFCS0 - CFCS1 | CompactFlash Chip Select Lines | Output | Low | |
| **NAND Flash Support** | | | | |
| NANDOE | NAND Flash Output Enable | Output | Low | |
| NANDWE | NAND Flash Write Enable | Output | Low | |
| NANDCS | NAND Flash Chip Select | Output | Low | |

**Table 3-1.** Signal Description by Peripheral (Continued)

| Signal Name | Function | Type | Active Level | Comments |
|---|---|---|---|---|
| **SDRAM Controller** | | | | |
| SDCK | SDRAM Clock | Output | | |
| SDCKE | SDRAM Clock Enable | Output | High | |
| SDCS | SDRAM Controller Chip Select | Output | Low | |
| BA0 - BA1 | Bank Select | Output | | |
| SDWE | SDRAM Write Enable | Output | Low | |
| RAS - CAS | Row and Column Signal | Output | Low | |
| SDA10 | SDRAM Address 10 Line | Output | | |
| **Multimedia Card Interface** | | | | |
| MCCK | Multimedia Card Clock | Output | | |
| MCCDA | Multimedia Card A Command | I/O | | |
| MCDA0 - MCDA3 | Multimedia Card A Data | I/O | | |
| **USART** | | | | |
| SCK0 - SCK2 | Serial Clock | I/O | | |
| TXD0 - TXD2 | Transmit Data | Output | | |
| RXD0 - RXD2 | Receive Data | Input | | |
| RTS0 - RTS2 | Request To Send | Output | | |
| CTS0 - CTS2 | Clear To Send | Input | | |
| **Synchronous Serial Controller** | | | | |
| TD0 - TD2 | Transmit Data | Output | | |
| RD0 - RD2 | Receive Data | Input | | |
| TK0 - TK2 | Transmit Clock | I/O | | |
| RK0 - RK2 | Receive Clock | I/O | | |
| TF0 - TF2 | Transmit Frame Sync | I/O | | |
| RF0 - RF2 | Receive Frame Sync | I/O | | |
| **Timer/Counter** | | | | |
| TCLK0 - TCLK2 | External Clock Input | Input | | |
| TIOA0 - TIOA2 | I/O Line A | I/O | | |
| TIOB0 - TIOB2 | I/O Line B | I/O | | |
| **SPI** | | | | |
| SPI0_MISO - SPI1_MISO | Master In Slave Out | I/O | | |
| SPI0_MOSI - SPI1_MOSI | Master Out Slave In | I/O | | |
| SPI0_SPCK - SPI1_SPCK | SPI Serial Clock | I/O | | |
| SPI0_NPCS0, SPI1_NPCS0 | SPI Peripheral Chip Select 0 | I/O | Low | |
| SPI0_NPCS1 - SPI0_NPCS3<br>SPI1_NPCS1 - SPI1_NPCS3 | SPI Peripheral Chip Select | Output | Low | |

# 4. Package and Pinout

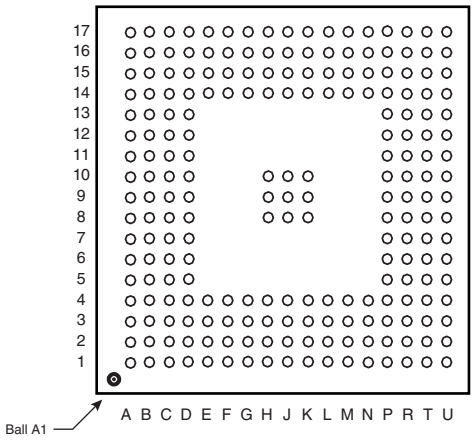
The AT91SAM9261 is available in a 217-ball LFBGA RoHS-compliant package, 15 x 15 mm, 0.8 mm ball pitch

## 4.1 217-ball LFBGA Package Outline

Figure 4-1 shows the orientation of the 217-ball LFBGA Package.

A detailed mechanical description is given in the section “AT91SAM9261 Mechanical Characteristics” of the product datasheet.

**Figure 4-1.** 217-ball LFBGA Package Outline (Top View)



# 7. Processor and Architecture

## 7.1 ARM926EJ-S Processor

- RISC Processor Based on ARM v5TEJ Architecture with Jazelle technology for Java acceleration
- Two Instruction Sets
  - ARM High-performance 32-bit Instruction Set
  - Thumb High Code Density 16-bit Instruction Set
- DSP Instruction Extensions
- 5-Stage Pipeline Architecture:
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)
  - Data Memory (M)
  - Register Write (W)
- 16 Kbyte Data Cache, 16 Kbyte Instruction Cache
  - Virtually-addressed 4-way Associative Cache
  - Eight words per line
  - Write-through and Write-back Operation
  - Pseudo-random or Round-robin Replacement
- Write Buffer
  - Main Write Buffer with 16-word Data Buffer and 4-address Buffer
  - DCache Write-back Buffer with 8-word Entries and a Single Address Entry
  - Software Control Drain
- Standard ARM v4 and v5 Memory Management Unit (MMU)
  - Access Permission for Sections
  - Access Permission for large pages and small pages can be specified separately for each quarter of the page
  - 16 embedded domains
- Bus Interface Unit (BIU)
  - Arbitrates and Schedules AHB Requests
  - Separate Masters for both instruction and data access providing complete AHB system flexibility
  - Separate Address and Data Buses for both the 32-bit instruction interface and the 32-bit data interface
  - On Address and Data Buses, data can be 8-bit (Bytes), 16-bit (Half-words) or 32-bit (Words)

## 7.2 Debug and Test Features

- Integrated Embedded In-circuit Emulator Real-Time
  - Two real-time Watchpoint Units
  - Two Independent Registers: Debug Control Register and Debug Status Register
  - Test Access Port Accessible through JTAG Protocol
  - Debug Communications Channel
- Debug Unit
  - Two-pin UART
  - Debug Communication Channel Interrupt Handling
  - Chip ID Register
- Embedded Trace Macrocell: ETM9™
  - Medium+ Level Implementation
  - Half-rate Clock Mode
  - Four Pairs of Address Comparators
  - Two Data Comparators
  - Eight Memory Map Decoder Inputs
  - Two 16-bit Counters
  - One 3-stage Sequencer
  - One 45-byte FIFO
- IEEE1149.1 JTAG Boundary-scan on All Digital Pins

## 7.3 Bus Matrix

- Five Masters and Five Slaves handled
  - Handles Requests from the ARM926EJ-S, USB Host Port, LCD Controller and the Peripheral DMA Controller to internal ROM, internal SRAM, EBI, APB, LCD Controller and USB Host Port.
  - Round-Robin Arbitration (three modes supported: no default master, last accessed default master, fixed default master)
  - Burst Breaking with Slot Cycle Limit
- One Address Decoder Provided per Master
  - Three different slaves may be assigned to each decoded memory area: one for internal boot, one for external boot, one after remap.
- Boot Mode Select Option
  - Non-volatile Boot Memory can be Internal or External.
  - Selection is made by BMS pin sampled at reset.
- Remap Command
  - Allows Remapping of an Internal SRAM in Place of the Boot Non-Volatile Memory
  - Allows Handling of Dynamic Exception Vectors

The memory blocks assigned to SRAM A, SRAM B and SRAM C areas are not contiguous and when the user dynamically changes the Internal SRAM configuration, the new 16 Kbyte block organization may affect the previous configuration from a software point of view.

Table 8-5 illustrates different configurations and the related 16 Kbyte blocks (RB0 to RB9) assignments.

**Table 8-5.** 16 Kbyte Block Allocation

| Decoded Area | Address | Configuration Examples and Related 16 Kbyte Block Assignments | | | |
|---|---|---|---|---|---|
| | | **ITCM = 0 Kbyte<br>DTCM = 0 Kbyte<br>AHB = 160 Kbytes** (1) | **ITCM = 64 Kbytes<br>DTCM = 64 Kbytes<br>AHB = 32 Kbytes** | **ITCM = 32 Kbytes<br>DTCM = 64 Kbytes<br>AHB = 64 Kbytes** | **ITCM = 32 Kbytes<br>DTCM = 16 Kbytes<br>AHB = 112 Kbytes** |
| Internal SRAM A (ITCM) | 0x0010 0000 | | RB3 | RB3 | RB3 |
| | 0x0010 4000 | | RB2 | RB2 | RB2 |
| | 0x0010 8000 | | RB1 | | |
| | 0x0010 C000 | | RB0 | | |
| Internal SRAM B (DTCM) | 0x0020 0000 | | RB7 | RB7 | RB7 |
| | 0x0020 4000 | | RB6 | RB6 | |
| | 0x0020 8000 | | RB5 | RB5 | |
| | 0x0020 C000 | | RB4 | RB4 | |
| Internal SRAM C (AHB) | 0x0030 0000 | RB9 | RB9 | RB9 | RB9 |
| | 0x0030 4000 | RB8 | RB8 | RB8 | RB8 |
| | 0x0030 8000 | RB7 | | RB1 | RB6 |
| | 0x0030 C000 | RB6 | | RB0 | RB5 |
| | 0x0031 0000 | RB5 | | | RB4 |
| | 0x0031 4000 | RB4 | | | RB1 |
| | 0x0031 8000 | RB3 | | | RB0 |
| | 0x0031 C000 | RB2 | | | |
| | 0x0032 0000 | RB1 | | | |
| | 0x0032 4000 | RB0 | | | |

Note: 1. Configuration after reset.

### *8.1.1.2 Internal ROM*

The AT91SAM9261 integrates a 32 Kbyte Internal ROM mapped at address 0x0040 0000. It is also accessible at address 0x0 after reset and before remap if the BMS is tied high during reset.

### *8.1.1.3 USB Host Port*

The AT91SAM9261 integrates a USB Host Port Open Host Controller Interface (OHCI). The registers of this interface are directly accessible on the AHB Bus and are mapped like a standard internal memory at address 0x0050 0000.

### *8.1.1.4 LCD Controller*

The AT91SAM9261 integrates an LCD Controller. The interface is directly accessible on the AHB Bus and is mapped like a standard internal memory at address 0x0060 0000.

### 8.1.2 Boot Strategies

The system always boots at address 0x0. To ensure a maximum number of possibilities for boot, the memory layout can be configured with two parameters.

REMAP allows the user to lay out the first internal SRAM bank to 0x0 to ease development. This is done by software once the system has booted for each Master of the Bus Matrix. Refer to the Bus Matrix Section for more details.

When REMAP = 0, BMS allows the user to lay out to 0x0, at his convenience, the ROM or an external memory. This is done via hardware at reset.

Note: Memory blocks not affected by these parameters can always be seen at their specified base addresses. See the complete memory map presented in Figure 8-1 on page 16.

The AT91SAM9261 Bus Matrix manages a boot memory that depends on the level on the BMS pin at reset. The internal memory area mapped between address 0x0 and 0x000F FFFF is reserved for this purpose.

If BMS is detected at 1, the boot memory is the embedded ROM.

If BMS is detected at 0, the boot memory is the memory connected on the Chip Select 0 of the External Bus Interface.

#### *8.1.2.1 BMS = 1, Boot on Embedded ROM*

The system boots using the Boot Program.

- Downloads and runs an application from external storage media into internal SRAM
- Downloaded code size depends on embedded SRAM size
- Automatic detection of valid application
- Bootloader on a non-volatile memory
  - SDCard
  - NAND Flash
  - SPI DataFlash connected on NPCS0 of the SPI
- SAM-BA® boot in case no valid program is detected in external NVM, supporting:
  - Serial communication on a DBGU
  - USB Device HS Port

#### *8.1.2.2 BMS = 0, Boot on External Memory*

- Boot on slow clock (32,768 Hz)
- Boot with the default configuration for the Static Memory Controller, byte select mode, 16-bit data bus, Read/Write controlled by Chip Select, allows boot on 16-bit non-volatile memory.

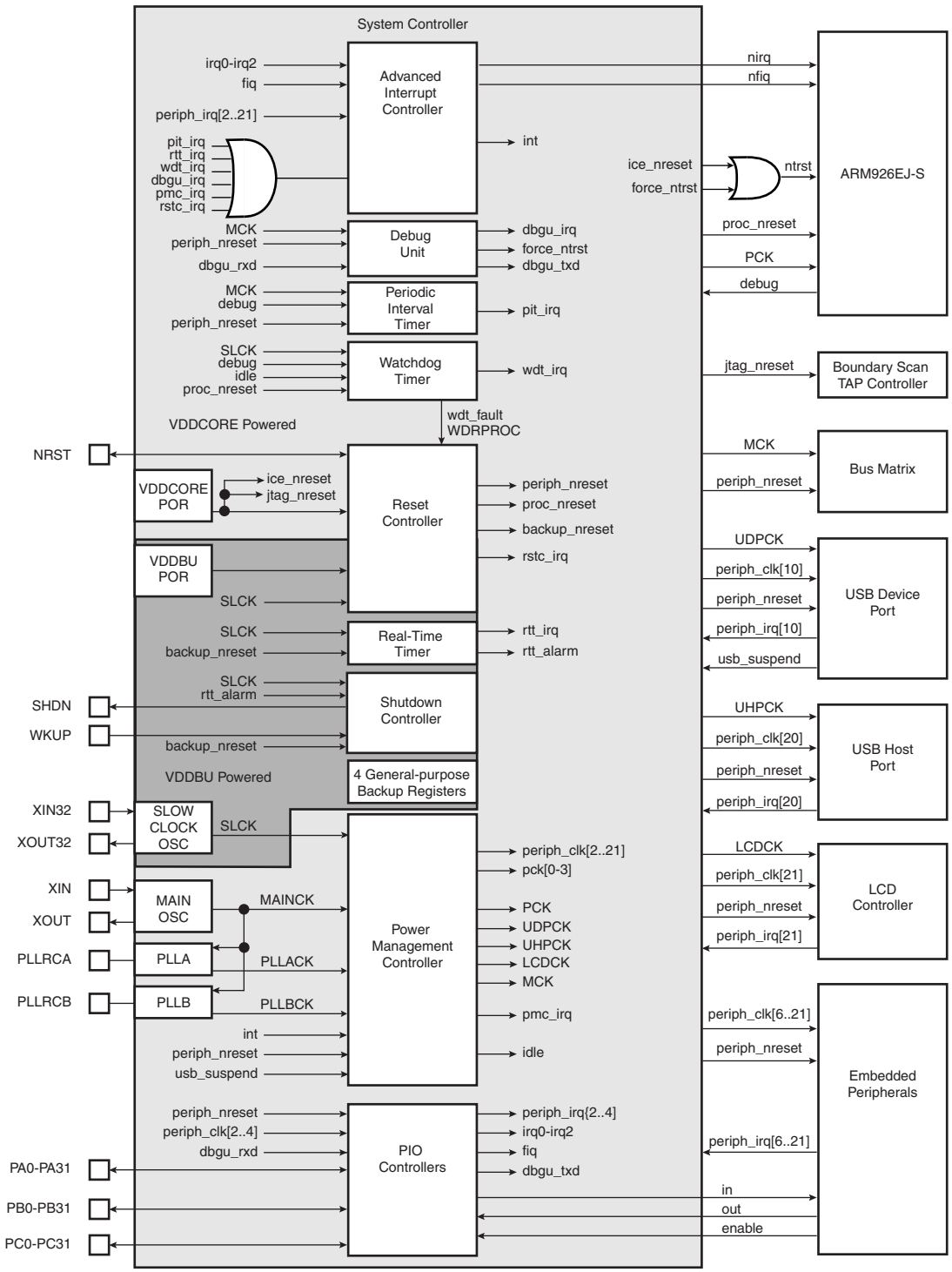
The customer-programmed software must perform a complete configuration.

To speed up the boot sequence when booting at 32 kHz EBI CS0 (BMS=0), the user must take the following steps:

1. Program the PMC (main oscillator enable or bypass mode).
2. Program and start the PLL.
3. Reprogram the SMC setup, cycle, hold, mode timings registers for CS0 to adapt them to the new clock
4. Switch the main clock to the new value.

## 9.1 Block Diagram

**Figure 9-1.** System Controller Block Diagram



## 9.10 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of an ARM Processor
- Thirty-two individually maskable and vectored interrupt sources
  - Source 0 is reserved for the Fast Interrupt Input (FIQ)
  - Source 1 is reserved for system peripherals (PIT, RTT, PMC, DBGU, etc.)
  - Source 2 to Source 31 control up to thirty embedded peripheral interrupts or external interrupts
  - Programmable edge-triggered or level-sensitive internal sources
  - Programmable positive/negative edge-triggered or high/low level-sensitive
- Four External Sources
- 8-level Priority Controller
  - Drives the normal interrupt of the processor
  - Handles priority of the interrupt sources 1 to 31
  - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
  - Optimizes Interrupt Service Routine Branch and Execution
  - One 32-bit Vector Register per interrupt source
  - Interrupt Vector Register reads the corresponding current Interrupt Vector
- Protect Mode
  - Easy debugging by preventing automatic operations when protect mode is enabled
- Fast Forcing
  - Permits redirecting any normal interrupt source on the Fast Interrupt of the processor
- General Interrupt Mask
  - Provides processor synchronization on events without triggering an interrupt

## 9.11 Debug Unit

- Composed of four functions
  - Two-pin UART
  - Debug Communication Channel (DCC) support
  - Chip ID Registers
  - ICE Access Prevention
- Two-pin UART
  - Implemented features are 100% compatible with the standard Atmel USART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Support for two PDC channels with connection to receiver and transmitter
- Debug Communication Channel Support

  - Offers visibility of COMMRX and COMMTX signals from the ARM Processor
- Chip ID Registers
  - Identification of the device revision, sizes of the embedded memories, set of peripherals
- ICE Access prevention
  - Enables software to prevent system access through the ARM Processor's ICE
  - Prevention is made by asserting the NTRST line of the ARM Processor's ICE

## 9.12 PIO Controllers

- Three PIO Controllers, each controlling up to 32 programmable I/O Lines
  - PIOA has 32 I/O Lines
  - PIOB has 32 I/O Lines
  - PIOC has 32 I/O Lines
- Fully programmable through Set/Clear Registers
- Multiplexing of two peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general-purpose I/O)
  - Input change interrupt
  - Glitch filter
  - Multi-drive option enables driving in open drain
  - Programmable pull up on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

- using the three Timer Counter channels' outputs and trigger inputs
- using the SSC2

#### 10.3.1.5 *NAND Flash Interface*

Using the NAND Flash interface prevents:

- using NCS3, NCS6 and NCS7 to access other parallel devices

#### 10.3.1.6 *Compact Flash Interface*

Using the CompactFlash interface prevents:

- using NCS4 and/or NCS5 to access other parallel devices

#### 10.3.1.7 *SPI0 and the MultiMedia Card Interface*

As the DataFlash Card is compatible with the SDCard, it is useful to multiplex SPI and MCI. Here, the SPI0 signal is multiplexed with the MCI.

#### 10.3.1.8 *USARTs*

- Using the USART1 and USART2 control signals prevents using the ETM.
- Alternatively, using USART0 with its control signals prevents using some clock outputs and interrupt lines.

#### 10.3.1.9 *Clock Outputs*

- Using the clock outputs multiplexed with the PIO A prevents using the Debug Unit and/or the Two Wire Interface.
- Alternatively, using the second implementation of the clock outputs prevents using the LCD Controller Interface and/or USART0.

#### 10.3.1.10 *Interrupt Lines*

- Using FIQ prevents using the USART0 control signals.
- Using IRQ0 prevents using the NWAIT EBI signal.
- Using the IRQ1 and/or IRQ2 prevents using the SPI1.

### 10.3.2 PIO Controller A Multiplexing

**Table 10-2.** Multiplexing on PIO Controller A

| PIO Controller A | | | | | Application Usage | | |
|---|---|---|---|---|---|---|---|
| I/O Line | Peripheral A | Peripheral B | Comments | Reset State | Power Supply | Function | Comments |
| PA0 | SPI0_MISO | MCDA0 | | I/O | VDDIOP | | |
| PA1 | SPI0_MOSI | MCCDA | | I/O | VDDIOP | | |
| PA2 | SPI0_SPCK | MCCK | | I/O | VDDIOP | | |
| PA3 | SPI0_NPCS0 | | | I/O | VDDIOP | | |
| PA4 | SPI0_NPCS1 | MCDA1 | | I/O | VDDIOP | | |
| PA5 | SPI0_NPCS2 | MCDA2 | | I/O | VDDIOP | | |
| PA6 | SPI0_NPCS3 | MCDA3 | | I/O | VDDIOP | | |
| PA7 | TWD | PCK0 | | I/O | VDDIOP | | |
| PA8 | TWCK | PCK1 | | I/O | VDDIOP | | |
| PA9 | DRXD | PCK2 | | I/O | VDDIOP | | |
| PA10 | DTXD | PCK3 | | I/O | VDDIOP | | |
| PA11 | TSYNC | SCK1 | | I/O | VDDIOP | | |
| PA12 | TCLK | RTS1 | | I/O | VDDIOP | | |
| PA13 | TPS0 | CTS1 | | I/O | VDDIOP | | |
| PA14 | TPS1 | SCK2 | | I/O | VDDIOP | | |
| PA15 | TPS2 | RTS2 | | I/O | VDDIOP | | |
| PA16 | TPK0 | CTS2 | | I/O | VDDIOP | | |
| PA17 | TPK1 | TF1 | | I/O | VDDIOP | | |
| PA18 | TPK2 | TK1 | | I/O | VDDIOP | | |
| PA19 | TPK3 | TD1 | | I/O | VDDIOP | | |
| PA20 | TPK4 | RD1 | | I/O | VDDIOP | | |
| PA21 | TPK5 | RK1 | | I/O | VDDIOP | | |
| PA22 | TPK6 | RF1 | | I/O | VDDIOP | | |
| PA23 | TPK7 | RTS0 | | I/O | VDDIOP | | |
| PA24 | TPK8 | SPI1_NPCS1 | | I/O | VDDIOP | | |
| PA25 | TPK9 | SPI1_NPCS2 | | I/O | VDDIOP | | |
| PA26 | TPK10 | SPI1_NPCS3 | | I/O | VDDIOP | | |
| PA27 | TPK11 | SPI0_NPCS1 | | I/O | VDDIOP | | |
| PA28 | TPK12 | SPI0_NPCS2 | | I/O | VDDIOP | | |
| PA29 | TPK13 | SPI0_NPCS3 | | I/O | VDDIOP | | |
| PA30 | TPK14 | A23 | | A23 | VDDIOP | | |
| PA31 | TPK15 | A24 | | A24 | VDDIOP | | |

### 10.3.3 PIO Controller B Multiplexing

**Table 10-3.** Multiplexing on PIO Controller B

| PIO Controller B | | | | | Application Usage | | |
|---|---|---|---|---|---|---|---|
| I/O Line | Peripheral A | Peripheral B | Comments | Reset State | Power Supply | Function | Comments |
| PB0 | LCDVSYNC | | | I/O | VDDIOP | | |
| PB1 | LCDHSYNC | | | I/O | VDDIOP | | |
| PB2 | LCDDOTCK | PCK0 | | I/O | VDDIOP | | |
| PB3[1] | LCDDEN | | See footnote[1] | I/O | VDDIOP | | |
| PB4 | LCDCC | LCDD2 | | I/O | VDDIOP | | |
| PB5 | LCDD0 | LCDD3 | | I/O | VDDIOP | | |
| PB6 | LCDD1 | LCDD4 | | I/O | VDDIOP | | |
| PB7 | LCDD2 | LCDD5 | | I/O | VDDIOP | | |
| PB8 | LCDD3 | LCDD6 | | I/O | VDDIOP | | |
| PB9 | LCDD4 | LCDD7 | | I/O | VDDIOP | | |
| PB10 | LCDD5 | LCDD10 | | I/O | VDDIOP | | |
| PB11 | LCDD6 | LCDD11 | | I/O | VDDIOP | | |
| PB12 | LCDD7 | LCDD12 | | I/O | VDDIOP | | |
| PB13 | LCDD8 | LCDD13 | | I/O | VDDIOP | | |
| PB14 | LCDD9 | LCDD14 | | I/O | VDDIOP | | |
| PB15 | LCDD10 | LCDD15 | | I/O | VDDIOP | | |
| PB16 | LCDD11 | LCDD19 | | I/O | VDDIOP | | |
| PB17 | LCDD12 | LCDD20 | | I/O | VDDIOP | | |
| PB18 | LCDD13 | LCDD21 | | I/O | VDDIOP | | |
| PB19 | LCDD14 | LCDD22 | | I/O | VDDIOP | | |
| PB20 | LCDD15 | LCDD23 | | I/O | VDDIOP | | |
| PB21 | TF0 | LCDD16 | | I/O | VDDIOP | | |
| PB22 | TK0 | LCDD17 | | I/O | VDDIOP | | |
| PB23 | TD0 | LCDD18 | | I/O | VDDIOP | | |
| PB24 | RD0 | LCDD19 | | I/O | VDDIOP | | |
| PB25 | RK0 | LCDD20 | | I/O | VDDIOP | | |
| PB26 | RF0 | LCDD21 | | I/O | VDDIOP | | |
| PB27 | SPI1_NPCS1 | LCDD22 | | I/O | VDDIOP | | |
| PB28 | SPI1_NPCS0 | LCDD23 | | I/O | VDDIOP | | |
| PB29 | SPI1_SPCK | IRQ2 | | I/O | VDDIOP | | |
| PB30 | SPI1_MISO | IRQ1 | | I/O | VDDIOP | | |
| PB31 | SPI1_MOSI | PCK2 | | I/O | VDDIOP | | |

Note: 1. PB3 is multiplexed with BMS signal. Care should be taken during reset time.

### 10.3.4 PIO Controller C Multiplexing

**Table 10-4.** Multiplexing on PIO Controller C

| PIO Controller C | | | | | Application Usage | | |
|---|---|---|---|---|---|---|---|
| I/O Line | Peripheral A | Peripheral B | Comments | Reset State | Power Supply | Function | Comments |
| PC0 | NANDOE | NCS6 | | I/O | VDDIOP | | |
| PC1 | NANDWE | NCS7 | | I/O | VDDIOP | | |
| PC2 | NWAIT | IRQ0 | | I/O | VDDIOP | | |
| PC3 | A25/CFRNW | | | A25 | VDDIOP | | |
| PC4 | NCS4/CFCS0 | | | I/O | VDDIOP | | |
| PC5 | NCS5/CFCS1 | | | I/O | VDDIOP | | |
| PC6 | CFCE1 | | | I/O | VDDIOP | | |
| PC7 | CFCE2 | | | I/O | VDDIOP | | |
| PC8 | TXD0 | PCK2 | | I/O | VDDIOP | | |
| PC9 | RXD0 | PCK3 | | I/O | VDDIOP | | |
| PC10 | RTS0 | SCK0 | | I/O | VDDIOP | | |
| PC11 | CTS0 | FIQ | | I/O | VDDIOP | | |
| PC12 | TXD1 | NCS6 | | I/O | VDDIOP | | |
| PC13 | RXD1 | NCS7 | | I/O | VDDIOP | | |
| PC14 | TXD2 | SPI1_NPCS2 | | I/O | VDDIOP | | |
| PC15 | RXD2 | SPI1_NPCS3 | | I/O | VDDIOP | | |
| PC16 | D16 | TCLK0 | | I/O | VDDIOM | | |
| PC17 | D17 | TCLK1 | | I/O | VDDIOM | | |
| PC18 | D18 | TCLK2 | | I/O | VDDIOM | | |
| PC19 | D19 | TIOA0 | | I/O | VDDIOM | | |
| PC20 | D20 | TIOB0 | | I/O | VDDIOM | | |
| PC21 | D21 | TIOA1 | | I/O | VDDIOM | | |
| PC22 | D22 | TIOB1 | | I/O | VDDIOM | | |
| PC23 | D23 | TIOA2 | | I/O | VDDIOM | | |
| PC24 | D24 | TIOB2 | | I/O | VDDIOM | | |
| PC25 | D25 | TF2 | | I/O | VDDIOM | | |
| PC26 | D26 | TK2 | | I/O | VDDIOM | | |
| PC27 | D27 | TD2 | | I/O | VDDIOM | | |
| PC28 | D28 | RD2 | | I/O | VDDIOM | | |
| PC29 | D29 | RK2 | | I/O | VDDIOM | | |
| PC30 | D30 | RF2 | | I/O | VDDIOM | | |
| PC31 | D31 | PCK1 | | I/O | VDDIOM | | |

### 10.3.5 System Interrupt

The System Interrupt in Source 1 is the wired-OR of the interrupt signals coming from:

- the SDRAM Controller
- the Debug Unit
- the Periodic Interval Timer
- the Real-Time Timer
- the Watchdog Timer
- the Reset Controller
- the Power Management Controller

The clock of these peripherals cannot be deactivated and Peripheral ID 1 can only be used within the Advanced Interrupt Controller.

### 10.3.6 External Interrupts

All external interrupt signals, i.e., the Fast Interrupt signal FIQ or the Interrupt signals IRQ0 to IRQ2, use a dedicated Peripheral ID. However, there is no clock control associated with these peripheral IDs.

## 10.4 External Bus Interface

- Integrates two External Memory Controllers:
  - Static Memory Controller
  - SDRAM Controller
- Additional logic for NAND Flash and CompactFlash support
  - NAND Flash support: 8-bit as well as 16-bit devices are supported
  - CompactFlash support: all modes (Attribute Memory, Common Memory, I/O, True IDE) are supported but the signals -IOIS16 (I/O and True IDE modes) and -ATA SEL (True IDE mode) are not handled.
- Optimized External Bus
  - 16- or 32-bit Data Bus
  - Up to 26-bit Address Bus, up to 64 Mbytes addressable
  - Eight Chip Selects, each reserved to one of the eight Memory Areas
  - Optimized pin multiplexing to reduce latencies on External Memories
- Configurable Chip Select Assignment Managed by EBI_CSA Register located in the MATRIX user interface
  - Static Memory Controller on NCS0
  - SDRAM Controller or Static Memory Controller on NCS1
  - Static Memory Controller on NCS2
  - Static Memory Controller on NCS3, Optional NAND Flash Support
  - Static Memory Controller on NCS4 - NCS5, Optional CompactFlash Support
  - Static Memory Controller on NCS6 - NCS7

## 10.7 Serial Peripheral Interface

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to fifteen peripherals
  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to MCK
  - The chip select line may be left active to speed up transfers on the same device

## 10.8 Two-wire Interface

- Compatibility with standard two-wire serial memory
- One, two or three bytes for slave address
- Sequential read/write operations

## 10.9 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB- or LSB-first
  - Optional break generation and detection
  - By-8 or by-16 over-sampling receiver frequency
  - Hardware handshaking RTS-CTS
  - Receiver time-out and transmitter timeguard
  - Optional Multi-drop Mode with address generation and detection
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps

# 12. Ordering Information

**Table 12-1.** AT91SAM9261 Ordering Information

| Ordering Code | MRL | Package | Package Type | Temperature Operating Range |
|---|---|---|---|---|
| AT91SAM9261-CJ | A | BGA217 | RoHS-compliant | Industrial<br>-40°C to 85°C |
| AT91SAM9261B-CU | B | BGA217 | Green | Industrial<br>-40°C to 85°C |

**Table 13-1.** Revision History (Continued)

| Doc. Rev. | Source | Comments |
|---|---|---|
| **6062KS** | 5846<br><br>5932 | In **Features**, on page 2<br>Debug Unit (DBGU) updated<br>Section 10.9 “USART”, manchester encoding option is not avaiilable. |
| **6062L**  | 5424/rfo | Section 8.1.2.1 “BMS = 1, Boot on Embedded ROM”, updated.<br>**Section 12. “Ordering Information”,**<br>updated with ordering information for chip revision B. |
| | | |