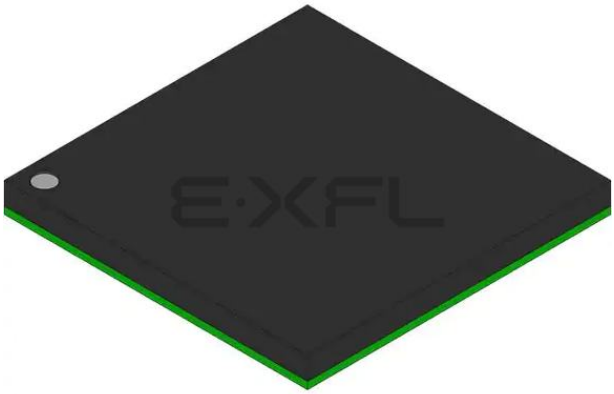

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	AVR
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	EBI/EMI, I²C, Memory Card, PS/2, SPI, SSC, UART/USART, USB
Peripherals	AC'97, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	85
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	D/A 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-TFBGA, CSBGA
Supplier Device Package	196-CTBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at32ap7002-ctut

1. Part Description

The AT32AP7002 is a complete System-on-chip application processor with an AVR32 RISC processor achieving 210 DMIPS running 150 MHz. AVR32 is a high-performance 32-bit RISC microprocessor core, designed for cost-sensitive embedded applications, with particular emphasis on low power consumption, high code density and high application performance.

AT32AP7002 implements a Memory Management Unit (MMU) and a flexible interrupt controller supporting modern operating systems and real-time operating systems. The processor also includes a rich set of DSP and SIMD instructions, specially designed for multimedia and telecom applications.

AT32AP7002 incorporates SRAM memories on-chip for fast and secure access. For applications requiring additional memory, external 16-bit SRAM is accessible. Additionally, an SDRAM controller provides off-chip volatile memory access as well as controllers for all industry standard off-chip non-volatile memories, like Compact Flash, Multi Media Card (MMC), Secure Digital (SD)-card, SmartCard, NAND Flash and Atmel DataFlash™.

The Direct Memory Access controller for all the serial peripherals enables data transfer between memories without processor intervention. This reduces the processor overhead when transferring continuous and large data streams between modules in the MCU.

The Timer/Counters includes three identical 16-bit timer/counter channels. Each channel can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation.

AT32AP7002 also features an onboard LCD Controller, supporting single and double scan monochrome and color passive STN LCD modules and single scan active TFT LCD modules. On monochrome STN displays, up to 16 gray shades are supported using a time-based dithering algorithm and Frame Rate Control (FRC) method. This method is also used in color STN displays to generate up to 4096 colors.

The LCD Controller is programmable for supporting resolutions up to 2048 x 2048 with a pixel depth from 1 to 24 bits per pixel.

A pixel co-processor provides color space conversions for images and video, in addition to a wide variety of hardware filter support

The media-independent interface (MII) and reduced MII (RMII) 10/100 Ethernet MAC modules provides on-chip solutions for network-connected devices.

Synchronous Serial Controllers provide easy access to serial communication protocols, audio standards like I2S and frame-based protocols.

The Java hardware acceleration implementation in AVR32 allows for a very high-speed Java byte-code execution. AVR32 implements Java instructions in hardware, reusing the existing RISC data path, which allows for a near-zero hardware overhead and cost with a very high performance.

The Image Sensor Interface supports cameras with up to 12-bit data buses.

PS2 connectivity is provided for standard input devices like mice and keyboards.

- Configurable coefficients with flexible fixed-point representation.

2.0.3 Debug and Test system

- IEEE1149.1 compliant JTAG and boundary scan
- Direct memory access and programming capabilities through JTAG interface
- Extensive On-Chip Debug features in compliance with IEEE-ISTO 5001-2003 (Nexus 2.0) Class 3
- Auxiliary port for high-speed trace information
- Hardware support for 6 Program and 2 data breakpoints
- Unlimited number of software breakpoints supported
- Advanced Program, Data, Ownership, and Watchpoint trace supported

2.0.4 DMA Controller

- 2 HSB Master Interfaces
- 3 Channels
- Software and Hardware Handshaking Interfaces
  - 11 Hardware Handshaking Interfaces
- Memory/Non-Memory Peripherals to Memory/Non-Memory Peripherals Transfer
- Single-block DMA Transfer
- Multi-block DMA Transfer
  - Linked Lists
  - Auto-Reloading
  - Contiguous Blocks
- DMA Controller is Always the Flow Controller
- Additional Features
  - Scatter and Gather Operations
  - Channel Locking
  - Bus Locking
  - FIFO Mode
  - Pseudo Fly-by Operation

2.0.5 Peripheral DMA Controller

- Transfers from/to peripheral to/from any memory space without intervention of the processor.
- Next Pointer Support, forbids strong real-time constraints on buffer management.
- Eighteen channels
  - Two for each USART
  - Two for each Serial Synchronous Controller
  - Two for each Serial Peripheral Interface

2.0.6 Bus system

- HSB bus matrix with 10 Masters and 8 Slaves handled
  - Handles Requests from the CPU Icache, CPU Dcache, HSB bridge, HISI, USB 2.0 Controller, LCD Controller, DMA Controller 0, DMA Controller 1, and to internal SRAM 0, internal SRAM 1, PB A, PB B, EBI and, USB.

2.1 Package and PinoutAVR32AP7002

Figure 2-2. 196 CTBGA Pinout

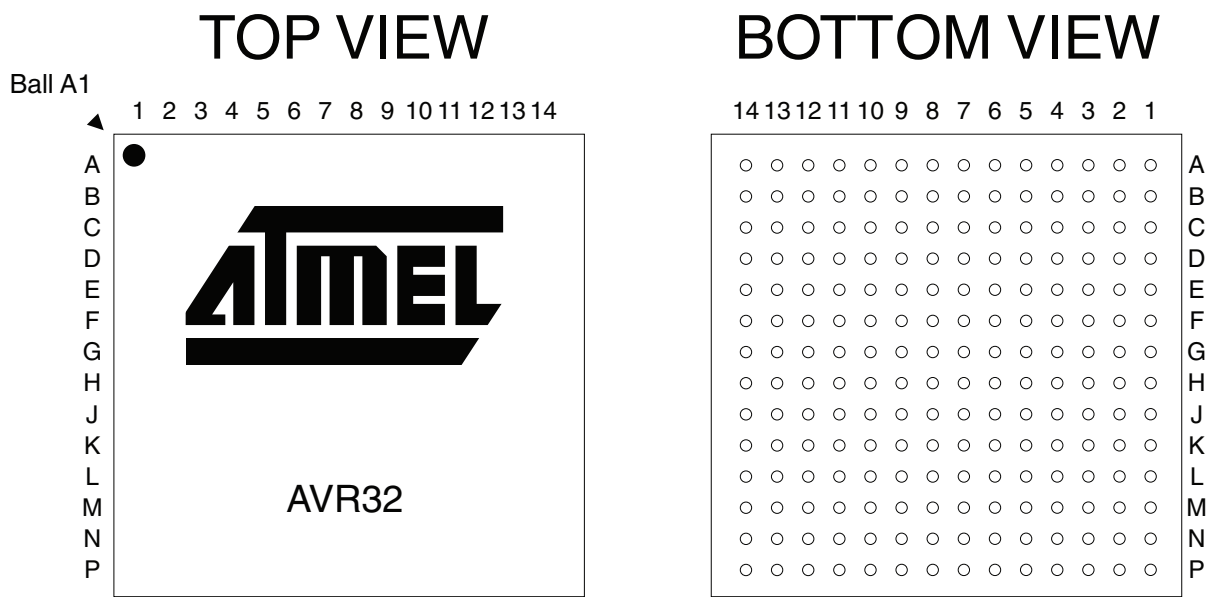

Table 2-1. CTBGA196 Package Pinout A1..T8

	1	2	3	4	5	6	7	8
A	PX49	PX48	PX47	AVDDPLL	PC28	PC23	PC20	PB22
B	PX50	GND	VDDIO	PLL0	PLL1	XIN32	PC22	PB23
C	PX51	PD01	PX05	GND	AGNDPLL	XOUT32	PC29	PC21
D	PX32	PD00	VDDIO	PX02	XIN0	XOUT0	AGNDOSC	PC30
E	PX33	PX00	PX04	GND	PD07	AVDDOSC	OSCEN_N	PC31
F	PX01	PX03	VDDCORE	PD04	PD09	TDI	RESET_N	VDDCORE
G	PD05	PD08	PD06	TDO	PA04	PA02	PA08	PX22
H	TMS	TRST_N	TCK	EVTI_N	PB24	PA10	PA14	PX38
J	PA01	PA03	PA00	VDDIO	GND	PA09	PA18	GND
K	PA05	PA11	PA12	PA16	GND	GND	PA26	WAKE_N
L	PB25	PA21	PA19	GND	VDDIO	VDDIO	PA25	PA29
M	PA13	PA22	PA23	PD17	AVDDUSB	VDDCORE	VBG	PA30
N	PA15	PA20	PD12	PD15	PD16	AGNDUSB	FSDP	HSDP
P	PA17	PA24	PD13	PD14	XIN1	XOUT1	FSDM	HSDM

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
EVTO_N	Event Out	Output	Low	
Power Manager - PM				
GCLK0 - GCLK4	Generic Clock Pins	Output		
OSCEN_N	Oscillator Enable	Input	Low	
RESET_N	Reset Pin	Input	Low	
WAKE_N	Wake Pin	Input	Low	
External Interrupt Controller - EIC				
EXTINT0 - EXTINT3	External Interrupt Pins	Input		
NMI_N	Non-Maskable Interrupt Pin	Input	Low	
AC97 Controller - AC97C				
SCLK	AC97 Clock Signal	Input		
SDI	AC97 Receive Signal	Output		
SDO	AC97 Transmit Signal	Output		
SYNC	AC97 Frame Synchronization Signal	Input		
Audio Bitstream DAC - ABDAC				
DATA0 - DATA1	D/A Data Out	Output		
DATAN0 - DATAN1	D/A Inverted Data Out	Output		
External Bus Interface - EBI				
PX0 - PX53	I/O Controlled by EBI	I/O		
ADDR0 - ADDR25	Address Bus	Output		
CAS	Column Signal	Output	Low	
CFCE1	Compact Flash 1 Chip Enable	Output	Low	
CFCE2	Compact Flash 2 Chip Enable	Output	Low	
CFRNW	Compact Flash Read Not Write	Output		
DATA0 - DATA31	Data Bus	I/O		
NANDOE	NAND Flash Output Enable	Output	Low	
NANDWE	NAND Flash Write Enable	Output	Low	
NCS0 - NCS5	Chip Select	Output	Low	

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
NRD	Read Signal	Output	Low	
NWAIT	External Wait Signal	Input	Low	
NWE0	Write Enable 0	Output	Low	
NWE1	Write Enable 1	Output	Low	
NWE3	Write Enable 3	Output	Low	
RAS	Row Signal	Output	Low	
SDA10	SDRAM Address 10 Line	Output		
SDCK	SDRAM Clock	Output		
SDCKE	SDRAM Clock Enable	Output		
SDWE	SDRAM Write Enable	Output	Low	
Image Sensor Interface - ISI				
DATA0 - DATA11	Image Sensor Data	Input		
HSYNC	Horizontal Synchronization	Input		
PCLK	Image Sensor Data Clock	Input		
VSYNC	Vertical Synchronization	Input		
LCD Controller - LCDC				
CC	LCD Contrast Control	Output		
DATA0 - DATA23	LCD Data Bus	Input		
DVAL	LCD Data Valid	Output		
GPL0 - GPL7	LCD General Purpose Lines	Output		
HSYNC	LCD Horizontal Synchronization	Output		
MODE	LCD Mode	Output		
PCLK	LCD Clock	Output		
PWR	LCD Power	Output		
VSYNC	LCD Vertical Synchronization	Output		
MultiMedia Card Interface - MCI				
CLK	Multimedia Card Clock	Output		
CMD0 - CMD1	Multimedia Card Command	I/O		

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
DATA0 - DATA7	Multimedia Card Data	I/O		
Parallel Input/Output - PIOA, PIOB, PIOC, PIOD				
PA0 - PA31	Parallel I/O Controller PIOA	I/O		
PB0 - PB30	Parallel I/O Controller PIOB	I/O		
PC20 - PC23/ PC28 - PC31	Parallel I/O Controller PIOC	I/O		
PD0 - PD17	Parallel I/O Controller PIOD	I/O		
PS2 Interface - PSIF				
CLOCK0 - CLOCK1	PS2 Clock	Input		
DATA0 - DATA1	PS2 Data	I/O		
Serial Peripheral Interface - SPI0, SPI1				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
NPCS0 - NPCS3	SPI Peripheral Chip Select	I/O	Low	
SCK	Clock	Output		
Synchronous Serial Controller - SSC0, SSC1, SSC2				
RX_CLOCK	SSC Receive Clock	I/O		
RX_DATA	SSC Receive Data	Input		
RX_FRAME_SYNC	SSC Receive Frame Sync	I/O		
TX_CLOCK	SSC Transmit Clock	I/O		
TX_DATA	SSC Transmit Data	Output		
TX_FRAME_SYNC	SSC Transmit Frame Sync	I/O		
DMA Controller - DMACA				
DMARQ0 - DMARQ3	DMA Requests	Input		
Timer/Counter - TIMER0, TIMER1				
A0	Channel 0 Line A	I/O		
A1	Channel 1 Line A	I/O		
A2	Channel 2 Line A	I/O		
B0	Channel 0 Line B	I/O		

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
B1	Channel 1 Line B	I/O		
B2	Channel 2 Line B	I/O		
CLK0	Channel 0 External Clock Input	Input		
CLK1	Channel 1 External Clock Input	Input		
CLK2	Channel 2 External Clock Input	Input		
Two-wire Interface - TWI				
SCL	Serial Clock	I/O		
SDA	Serial Data	I/O		
Universal Synchronous Asynchronous Receiver Transmitter - USART0, USART1, USART2, USART3				
CLK	Clock	I/O		
CTS	Clear To Send	Input		
RTS	Request To Send	Output		
RXD	Receive Data	Input		
TXD	Transmit Data	Output		
Pulse Width Modulator - PWM				
PWM0 - PWM3	PWM Output Pins	Output		
USB Interface - USBA				
HSDM	High Speed USB Interface Data -	Analog		
FSDM	Full Speed USB Interface Data -	Analog		
HSDP	High Speed USB Interface Data +	Analog		
FSDP	Full Speed USB Interface Data +	Analog		
VBG	USB bandgap	Analog		Connected to a 6810 Ohm ± 0.5% resistor to gound and a 10 pF capacitor to ground.

5. I/O Line Considerations

5.1 JTAG pins

The TMS, TDI and TCK pins have pull-up resistors. TDO is an output, driven at up to VDDIO, and have no pull-up resistor. The TRST_N pin is used to initialize the embedded JTAG TAP Controller when asserted at a low level. It is a schmitt input and integrates permanent pull-up resistor to VDDIO, so that it can be left unconnected for normal operations.

5.2 WAKE_N pin

The WAKE_N pin is a schmitt trigger input integrating a permanent pull-up resistor to VDDIO.

5.3 RESET_N pin

The RESET_N pin is a schmitt input and integrates a permanent pull-up resistor to VDDIO. As the product integrates a power-on reset cell, the RESET_N pin can be left unconnected in case no reset from the system needs to be applied to the product.

5.4 EVTI_N pin

The EVTI_N pin is a schmitt input and integrates a non-programmable pull-up resistor to VDDIO.

5.5 TWI pins

When these pins are used for TWI, the pins are open-drain outputs with slew-rate limitation and inputs with inputs with spike-filtering. When used as GPIO-pins or used for other peripherals, the pins have the same characteristics as PIO pins.

5.6 PIO pins

All the I/O lines integrate a programmable pull-up resistor. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers. After reset, I/O lines default as inputs with pull-up resistors enabled, except when indicated otherwise in the column “Reset State” of the PIO Controller multiplexing tables.

Table 6-2. HSB masters

Master 0	CPU Dcache
Master 1	CPU Icache
Master 2	HSB-HSB Bridge
Master 3	ISI DMA
Master 4	USBA DMA
Master 5	LCD Controller DMA
Master 8	DMAC Master Interface 0
Master 9	DMAC Master Interface 1

Each slave has its own arbiter, thus allowing a different arbitration per slave. The slave number in the table below can be used to index the HMATRIX control registers. For example, SCFG3 is associated with PBB.

Table 6-3. HSB slaves

Slave 0	Internal SRAM 0
Slave 1	Internal SRAM1
Slave 2	PBA
Slave 3	PBB
Slave 4	EBI
Slave 5	USBA data
Slave 6	LCDC configuration
Slave 7	DMACA configuration

Table 7-1. Peripheral Address Mapping (Continued)

Address		Peripheral Name	Bus
0xFFE03800	PIOE	Parallel Input/Output 2 - PIOE	PB A
0xFFE03C00	PSIF	PS2 Interface - PSIF	PB A
0xFFF00000	PM	Power Manager - PM	PB B
0xFFF00080	RTC	Real Time Counter- RTC	PB B
0xFFF000B0	WDT	WatchDog Timer- WDT	PB B
0xFFF00100	EIC	External Interrupt Controller - EIC	PB B
0xFFF00400	INTC	Interrupt Controller - INTC	PB B
0xFFF00800	HMATRIX	HSB Matrix - HMATRIX	PB B
0xFFF00C00	TC0	Timer/Counter - TC0	PB B
0xFFF01000	TC1	Timer/Counter - TC1	PB B
0xFFF01400	PWM	Pulse Width Modulation Controller - PWM	PB B
0xFFF02000	ABDAC	Audio Bitstream DAC - ABDAC	PB B
0xFFF02400	MCI	MultiMedia Card Interface - MCI	PB B
0xFFF02800	AC97C	AC97 Controller - AC97C	PB B
0xFFF02C00	ISI	Image Sensor Interface - ISI	PB B
0xFFF03000	USBA	USB Configuration Interface - USBA	PB B
0xFFF03400	SMC	Static Memory Controller - SMC	PB B
0xFFF03800	SDRAMC	SDRAM Controller - SDRAMC	PB B
0xFFF03C00	ECC	Error Correcting Code Controller - ECC	PB B

7.4 Clock Connections

7.4.1 Timer/Counters

Each Timer/Counter channel can independently select an internal or external clock source for its counter:

Table 7-4. Timer/Counter clock connections

Timer/Counter	Source	Name	Connection
0	Internal	TIMER_CLOCK1	clk_osc32
		TIMER_CLOCK2	clk_pbb / 4
		TIMER_CLOCK3	clk_pbb / 8
		TIMER_CLOCK4	clk_pbb / 16
		TIMER_CLOCK5	clk_pbb / 32
	External	XC0	See Section 7.7
		XC1	
		XC2	
1	Internal	TIMER_CLOCK1	clk_osc32
		TIMER_CLOCK2	clk_pbb / 4
		TIMER_CLOCK3	clk_pbb / 8
		TIMER_CLOCK4	clk_pbb / 16
		TIMER_CLOCK5	clk_pbb / 32
	External	XC0	See Section 7.7
		XC1	
		XC2	

7.4.2 USARTs

Each USART can be connected to an internally divided clock:

Table 7-5. USART clock connections

USART	Source	Name	Connection
0	Internal	CLK_DIV	clk_pba / 8
1			
2			
3			

7.7 Peripheral Multiplexing on IO lines

The AT32AP7002 features five PIO controllers, PIOA to PIOE, that multiplex the I/O lines of the peripheral set. Each PIO Controller controls up to thirty-two lines.

Each line can be assigned to one of two peripheral functions, A or B. The tables in the following pages define how the I/O lines of the peripherals A and B are multiplexed on the PIO Controllers.

Note that some output only peripheral functions might be duplicated within the tables.

7.7.1 PIO Controller A Multiplexing

Table 7-9. PIO Controller A Multiplexing

CTBGA196	I/O Line	Peripheral A	Peripheral B
J3	PA00	SPI0 - MISO	SSC1 - RX_FRAME_SYNC
J1	PA01	SPI0 - MOSI	SSC1 - TX_FRAME_SYNC
G6	PA02	SPI0 - SCK	SSC1 - TX_CLOCK
J2	PA03	SPI0 - NPCS[0]	SSC1 - RX_CLOCK
G5	PA04	SPI0 - NPCS[1]	SSC1 - TX_DATA
K1	PA05	SPI0 - NPCS[2]	SSC1 - RX_DATA
C9	PA06	TWI - SDA	USART0 - RTS
E9	PA07	TWI - SCL	USART0 - CTS
G7	PA08	PSIF - CLOCK	USART0 - RXD
J6	PA09	PSIF - DATA	USART0 - TXD
H6	PA10	MCI - CLK	USART0 - CLK
K2	PA11	MCI - CMD	TC0 - CLK0
K3	PA12	MCI - DATA[0]	TC0 - A0
M1	PA13	MCI - DATA[1]	TC0 - A1
H7	PA14	MCI - DATA[2]	TC0 - A2
N1	PA15	MCI - DATA[3]	TC0 - B0
K4	PA16	USART1 - CLK	TC0 - B1
P1	PA17	USART1 - RXD	TC0 - B2
J7	PA18	USART1 - TXD	TC0 - CLK2
L3	PA19	USART1 - RTS	TC0 - CLK1
N2	PA20	USART1 - CTS	SPI0 - NPCS[3]
L2	PA21	SSC0 - RX_FRAME_SYNC	PWM - PWM[2]
M2	PA22	SSC0 - RX_CLOCK	PWM - PWM[3]
M3	PA23	SSC0 - TX_CLOCK	TC1 - A0
P2	PA24	SSC0 - TX_FRAME_SYNC	TC1 - A1
L7	PA25	SSC0 - TX_DATA	TC1 - B0
K7	PA26	SSC0 - RX_DATA	TC1 - B1
P9	PA27	SPI1 - NPCS[3]	TC1 - CLK0
H9	PA28	PWM - PWM[0]	TC1 - A2

7.7.5 IO Pins Without Multiplexing

Many of the external EBI pins are not controlled by the PIO modules, but directly driven by the EBI. These pins have programmable pullup resistors. These resistors are controlled by Special Function Register 4 (SFR4) in the HMATRIX. The pullup on the lines multiplexed with PIO is controlled by the appropriate PIO control register.

This SFR can also control CompactFlash, SmartMedia or NandFlash Support, see the EBI chapter for details

7.7.5.1 HMatrix SFR4 EBI Control Register

Name: HMATRIX_SFR4

Access Type: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	EBI_DBPUC
7	6	5	4	3	2	1	0
–	–	EBI_CS5A	EBI_CS4A	EBI_CS3A	–	EBI_CS1A	-

- **CS1A: Chip Select 1 Assignment**

0 = Chip Select 1 is assigned to the Static Memory Controller.

1 = Chip Select 1 is assigned to the SDRAM Controller.

- **CS3A: Chip Select 3 Assignment**

0 = Chip Select 3 is only assigned to the Static Memory Controller and NCS3 behaves as defined by the SMC.

1 = Chip Select 3 is assigned to the Static Memory Controller and the NAND Flash/SmartMedia Logic is activated.

- **CS4A: Chip Select 4 Assignment**

0 = Chip Select 4 is assigned to the Static Memory Controller and NCS4, NCS5 and NCS6 behave as defined by the SMC.

1 = Chip Select 4 is assigned to the Static Memory Controller and the CompactFlash Logic is activated.

- **CS5A: Chip Select 5 Assignment**

0 = Chip Select 5 is assigned to the Static Memory Controller and NCS4, NCS5 and NCS6 behave as defined by the SMC.

1 = Chip Select 5 is assigned to the Static Memory Controller and the CompactFlash Logic is activated.

7.8.7 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB- or LSB-first
  - Optional break generation and detection
  - By 8 or by-16 over-sampling receiver frequency
  - Hardware handshaking RTS-CTS
  - Receiver time-out and transmitter timeguard
  - Optional Multi-drop Mode with address generation and detection
  - Optional Manchester Encoding
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes 46
  - Remote Loopback, Local Loopback, Automatic Echo

7.8.8 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I2S, TDM Buses, Magnetic Card Reader, etc.)
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

7.8.9 AC97 Controller

- Compatible with AC97 Component Specification V2.2
- Capable to Interface with a Single Analog Front end
- Three independent RX Channels and three independent TX Channels
  - One RX and one TX channel dedicated to the AC97 Analog Front end control
  - One RX and one TX channel for data transfers, connected to the DMACA
  - One RX and one TX channel for data transfers, connected to the DMACA
- Time Slot Assigner allowing to assign up to 12 time slots to a channel
- Channels support mono or stereo up to 20 bit sample length - Variable sampling rate AC97 Codec Interface (48KHz and below)

7.8.13 MultiMedia Card Interface

- 2 double-channel MultiMedia Card Interface, allowing concurrent transfers with 2 cards
- Compatibility with MultiMedia Card Specification Version 2.2
- Compatibility with SD Memory Card Specification Version 1.0
- Compatibility with SDIO Specification Version V1.0.
- Cards clock rate up to Master Clock divided by 2
- Embedded power management to slow down clock rate when not used
- Each MCI has two slot, each supporting
  - One slot for one MultiMediaCard bus (up to 30 cards) or
  - One SD Memory Card
- Support for stream, block and multi-block data read and write

7.8.14 PS/2 Interface

- Peripheral Bus slave
- PS/2 Host
- Receive and transmit capability
- Parity generation and error detection
- Overrun error detection

7.8.15 USB Interface

- Supports Hi (480Mbps) and Full (12Mbps) speed communication
- Compatible with the USB 2.0 specification
- UTMI Compliant
- 7 Endpoints
- Embedded Dual-port RAM for Endpoints
- Suspend/Resume Logic (Command of UTMI)
- Up to Three Memory Banks for Endpoints (Not for Control Endpoint)
- 4 KBytes of DPRAM

7.8.16 LCD Controller

- Single and Dual scan color and monochrome passive STN LCD panels supported
- Single scan active TFT LCD panels supported
- 4-bit single scan, 8-bit single or dual scan, 16-bit dual scan STN interfaces supported
- Up to 24-bit single scan TFT interfaces supported
- Up to 16 gray levels for mono STN and up to 4096 colors for color STN displays
- 1, 2 bits per pixel (palletized), 4 bits per pixel (non-palletized) for mono STN
- 1, 2, 4, 8 bits per pixel (palletized), 16 bits per pixel (non-palletized) for color STN
- 1, 2, 4, 8 bits per pixel (palletized), 16, 24 bits per pixel (non-palletized) for TFT
- Single clock domain architecture
- Resolution supported up to 2048x2048
- 2D-DMA Controller for management of virtual Frame Buffer
  - Allows management of frame buffer larger than the screen size and moving the view over this virtual frame buffer
- Automatic resynchronization of the frame buffer pointer to prevent flickering
- Configurable coefficients with flexible fixed-point representation.

10. Errata

10.1 Rev. C

1. **SPI FDIV option does not work**
   Selecting clock signal using FDIV = 1 does not work as specified.

   Fix/Workaround
   Do not set FDIV = 1.

2. **SPI Chip Select 0 BITS field overrides other Chip Selects**
   The BITS field for Chip Select 0 overrides BITS fields for other Chip selects.

   Fix/Workaround
   Update Chip Select 0 BITS field to the relevant settings before transmitting with Chip Selects other than 0.

3. **SPI LASTXFER may be overwritten**
   When Peripheral Select (PS) = 0, the LASTXFER-bit in the Transmit Data Register (TDR) should be internally discared. This fails and may cause problems during DMA transfers. Transmitting data using the PDC when PS=0, the size of the transferred data is 8- or 16-bits. The upper 16 bits of the TDR will be written to a random value. If Chip Select Active After Transfer (CSAAT) = 1, the behavior of the Chip Select will be unpredictable.

   Fix/Workaround
   - Do not use CSAAT = 1 if PS = 0

   - Use GPIO to control Chip Select lines

   - Select PS=1 and store data for PCS and LASTXFER for each data in transmit buffer.

4. **SPI LASTXFER overrides Chip Select**
   The LASTXFER bit overrides Chip Select input when PS = 0 and CSAAT is used.

   Fix/Workaround
   - Do not use the CSAAT

   - Use GPIO as Chip Select input

   - Select PS = 1. Transfer 32-bit with correct LASTXFER settings.

5. **MMC data write operation with less than 12 bytes is impossible.**
   MCI data write operation with less than 12 bytes is impossible. The Data Write operation with a number of bytes less than 12 leaves the internal MCI FIFO in an inconsistent state. Subsequent reads and writes will not function properly.

   Fix/Workaround
   Always transfer 12 or more bytes at a time. If less than 12 bytes are transferred, the only recovery mechanism is to perform a software reset of the MCI.

6. **MMC SDIO interrupt only works for slot A**
   If 1-bit data bus width and on other slots than slot A, the SDIO interrupt can not be captured.

Fix/Workaround

Use slot A.

7. **PSIF TXEN/RXEN may disable the transmitter/receiver**

   Writing a '0' to RXEN will disable the receiver. Writing '0' to TXEN will disable the transmitter.

   Fix/Workaround

   When accessing the PS/2 Control Register always write '1' to RXEN to keep the receiver enabled, and write '1' to TXEN to keep the transmitter enabled.

8. **PSIF TXRDY interrupt corrupts transfers**

   When writing to the Transmit Holding Register (THR), the data will be transferred to the data shift register immediately, regardless of the state of the data shift register. If a transfer is ongoing, it will be interrupted and a new transfer will be started with the new data written to THR.

   Fix/Workaround

   Use the TXEMPTY-interrupt instead of the TXRDY-interrupt to update the THR. This ensures that a transfer is completed.

9. **LCD memory error interupt does not work**

   Writing to the MERIT-bit in the LCD Interrupt Test Register (ITR) does not cause an interrupt as intended. The MERIC-bit in the LCD Interrupt Clear Register (ICR) cannot be written. This means that if the MERIS-bit in ISR is set, it cannot be cleared.

   Fix/Workaround

   Memory error interrupt should not be used.

10. **PWM counter restarts at 0x0001**

    The PWM counter restarts at 0x0001 and not 0x0000 as specified. Because of this the first PWM period has one more clock cycle.

    Fix/Workaround

    - The first period is 0x0000, 0x0001, ..., period

    - Consecutive periods are 0x0001, 0x0002, ..., period

11. **PWM channel interrupt enabling triggers an interrupt**

    When enabling a PWM channel that is configured with center aligned period (CALG=1), an interrupt is signalled.

    Fix/Workaround

    When using center aligned mode, enable the channel and read the status before channel interrupt is enabled.

12. **PWM update period to a 0 value does not work**

    It is impossible to update a period equal to 0 by the using the PWM update register (PWM_CUPD).

    Fix/Workaround

    Do not update the PWM_CUPD register with a value equal to 0.

13. **PWM channel status may be wrong if disabled before a period has elapsed**

TCMR.START = Receive start

RFMR.FSOS = None (Input)

RCMR.START = any on RF (edge/level)

Fix/Workaround

None.

30. **USART - TXD signal is floating in Modem and Hardware Handshaking mode**

The TXD signal is floating in Modem and Hardware Handshaking mode, but should be pulled up.

Fix/Workaround

Enable pullup on this line in the PIO.

31. **PWM - Impossible to update a period equal to 0 by using the CUPD register**

It is impossible to UPDATE a period equal to 0 by the using of the UPDATE register (CUPD).

Fix/Workaround

To update a period equal to 0, write directly to the CPRD register.

32. **WDT Clear is blocked after WDT Reset**

A watchdog timer event will, after reset, block writes to the WDT_CLEAR register, preventing the program to clear the next Watchdog Timer Reset.

Fix/Workaround

If the RTC is not used a write to AVR32_RTC.ctrl.pclr = 1, instead of writing to AVR32_WDT.clr, will reset the prescaler and thus prevent the watchdog event from happening. This will render the RTC useless, but prevents WDT reset because the RTC and WDT share the same prescaler. Another sideeffect of this is that the watchdog timeout period will be half the expected timeout period.

If the RTC is used one can disable the Watchdog Timer (WDT) after a WDT reset has occured. This will prevent the WDT resetting the system. To make the WDT functional again a hard reset (power on reset or RESET_N) must be applied. If you still want to use the WDT after a WDT reset a small code can be inserted at the startup checking the AVR32_PM.rcause register for WDT reset and use a GPIO pin to reset the system. This method requires that one of the GPIO pins are available and connected externally to the RESET_N pin. After the GPIO pin has pulled down the reset line the GPIO will be reset and leave the pin tristated with pullup.

33. **USART - The DCD Signal is active high from the USART, but should be active low**

The DCD signal is active high from the USART, but should be active low.

Fix/Workaround

An inverter should be added on this line on the PCB.

34. **MCI Transmit Data Register (TDR) FIFO corruption**

If the number of bytes to be transmitted by the MCI is not a multiple of 4, the Transmit Data Register (TDR) First In First Out data buffer control logic will become corrupted when transmit data is written to the TDR as 32-bit values.

Fix/Workaround

20. Added debug operation to product dependencies in ”Pulse Width Modulation Controller (PWM)” on page 774.
21. Consistently used the term LCDC Core Clock through the document when referring to the generic clock that drives the LCD Core and is used to generate PCLK and the other LCD synchronization signals.
22. Updated typos in ”LCD Controller (LCDC)” on page 800.
23. Rewritten the Register Configuration Guide and renamed it “Register Configuration Example“ in ”LCD Controller (LCDC)” on page 800.
24. Updated formula for pixel clock in ”LCD Control Register 1” on page 840.
25. Updated HOZVAL description in ”LCD Frame Configuration Register” on page 845.
26. Updated ”PLL Characteristics” on page 933.
27. Updated ”Errata” on page 40.

11.4 Rev. C 07/07

1. Updated ”Part Description” on page 2.
2. PC Signals removed in ”Signals Description” on page 5
3. USB Signals updated in ”Signals Description” on page 5.
4. The PX0 - PX53 Signals added in ”Signals Description” on page 5.
5. SDCS signals removed from PIO Controller Multiplexing tables in ”Peripherals” on page 79.
6. MAC references removed form tables in ”Memories” on page 77.
7. MAC controller references removed in ”Peripheral overview” on page 94.
8. SDCS1 signal removed from figures and tables, and SDCS0 renamed to SDCS in ”External Bus Interface (EBI)” on page 147.
9. SmartMedia renamed to NAND Flash in some description to avoid confusion in ”External Bus Interface (EBI)” on page 147.
10. Updated Application block diagram in Figure 1-2 on page 1.
11. Updated the reset state of the SMC Mode register in Table 27-9 on page 523.
12. Updated ”Mechanical Characteristics” on page 927.
13. Updated pad parameters in ”DC Characteristics” on page 928.
14. Updated ”Power Consumption by Peripheral in Active Mode” on page 930, LCD and MACB excluded.
15. Updated pad parameters in ”Clock Characteristics” on page 931.
16. Updated ”USB Transceiver Characteristics” on page 934.
17. Updated ”EBI Timings” on page 939.

11.5 Rev. B 04/07

1. Updated ”Features” on page 1.
2. Updated tables in ”Signals Description” on page 4.
3. Updated Table 9-2 on page 77, Table 9-9 on page 82, and Table 9-10 on page 83 in the ”Peripherals” on page 75.
4. Updated module names and abbreviations through the datasheet.

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