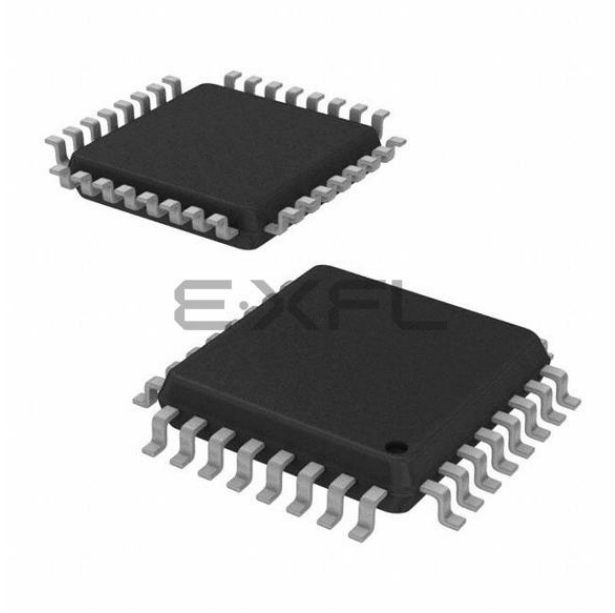

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Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	LINbus, SCI, SPI
Peripherals	POR, PWM
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908ey16acfje

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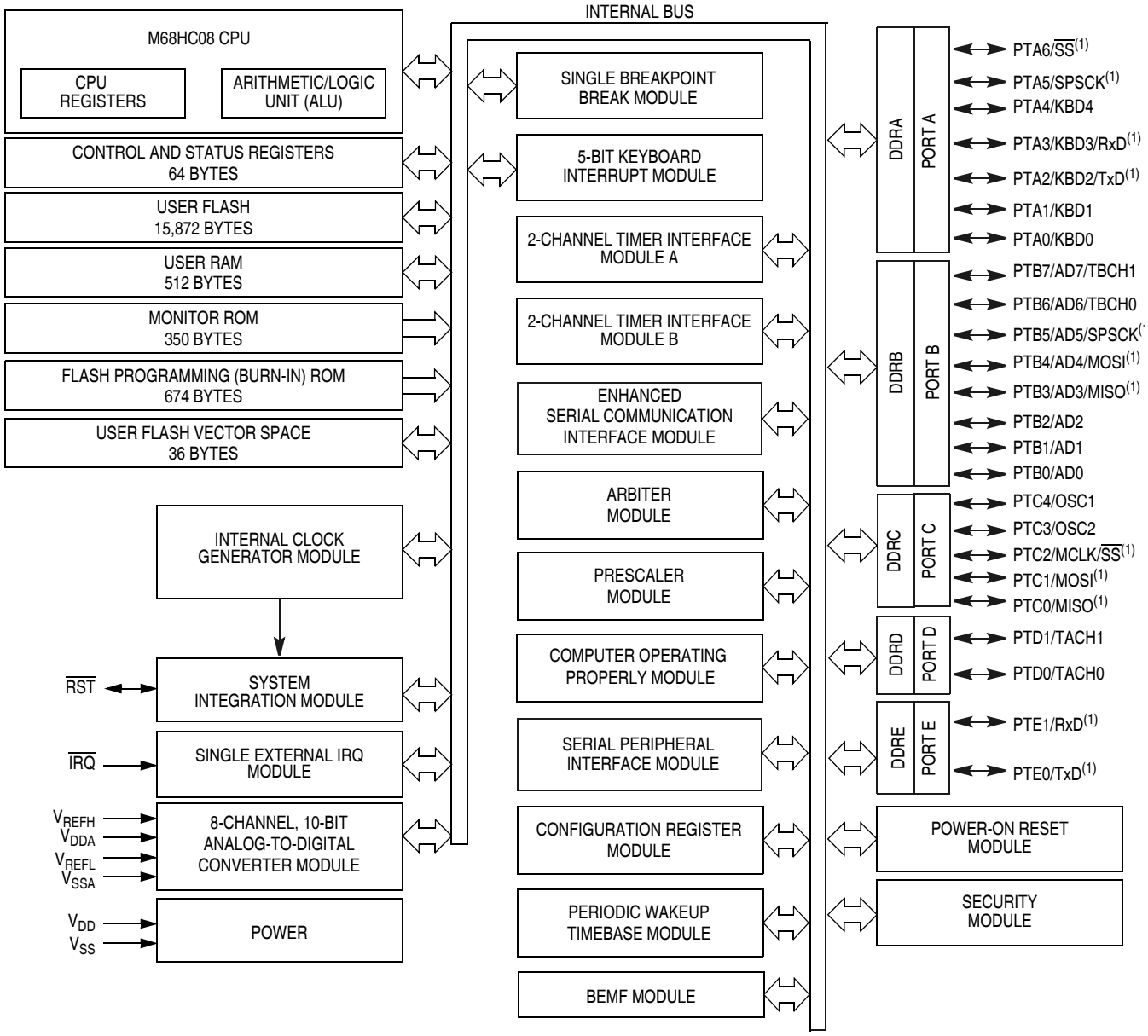


NOTE:
1. The locations of the ESCI and SPI pins are user selectable using CONFIG3 option bits.

Figure 1-1. MCU Block Diagram

Chapter 3
Analog-to-Digital Converter (ADC10) Module

3.1 Introduction

This section describes the 10-bit successive approximation analog-to-digital converter (ADC10).

The ADC10 module shares its pins with general-purpose input/output (I/O) port pins. See Figure 3-1 for port location of these shared pins. The ADC10 on this MCU uses V_{DDA} and V_{SSA} as its supply pins and V_{REFH} and V_{REFL} as its reference pins. This MCU uses CGMXCLK as its alternate clock source for the ADC. This MCU does not have a hardware conversion trigger.

3.2 Features

Features of the ADC10 module include:

- Linear successive approximation algorithm with 10-bit resolution
- Output formatted in 10- or 8-bit right-justified format
- Single or continuous conversion (automatic power-down in single conversion mode)
- Configurable sample time and conversion speed (to save power)
- Conversion complete flag and interrupt
- Input clock selectable from up to three sources
- Operation in wait and stop modes for lower noise operation

3.3 Functional Description

The ADC10 uses successive approximation to convert the input sample taken from ADVIN to a digital representation. The approximation is taken and then rounded to the nearest 10- or 8-bit value to provide greater accuracy and to provide a more robust mechanism for achieving the ideal code-transition voltage.

Figure 3-2 shows a block diagram of the ADC10.

For proper conversion, the voltage on ADVIN must fall between V_{REFH} and V_{REFL}. If ADVIN is equal to or exceeds V_{REFH}, the converter circuit converts the signal to $3FF for a 10-bit representation or $FF for a 8-bit representation. If ADVIN is equal to or less than V_{REFL}, the converter circuit converts it to $000. Input voltages between V_{REFH} and V_{REFL} are straight-line linear conversions.

NOTE

Input voltage must not exceed the analog supply voltages.

EXTXTALEN, when set, also configures the external clock stabilization divider in the clock monitor for a 4096-cycle timeout to allow the proper stabilization time for a crystal. When EXTXTALEN is clear, the stabilization divider is configured to 16 cycles since an external clock source does not need a startup time.

1 = Allows PTC3/OSC2 to be an external crystal connection.
0 = PTC3/OSC2 functions as an I/O port pin (default).

EXTSLOW — Slow External Crystal Enable Bit

The EXTSLOW bit has two functions. It configures the ICG module for a fast (1 MHz to 32 MHz) or slow (30 kHz to 100 kHz) speed crystal. The option also configures the clock monitor operation in the ICG module to expect an external frequency higher (307.2 kHz to 32 MHz) or lower (60 Hz to 307.2 kHz) than the base frequency of the internal oscillator. See Chapter 8 Internal Clock Generator (ICG) Module.

1 = ICG set for slow external crystal operation
0 = ICG set for fast external crystal operation

Table 5-1. External Clock Option Settings

External Clock Configuration Bits		Pin Function		Description
EXTCLKEN	EXTXTALEN	PTC4/OSC1	PTC3/OSC2	
0	0	PTC4	PTC3	Default setting — external oscillator disabled
0	1	PTC4	PTC3	External oscillator disabled since EXTCLKEN not set
1	0	OSC1	PTC3	External oscillator configured for an external clock source input (square wave) on OSC1
1	1	OSC1	OSC2	External oscillator configured for an external crystal configuration on OSC1 and OSC2. System will also operate with square-wave clock source in OSC1.

EXTCLKEN — External Clock Enable Bit

EXTCLKEN enables an external clock source or crystal/ceramic resonator to be used as a clock input. Setting this bit enables PTC4/OSC1 pin to be a clock input pin. Clearing this bit (default setting) allows the PTC4/OSC1 and PTC3/OSC2 pins to function as general-purpose input/output (I/O) pins. Refer to Table 5-1 for configuration options for the external source. See Chapter 8 Internal Clock Generator (ICG) Module for a more detailed description of the external clock operation.

1 = Allows PTC4/OSC1 to be an external clock connection
0 = PTC4/OSC1 and PTC3/OSC2 function as I/O port pins (default).

TMBCLKSEL — Timebase Clock Select Bit

TMBCLKSEL enables an enable the extra divide by 128 prescaler in the timebase module. Setting this bit enables the extra prescaler and clearing this bit disables it. Refer to Table 16-1 for timebase divider selection details.

1 = Enables extra divide by 128 prescaler in timebase module.
0 = Disables extra divide by 128 prescaler in timebase module.

8.4.4.1 Digitally Controlled Oscillator

The digitally controlled oscillator (DCO) is an inaccurate oscillator which generates the internal clock (ICLK), whose clock period is dependent on the digital loop filter outputs (DSTG[7:0] and DDIV[3:0]). Because of the digital nature of the DCO, the clock period of ICLK will change in quantized steps. This will create a clock period difference or quantization error (Q-ERR) from one cycle to the next. Over several cycles or for longer periods, this error is divided out until it reaches a minimum error of 0.202 percent to 0.368 percent. The dependence of this error on the DDIV[3:0] value and the number of cycles the error is measured over is shown in Table 8-2.

8.4.4.2 Binary Weighted Divider

The binary weighted divider divides the output of the ring oscillator by a power of two, specified by the DCO divider control bits (DDIV[3:0]). DDIV maximizes at %1001 (values of %1010 through %1111 are interpreted as %1001), which corresponds to a divide by 512. When DDIV is %0000, the ring oscillator's output is divided by 1. Incrementing DDIV by one will double the period; decrementing DDIV will halve the period. The DLF cannot directly increment or decrement DDIV; DDIV is only incremented or decremented when an addition or subtraction to DSTG carries or borrows.

Table 8-2. Quantization Error in ICLK

DDIV[3:0]	ICLK Cycles	Bus Cycles	τ_{ICLK} Q-ERR
%0000 (min)	1	NA	6.45%–11.8%
%0000 (min)	4	1	1.61%–2.94%
%0000 (min)	≥ 32	≥ 8	0.202%–0.368%
%0001	1	NA	3.23%–5.88%
%0001	4	1	0.806%–1.47%
%0001	≥ 16	≥ 4	0.202%–0.368%
%0010	1	NA	1.61%–2.94%
%0010	4	1	0.403%–0.735%
%0010	≥ 8	≥ 2	0.202%–0.368%
%0011	1	NA	0.806%–1.47%
%0011	≥ 4	≥ 1	0.202%–0.368%
%0100	1	NA	0.403%–0.735%
%0100	≥ 2	≥ 1	0.202%–0.368%
%0101–%1001 (max)	≥ 1	≥ 1	0.202%–0.368%

8.4.4.3 Variable-Delay Ring Oscillator

The variable-delay ring oscillator's period is adjustable from 17 to 31 stage delays, in increments of two, based on the upper three DCO stage control bits (DSTG[7:5]). A DSTG[7:5] of %000 corresponds to 17 stage delays; DSTG[7:5] of %111 corresponds to 31 stage delays. Adjusting the DSTG[5] bit has a 6.45 percent to 11.8 percent effect on the output frequency. This also corresponds to the size correction made when the frequency error is greater than ±15 percent. The value of the binary weighted divider does not affect the relative change in output clock period for a given change in DSTG[7:5].

Table 8-4. ICG Module Register Bit Interaction Summary

Condition	Register Bit Results for Given Condition											
	CMIE	CMF	CMON	CS	ICGON	ICGS	ECQON	ECQ	N[6:0]	TRIM[7:0]	DDIV[3:0]	DSTQ[7:0]
Reset	0	0	0	0	1	0	0	0	$15	$80	—	—
OSCENINSTOP = 0, STOP = 1	0	0	0	—	—	0	—	0	—	—	—	—
EXTCLKEN = 0	0	0	0	0	1	—	0	0	—	—	uw	uw
CMF = 1	—	(1)	1	—	1	—	1	—	uw	uw	uw	uw
CMON = 0	0	0	(0)	—	—	—	—	—	—	—	—	—
CMON = 1	—	—	(1)	—	1	—	1	—	uw	uw	uw	uw
CS = 0	—	—	—	(0)	1	—	—	—	—	—	uw	uw
CS = 1	—	—	—	(1)	—	—	1	—	—	—	—	—
ICGON = 0	0	0	0	1	(0)	0	1	—	—	—	—	—
ICGON = 1	—	—	—	—	(1)	—	—	—	—	—	uw	uw
ICGS = 0	us	—	us	uc	—	(0)	—	—	—	—	—	—
ECGON = 0	0	0	0	0	1	—	(0)	0	—	—	uw	uw
ECGS = 0	us	—	us	us	—	—	—	(0)	—	—	—	—
IOFF = 1	—	1*	(1)	1	(1)	0	(1)	—	uw	uw	uw	uw
EOFF = 1	—	1*	(1)	0	(1)	—	(1)	0	uw	uw	uw	uw
N = written	(0)	(0)	(0)	—	—	0*	—	—	—	—	—	—
TRIM = written	(0)	(0)	(0)	—	—	0*	—	—	—	—	—	—

—	Register bit is unaffected by the given condition.
0, 1	Register bit is forced clear or set (respectively) in the given condition.
0*, 1*	Register bit is temporarily forced clear or set (respectively) in the given condition.
(0), (1)	Register bit must be clear or set (respectively) for the given condition to occur.
us, uc, uw	Register bit cannot be set, cleared, or written (respectively) in the given condition.

8.7.1 ICG Control Register

The ICG control register (ICGCR) contains the control and status bits for the internal clock generator, external clock generator, and clock monitor as well as the clock select and interrupt enable bits.

Address: $0036

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CMIE	CMF	CMON	CS	ICGON	ICGS	ECGON	ECGS
Write:		0(1)						
Reset:	0	0	0	0	1	0	0	0

1. See CMF bit description for method of clearing CMF bit.

= Unimplemented

Figure 8-9. ICG Control Register (ICGCR)

Chapter 10
Keyboard Interrupt (KBI) Module

10.1 Introduction

The keyboard interrupt module (KBI) provides independently maskable external interrupts.

The KBI shares its pins with general-purpose input/output (I/O) port pins. See Figure 10-1 for port location of these shared pins.

10.2 Features

Features of the keyboard interrupt module include:

- Keyboard interrupt pins with separate keyboard interrupt enable bits and one keyboard interrupt mask
- Programmable edge-only or edge and level interrupt sensitivity
- Edge sensitivity programmable for rising or falling edge
- Level sensitivity programmable for high or low level
- Pullup or pulldown device automatically enabled based on the polarity of edge or level detect
- Exit from low-power modes

10.3 Functional Description

The keyboard interrupt module controls the enabling/disabling of interrupt functions on the KBI pins. These pins can be enabled/disabled independently of each other.

10.3.1 Keyboard Operation

Writing to the KBIEx bits in the keyboard interrupt enable register (KBIER) independently enables or disables each KBI pin. The polarity of the keyboard interrupt is controlled using the KBIPx bits in the keyboard interrupt polarity register (KBIPR). Edge-only or edge and level sensitivity is controlled using the MODEK bit in the keyboard status and control register (KBISCR).

Enabling a keyboard interrupt pin also enables its internal pullup or pulldown device based on the polarity enabled. On falling edge or low level detection, a pullup device is configured. On rising edge or high level detection, a pulldown device is configured.

The keyboard interrupt latch is set when one or more enabled keyboard interrupt inputs are asserted.

- If the keyboard interrupt sensitivity is edge-only, for KBIPx = 0, a falling (for KBIPx = 1, a rising) edge on a keyboard interrupt input does not latch an interrupt request if another enabled keyboard pin is already asserted. To prevent losing an interrupt request on one input because another input remains asserted, software can disable the latter input while it is asserted.
- If the keyboard interrupt is edge and level sensitive, an interrupt request is present as long as any enabled keyboard interrupt input is asserted.

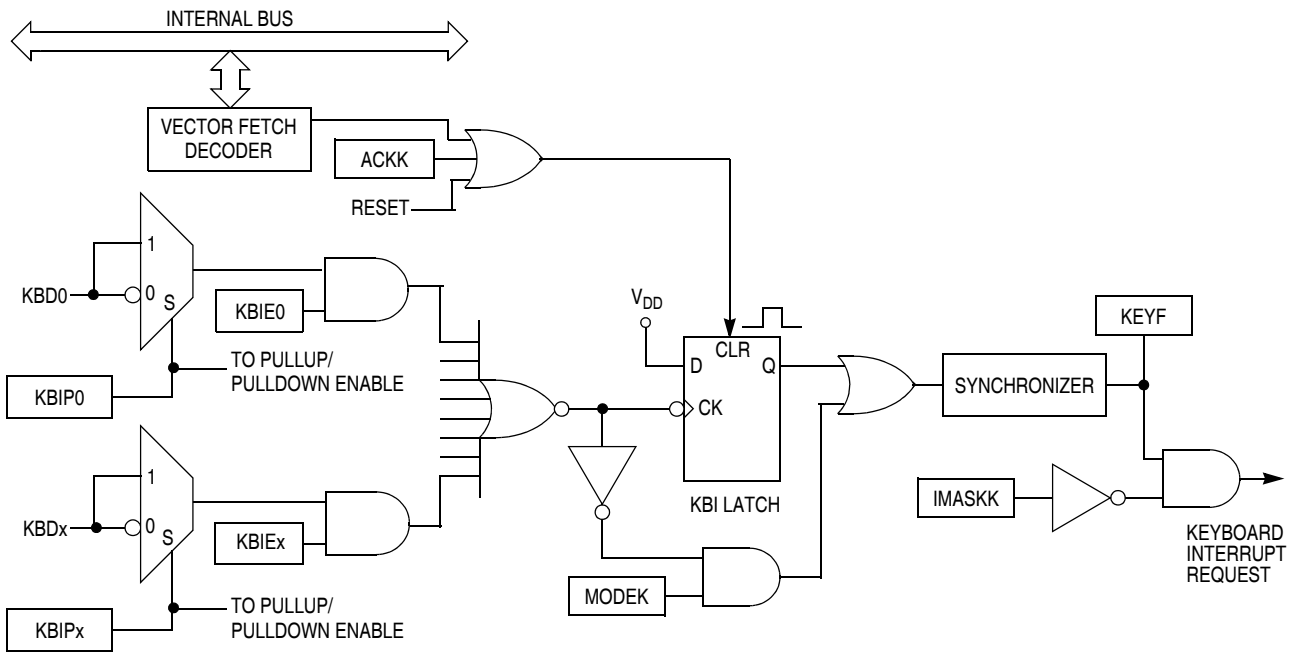


Figure 10-2. Keyboard Interrupt Block Diagram

10.3.1.1 MODEK = 1

If the MODEK bit is set, the keyboard interrupt inputs are both edge and level sensitive. The KBIPx bit will determine whether a edge sensitive pin detects rising or falling edges and on level sensitive pins whether the pin detects low or high levels. With MODEK set, both of the following actions must occur to clear a keyboard interrupt request:

- Return of all enabled keyboard interrupt inputs to a deasserted level. As long as any enabled keyboard interrupt pin is asserted, the keyboard interrupt remains active.
- Vector fetch or software clear. A KBI vector fetch generates an interrupt acknowledge signal to clear the KBI latch. Software generates the interrupt acknowledge signal by writing a 1 to ACKK in KBSCR. The ACKK bit is useful in applications that poll the keyboard interrupt inputs and require software to clear the KBI latch. Writing to ACKK prior to leaving an interrupt service routine can also prevent spurious interrupts due to noise. Setting ACKK does not affect subsequent transitions on the keyboard interrupt inputs. An edge detect that occurs after writing to ACKK latches another interrupt request. If the keyboard interrupt mask bit, IMASKK, is clear, the CPU loads the program counter with the KBI vector address.

The KBI vector fetch or software clear and the return of all enabled keyboard interrupt pins to a deasserted level may occur in any order.

Reset clears the keyboard interrupt request and the MODEK bit, clearing the interrupt request even if a keyboard interrupt input stays asserted.

10.3.1.2 MODEK = 0

If the MODEK bit is clear, the keyboard interrupt inputs are edge sensitive. The KBIPx bit will determine whether an edge sensitive pin detects rising or falling edges. A KBI vector fetch or software clear immediately clears the KBI latch.

When bit DDRCx is a 1, reading address $0002 reads the PTCx data latch. When bit DDRCx is a 0, reading address $0002 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit. Table 12-3 summarizes the operation of the port C pins.

Table 12-3. Port C Pin Functions

DDRC Bit	PTC Bit	I/O Pin Mode	Accesses to DDRC	Accesses to PTC	
			Read/Write	Read	Write
0	2	Input, Hi-Z	DDRC[7]	Pin	PTC2
1	2	Output	DDRC[7]	0	—
0	X	Input, Hi-Z	DDRC[4:0]	Pin	PTC[4:0](1)
1	X	Output	DDRC[4:0]	PTC[4:0]	PTC[4:0]

X = don't care
Hi-Z = high impedance
1. Writing affects data register, but does not affect input.

12.5 Port D

Port D is a 2-bit special function port that shares its pins with the timer interface module (TIMA).

12.5.1 Port D Data Register

The port D data register contains a data latch for each of the two port D pins.

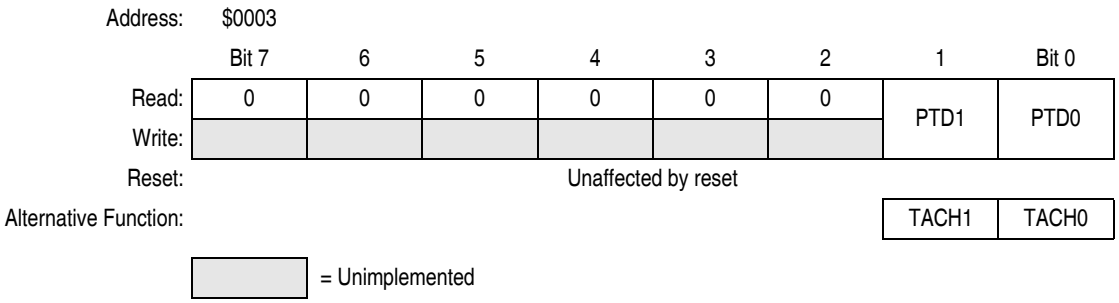


Figure 12-10. Port D Data Register (PTD)

PTD[1:0] — Port D Data Bits

PTD[1:0] are read/write, software programmable bits. Data direction of each port D pin is under the control of the corresponding bit in data direction register D.

12.5.2 Data Direction Register D

Data direction register D determines whether each port D pin is an input or an output. Writing a 1 to a DDRD bit enables the output buffer for the corresponding port D pin; a 0 disables the output buffer.

the IDLE bit has been cleared, a valid character must again set the SCRF bit before an idle condition can set the IDLE bit. Reset clears the IDLE bit.

1 = Receiver input idle

0 = Receiver input active (or idle since the IDLE bit was cleared)

OR — Receiver Overrun Bit

This clearable, read-only bit is set when software fails to read the SCDR before the receive shift register receives the next character. The OR bit generates an ESCI error CPU interrupt request if the ORIE bit in SCC3 is also set. The data in the shift register is lost, but the data already in the SCDR is not affected. Clear the OR bit by reading SCS1 with OR set and then reading the SCDR. Reset clears the OR bit.

1 = Receive shift register full and SCRF = 1

0 = No receiver overrun

Software latency may allow an overrun to occur between reads of SCS1 and SCDR in the flag-clearing sequence. Figure 13-13 shows the normal flag-clearing sequence and an example of an overrun caused by a delayed flag-clearing sequence. The delayed read of SCDR does not clear the OR bit because OR was not set when SCS1 was read. Byte 2 caused the overrun and is lost. The next flag-clearing sequence reads byte 3 in the SCDR instead of byte 2.

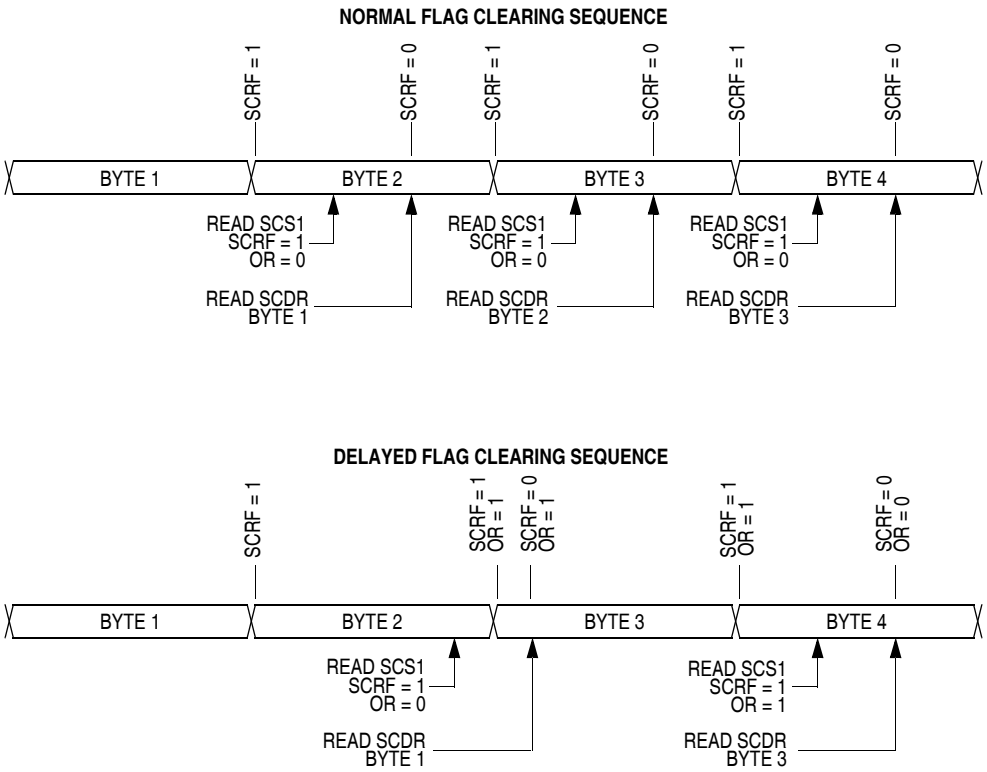


Figure 13-13. Flag Clearing Sequence

In applications that are subject to software latency or in which it is important to know which byte is lost due to an overrun, the flag-clearing routine can check the OR bit in a second read of SCS1 after reading the data register.

RPF — Reception in Progress Flag Bit

This read-only bit is set when the receiver detects a 0 during the RT1 time period of the start bit search. RPF does not generate an interrupt request. RPF is reset after the receiver detects false start bits (usually from noise or a baud rate mismatch), or when the receiver detects an idle character. Polling RPF before disabling the ESCI module or entering stop mode can show whether a reception is in progress.

1 = Reception in progress
0 = No reception in progress

13.8.6 ESCI Data Register

The ESCI data register (SCDR) is the buffer between the internal data bus and the receive and transmit shift registers. Reset has no effect on data in the ESCI data register.

Address: $0015

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R7	R6	R5	R4	R3	R2	R1	R0
Write:	T7	T6	T5	T4	T3	T2	T1	T0
Reset:	Unaffected by Reset							

Figure 13-15. ESCI Data Register (SCDR)

R7/T7:R0/T0 — Receive/Transmit Data Bits

Reading address $0018 accesses the read-only received data bits, R7:R0. Writing to address $0018 writes the data to be transmitted, T7:T0. Reset has no effect on the ESCI data register.

NOTE

Do not use read-modify-write instructions on the ESCI data register.

13.8.7 ESCI Baud Rate Register

The ESCI baud rate register (SCBR) together with the ESCI prescaler register selects the baud rate for both the receiver and the transmitter.

NOTE

There are two prescalers available to adjust the baud rate. One in the ESCI baud rate register and one in the ESCI prescaler register.

Address: $0016

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	LINT	LINR	SCP1	SCP0	R	SCR2	SCR1	SCR0
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 13-16. ESCI Baud Rate Register (SCBR)

LINT — LIN Break Symbol Transmit Enable

This read/write bit selects the enhanced ESCI features for master nodes in the local interconnect network (LIN) protocol (version 1.2) as shown in Table 13-6. Reset clears LINT.

Chapter 14
System Integration Module (SIM)

14.1 Introduction

This section describes the system integration module (SIM), which supports up to 24 external and/or internal interrupts. The SIM is a system state controller that coordinates the central processor unit (CPU) and exception timing. Together with the CPU, the SIM controls all microcontroller unit (MCU) activities. A block diagram of the SIM is shown in Figure 14-1.

The SIM is responsible for:

- Bus clock generation and control for CPU and peripherals:
  - Stop/wait/reset entry and recovery
  - Internal clock control
- Master reset control, including power-on reset (POR) and computer operating properly (COP) timeout
- Interrupt control:
  - Acknowledge timing
  - Arbitration control timing
  - Vector address generation
- CPU enable/disable timing
- Modular architecture expandable to 128 interrupt sources

Table 14-1 shows the internal signal names used in this section.

Table 14-1. Signal Name Conventions

Signal Name	Description
CGMXCLK	Selected clock source from internal clock generator module (ICG)
CGMOUT	Clock output from ICG module (bus clock = CGMOUT divided by two)
IAB	Internal address bus
IDB	Internal data bus
PORRST	Signal from the power-on reset (POR) module to the SIM
IRST	Internal reset signal
R/$\overline{W}$	Read/write signal

14.2 SIM Bus Clock Control and Generation

The bus clock generator provides system clock signals for the CPU and peripherals on the MCU. The system clocks are generated from an incoming clock, CGMOUT, as shown in Figure 14-2. This clock originates from either an external oscillator or from the internal clock generator.

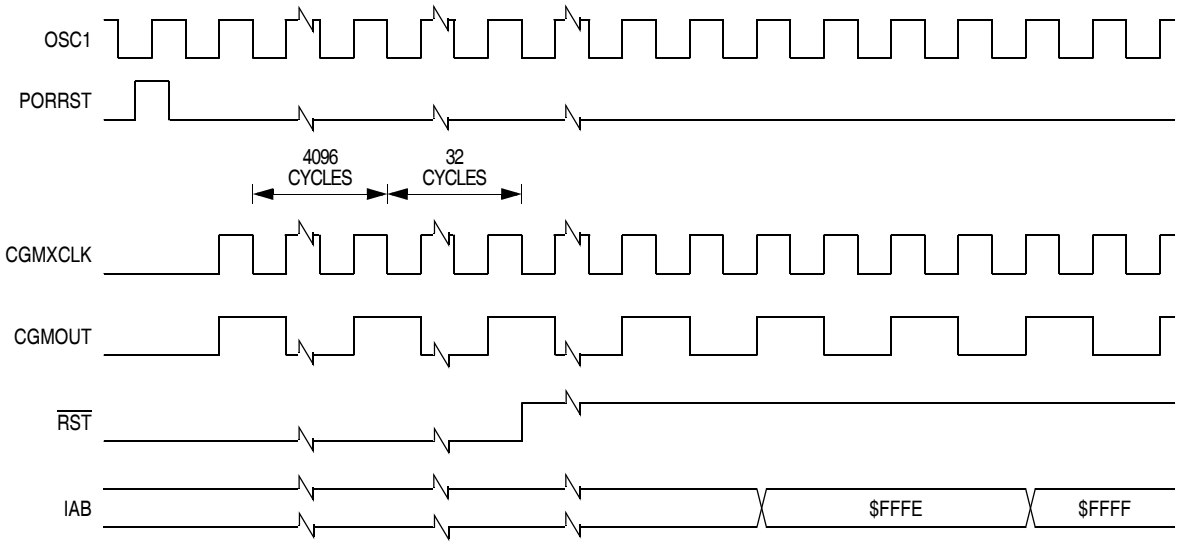


Figure 14-6. POR Recovery

14.3.2.2 Computer Operating Properly (COP) Reset

An input to the SIM is reserved for the COP reset signal. The overflow of the COP counter causes an internal reset and sets the COP bit in the reset status register (SRSR).

To prevent a COP module timeout, write any value to location $FFFF. Writing to location $FFFF clears the COP counter and stages 12–5 of the SIM counter. The SIM counter output, which occurs at least every 4080 CGMXCLK cycles, drives the COP counter. The COP should be serviced as soon as possible out of reset to guarantee the maximum amount of time before the first timeout.

The COP module is disabled if the $\overline{\text{IRQ}}$ pin is held at V_{TST} while the MCU is in monitor mode. The COP module can be disabled only through combinational logic conditioned with the high-voltage signal on the $\overline{\text{IRQ}}$ pin. This prevents the COP from becoming disabled as a result of external noise.

14.3.2.3 Illegal Opcode Reset

The SIM decodes signals from the CPU to detect illegal instructions. An illegal instruction sets the ILOP bit in the SIM reset status register (SRSR) and causes a reset.

If the stop enable bit, STOP, in the configuration register (CONFIG1) is 0, the SIM treats the STOP instruction as an illegal opcode and causes an illegal opcode reset.

14.3.2.4 Illegal Address Reset

An opcode fetch from an unmapped address generates an illegal address reset. The SIM verifies that the CPU is fetching an opcode prior to asserting the ILAD bit in the SIM reset status register (SRSR) and resetting the MCU. A data fetch from an unmapped address does not generate a reset.

14.3.2.5 Forced Monitor Mode Entry Reset (MENRST)

The MENRST module is monitoring the reset vector fetches and will assert an internal reset if it detects that the reset vectors are erased ($00). When the MCU comes out of reset, it is forced into monitor mode. See 19.3 Monitor Module (MON).

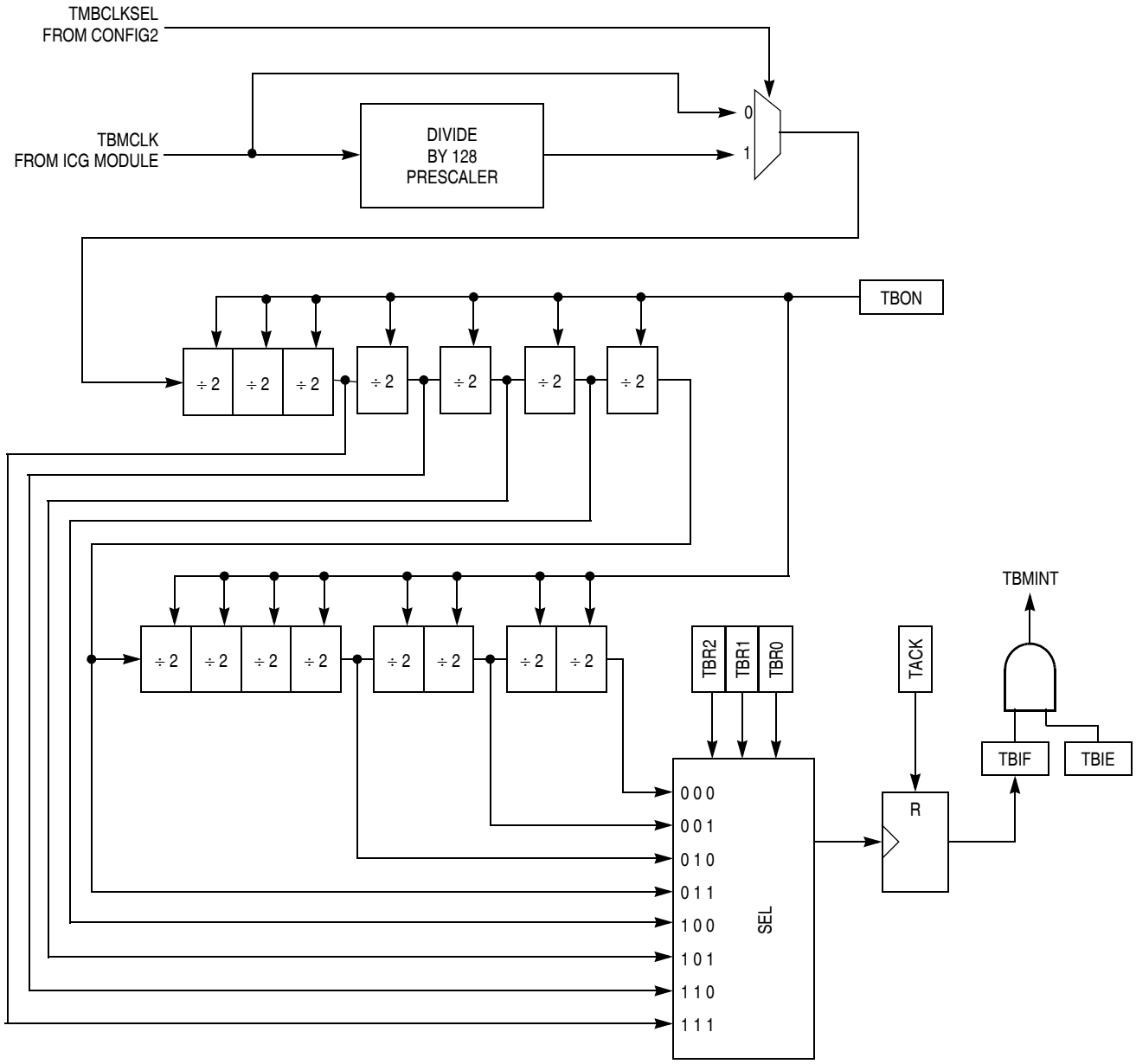


Figure 16-1. Timebase Block Diagram

16.5 TBM Interrupt Rate

The interrupt rate is determined by the equation:

$$t_{TBMRATE} = \frac{1}{f_{TBMRATE}} = \frac{Divider}{f_{TBMCLK}}$$

where:

f_{TBMCLK} = Frequency supplied from the internal clock generator (ICG) module

Divider = Divider value as determined by TBR2–TBR0 settings. See Table 16-1.

18.8 I/O Registers

These I/O registers control and monitor TIMB operation:

- TIMB status and control register, TBSC
- TIMB control registers, TBCNTH–TBCNTL
- TIMB counter modulo registers, TBMODH–TBMODL
- TIMB channel status and control registers, TBSC0 and TBSC1
- TIMB channel registers, TBCH0H–TBCH0L and TBCH1H–TBCH1L

18.8.1 TIMB Status and Control Register

The TIMB status and control register:

- Enables TIMB overflow interrupts
- Flags TIMB overflows
- Stops the TIMB counter
- Resets the TIMB counter
- Prescales the TIMB counter clock

Address: $002B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOF	TOIE	TSTOP	0	R	PS2	PS1	PS0
Write:	0			TRST				
Reset:	0	0	1	0	0	0	0	0

R = Reserved

Figure 18-4. TIMB Status and Control Register (TBSC)

TOF — TIMB Overflow Flag Bit

This read/write flag is set when the TIMB counter reaches the modulo value programmed in the TIMB counter modulo registers. Clear TOF by reading the TIMB status and control register when TOF is set and then writing a 0 to TOF. If another TIMB overflow occurs before the clearing sequence is complete, then writing 0 to TOF has no effect. Therefore, a TOF interrupt request cannot be lost due to inadvertent clearing of TOF. Reset clears the TOF bit. Writing a 1 to TOF has no effect.

1 = TIMB counter has reached modulo value
0 = TIMB counter has not reached modulo value

TOIE — TIMB Overflow Interrupt Enable Bit

This read/write bit enables TIMB overflow interrupts when the TOF bit becomes set. Reset clears the TOIE bit.

1 = TIMB overflow interrupts enabled
0 = TIMB overflow interrupts disabled

18.8.5 TIMB Channel Registers

These read/write registers contain the captured TIMB counter value of the input capture function or the output compare value of the output compare function. The state of the TIMB channel registers after reset is unknown.

In input capture mode (MSxB–MSxA = 0:0), reading the high byte of the TIMB channel x registers (TBCHxH) inhibits input captures until the low byte (TBCHxL) is read.

In output compare mode (MSxB–MSxA ≠ 0:0), writing to the high byte of the TIMB channel x registers (TBCHxH) inhibits output compares and the CHxF bit until the low byte (TBCHxL) is written.

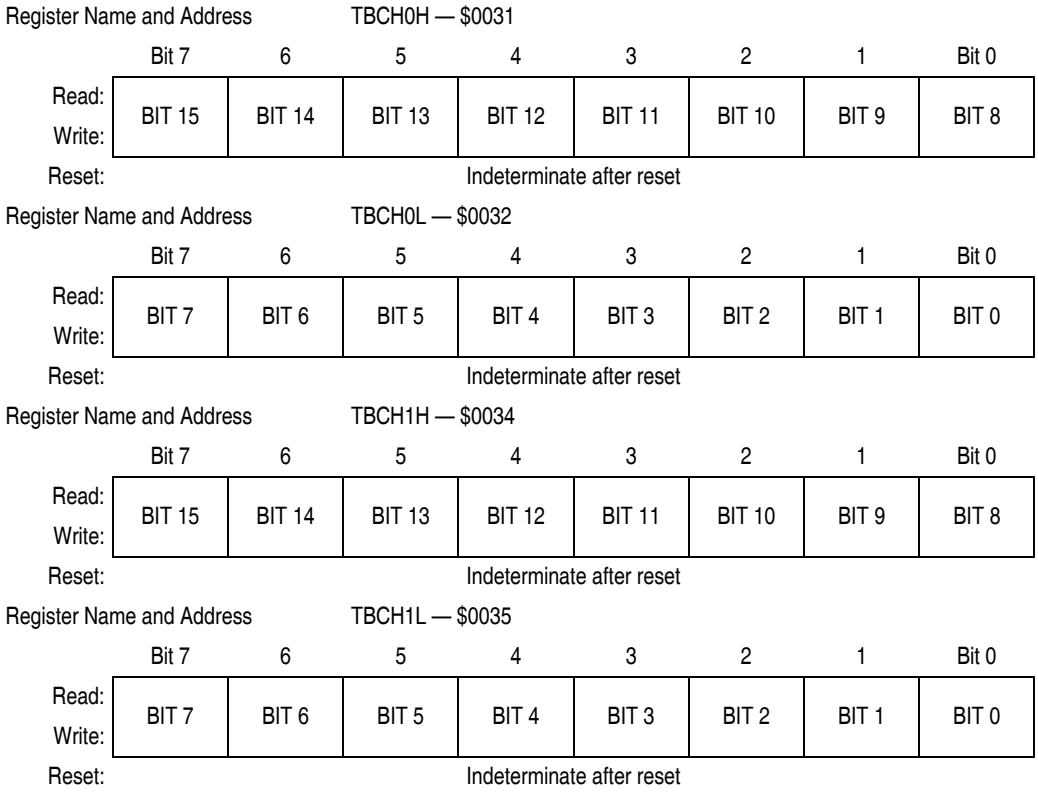


Figure 18-9. TIMB Channel Registers (TBCH0H/L–TBCH1H/L)

Table 19-10. Summary of On-Chip FLASH Support Routines

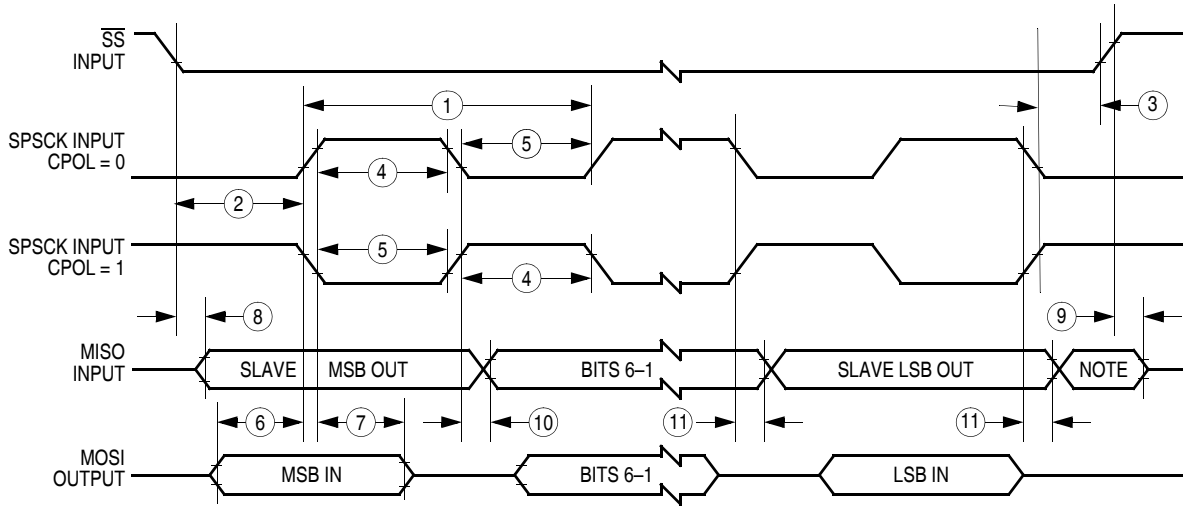
	GetByte	PutByte	Verify	fProgram	fErase
Jump Table Address	$1000	$100C	$1003	$1009	$1006
Routine Description	Get a data byte serially through PTA0	Send a data byte serially through PTA0	Read and/or compare a FLASH range	Program a FLASH range	Erase a PAGE or entire array
Internal Operating Frequency (f_{op})	N/A	N/A	N/A	1.0 MHz to 8.0 MHz	1.0 MHz to 8.0 MHz
Hardware Requirement	Pullup on PTA0	Pullup on PTA0	For send-out option, pullup on PTA0	N/A	N/A
Entry Conditions	PTA0: Input (DDRA0 = 0)	PTA0: Input and 0 data bit (DDRA0 = 0, PTA0 = 0) A: data to be sent	H:X: First address of range LADDR: Last address of range A: A = $00 for send-out option or A ≠ $00 for compare option. For send-out option, PTA0: Input and 0 data bit (DDRA0 = 0, PTA0 = 0) For compare option, DATA array: Load data to be compared against FLASH read data	H:X: First address of range LADDR: Last address of range CPUSPD: the nearest integer f_{op} (in MHz) times 4 Data array: Load data to be programmed	H:X: Page erase — an address within the page Mass erase = FLBPR CPUSPD: the nearest integer f_{op} (in MHz) times 4
Exit Conditions	A: Data received through PTA0 C-bit: Framing error indicator (error: C = 0)	A, X: No change PTA0: Input and 0 data bit (DDRA0 = 0, PTA0 = 0)	A: Checksum H:X: Next FLASH address C-bit: Verify result indicator (success: C = 1) DATA array: Data replaced with FLASH read data (compare option)	H:X: Next FLASH address	H:X: No change
I Bit	I bit is preserved	I bit is preserved	I bit is preserved	I bit is set, then restored to entry condition on exit	I bit is set, then restored to entry condition on exit
COP	Not Serviced	Not Serviced	Serviced	Serviced	Serviced

Continued on next page

20.7 3V DC Electrical Characteristics

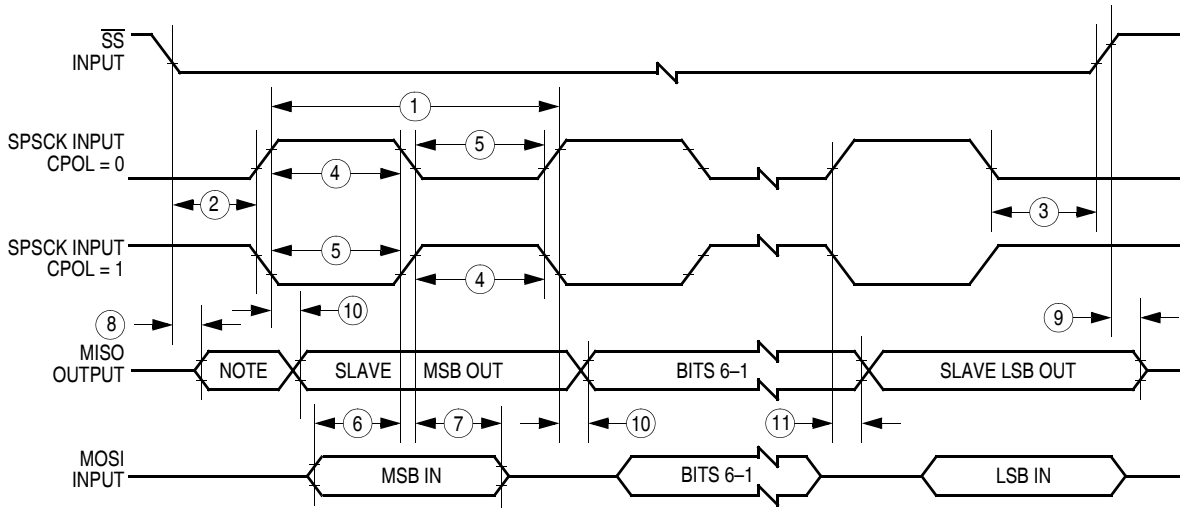
Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output high voltage I_{Load} = –0.6 mA, all I/O pins I_{Load} = –4.0 mA, all I/O pins I_{Load} = –10.0 mA, PTA0–PTA6/$\overline{SS}$, PTC0–PTC1 only	V_{OH}	 V_{DD}–0.3 V_{DD}–1.0 V_{DD}–0.8	 — — —	 — — —	V
Output low voltage I_{Load} = 0.5 mA, all I/O pins I_{Load} = 6.0 mA, all I/O pins I_{Load} = 10.0 mA, PTA0–PTA6/$\overline{SS}$, PTC0–PTC1 only	V_{OL}	 — — —	 — — —	 0.3 1.0 0.8	V
Input high voltage — all ports, $\overline{IRQ}$, $\overline{RST}$	V_{IH}	0.7 x V_{DD}	—	V_{DD} + 0.3	V
Input low voltage — all ports, $\overline{IRQ}$, $\overline{RST}$	V_{IL}	V_{SS}	—	0.3 x V_{DD}	V
DC injection current, all ports	I_{INJ}	–2	—	+2	mA
Total dc current injection (sum of all I/O)	I_{INJTOT}	–25	—	+25	mA
V_{DD} + V_{DDA} supply current Run[3],[4] Wait[4], [5] Stop (LVI off) @ 25°C[4], [6] Stop (LVI on) @ 25°C Stop (LVI off), –40°C to 125°C Stop (LVI on), –40°C to 125°C	I_{DD}	 — — — — — —	 5.7 1.8 0.52 0.15 1.6 0.15	 TBD TBD TBD TBD TBD TBD	 mA mA µA mA µA mA
Ports Hi-Z leakage current	I_{IL}	–1	±0.1	+1	mA
Input current – $\overline{RST}$, OSC1	I_{In}	–1	—	+1	µA
Capacitance Ports (as input or output)	C_{IN} C_{OUT}	— —	— —	12 8	pF
POR rearm voltage	V_{POR}	750	—	—	mV
POR rise time ramp rate	R_{POR}	0.035	—	—	V/ms
Monitor mode entry voltage	V_{TST}	V_{DD} + 2.5	—	9.1	V
Low-voltage inhibit reset, trip falling voltage[7]	V_{TRIPF}	2.35	2.60	2.70	V
Low-voltage inhibit reset, trip rising voltage[7]	V_{TRIPR}	2.45	2.66	2.80	V
Low-voltage inhibit reset/recover hysteresis[7]	V_{HYS}	—	60	—	mV
Pullup resistor — PTA0–PTA6/$\overline{SS}$, $\overline{IRQ}$, $\overline{RST}$[8]	R_{PU}	16	26	36	kΩ
Pulldown resistor — PTA0–PTA4[9]	R_{PD}	16	26	36	kΩ

1. V_{DD} = 2.7 to 3.3 Vdc, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted.
2. Typical values reflect average measurements at midpoint of voltage range, 25•C only.
3. Run (operating) I_{DD} measured using internal oscillator at its 16-MHz rate. V_{DD} = 3.0 Vdc. All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. All ports configured as inputs. Measured with all modules enabled.
4. All measurements taken with LVI enabled.
5. Wait I_{DD} measured using internal oscillator at its 16-MHz rate. All inputs 0.2 V from rail; no dc loads; less than 100 pF on all outputs. All ports configured as inputs.
6. Stop I_{DD} is measured with no port pin sourcing current; all modules are disabled. OSCSTOPEN option is not selected.
7. These values assume the LVI is operating in 3-V mode (i.e. LVI5OR3 bit is set to 0)
8. R_{PU} is measured at V_{DD} = 3.0 V.
9. Pulldown resistors available only when KBIx is enabled with KBIPx = 1.



Note: Not defined but normally MSB of character just received

a) SPI Slave Timing (CPHA = 0)



Note: Not defined but normally LSB of character previously transmitted

b) SPI Slave Timing (CPHA = 1)

Figure 20-4. SPI Slave Timing

20.17.2 Conducted Transient Susceptibility

Microcontroller transient conducted susceptibility is measured in accordance with an internal Freescale test method. The measurement is performed with the microcontroller installed on a custom EMC evaluation board and running specialized EMC test software designed in compliance with the test method. The conducted susceptibility is determined by injecting the transient susceptibility signal on each pin of the microcontroller. The transient waveform and injection methodology are in accordance with IEC 61000-4-2 (ESD) and IEC 61000-4-4 (EFT/B). The transient voltage required to cause performance degradation on any pin in the tested configuration is greater than or equal to the reported levels unless otherwise indicated by footnotes below the table.

Parameter	Symbol	Conditions	f_{OSC}/f_{CPU}	Result	Amplitude(1) (Min)	Unit
Conducted susceptibility, electrical fast transient/burst (EFT/B)	V_{CS_EFT}	V_{DD} = 5 V T_A = +25°C 32 QFP	4/8	A	TBD	kV
				B	TBD	
				C	TBD	
				D	TBD	
Conducted susceptibility, electrostatic discharge (ESD)	V_{CS_ESD}	V_{DD} = 5 V T_A = +25°C 32 QFP	4/8	A	TBD	kV
				B	TBD	
				C	TBD	
				D	TBD	

1. Data based on qualification test results. Not tested in production.
2. These pins demonstrate particularly low levels of performance:

The susceptibility performance classification is described in the following table.

Result	Performance Criteria	
A	No failure	The MCU performs as designed during and after exposure.
B	Self-recovering failure	The MCU does not perform as designed during exposure. The MCU returns automatically to normal operation after exposure is removed.
C	Soft failure	The MCU does not perform as designed during exposure. The MCU does not return to normal operation until exposure is removed and the RESET pin is asserted.
D	Hard failure	The MCU does not perform as designed during exposure. The MCU does not return to normal operation until exposure is removed and the power to the MCU is cycled.
E	Damage	The MCU does not perform as designed during and after exposure. The MCU cannot be returned to proper operation due to physical damage or other permanent performance degradation.