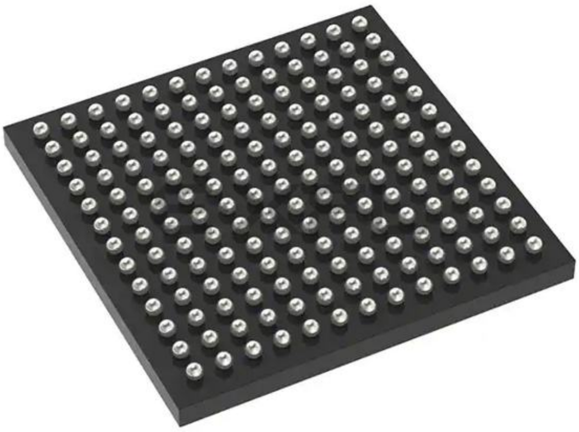

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	136
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	169-UFBGA
Supplier Device Package	169-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l496agi6p

Table 2. STM32L496xx family device features and peripheral counts (continued)

Peripheral	STM32L496Ax	STM32L496Zx	STM32L496Qx	STM32L496Vx	STM32L496Rx
LCD COM x SEG	Yes 8x40 or 4x44				
Random generator	Yes				
GPIOs(3) Wakeup pins Nb of I/Os down to 1.08 V	136 5 14	115 5 14	110 5 14	83 5 0	52 4 0
Capacitive sensing Number of channels	24	24	24	21	21
12-bit ADCs Number of channels	3 24	3 24	3 19	3 16	3 16
12-bit DAC channels	2				
Internal voltage reference buffer	Yes				
Analog comparator	2				
Operational amplifiers	2				
Max. CPU frequency	80 MHz				
Operating voltage (VDD)	1.71 to 3.6 V				
Operating voltage (VDD12)	1.05 to 1.32 V				
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 105 °C / -40 to 125 °C Junction temperature: -40 to 105 °C / -40 to 125 °C / -40 to 130 °C				
Packages	UFBGA169	LQFP144	UFBGA132	LQFP100 WLCSP100	LQFP64

1. For the LQFP100 and WLCSP100 packages, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.
2. Only up to 13 data bits.
3. In case external SMPS package type is used, 2 GPIO's are replaced by VDD12 pins to connect the SMPS power supplies hence reducing the number of available GPIO's by 2.

3.12 Clocks and startup

The clock controller (see *Figure 4*) distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
  - 4-48 MHz high-speed external crystal or ceramic resonator (HSE), that can supply a PLL. The HSE can also be configured in bypass mode for an external clock.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies from 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach better than ±0.25% accuracy. In this mode the MSI can feed the USB device, saving the need of an external high-speed crystal (HSE). The MSI can supply a PLL.
  - System PLL which can be fed by HSE, HSI16 or MSI, with a maximum frequency at 80 MHz.
- RC48 with clock recovery system (HSI48): internal 48 MHz clock source (HSI48)can be used to drive the USB, the SDMMC or the RNG peripherals. This clock can be output on the MCO.
- **Auxiliary clock source:** two ultralow-power clock sources that can be used to drive the LCD controller and the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock accuracy is ±5% accuracy.
- **Peripheral clock sources:** Several peripherals (USB, SDMMC, RNG, SAI, USARTs, I2Cs, LPTimers, ADC, SWPMI) have their own independent clock whatever the system clock. Three PLLs, each having three independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, the USB/SDMMC/RNG and the two SAIs.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 4 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI16 and a software

3.28 Real-time clock (RTC) and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to VBAT mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the V_{DD} supply when present or from the VBAT pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when VDD power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby or Shutdown mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32.

The RTC is functional in VBAT mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in VBAT mode, but is functional in all low-power modes except Shutdown mode.

All RTC events (Alarm, WakeUp Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

Table 15. STM32L496xx pin definitions (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP100	WLCSP100_SMPS	LQFP100	UFBGA132	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	-	-	-	D6	10	10	F5	F5	PF0	I/O	FT_f	-	I2C2_SDA, FMC_A0, EVENTOUT	-
-	-	-	-	D5	11	11	F4	F4	PF1	I/O	FT_f	-	I2C2_SCL, FMC_A1, EVENTOUT	-
-	-	-	-	D4	12	12	F3	F3	PF2	I/O	FT	-	I2C2_SMBA, FMC_A2, EVENTOUT	-
-	-	-	-	E4	13	13	G3	G3	PF3	I/O	FT_a	-	FMC_A3, EVENTOUT	ADC3_IN6
-	-	-	-	F3	14	14	G4	G4	PF4	I/O	FT_a	-	FMC_A4, EVENTOUT	ADC3_IN7
-	-	-	-	F4	15	15	G5	G5	PF5	I/O	FT_a	-	FMC_A5, EVENTOUT	ADC3_IN8
-	D9	E10	10	F2	16	16	F2	F2	VSS	S	-	-	-	-
-	E9	E9	11	G2	17	17	G2	G2	VDD	S	-	-	-	-
-	-	-	-	-	18	18	-	-	PF6	I/O	FT_a	-	TIM5_ETR, TIM5_CH1, QUADSPI_BK1_IO3, SAI1_SD_B, EVENTOUT	ADC3_IN9
-	-	-	-	-	19	19	-	-	PF7	I/O	FT_a	-	TIM5_CH2, QUADSPI_BK1_IO2, SAI1_MCLK_B, EVENTOUT	ADC3_IN10
-	-	-	-	-	20	20	-	-	PF8	I/O	FT_a	-	TIM5_CH3, QUADSPI_BK1_IO0, SAI1_SCK_B, EVENTOUT	ADC3_IN11
-	-	-	-	-	21	21	-	-	PF9	I/O	FT_a	-	TIM5_CH4, QUADSPI_BK1_IO1, SAI1_FS_B, TIM15_CH1, EVENTOUT	ADC3_IN12
-	-	-	-	-	22	22	H4	H4	PF10	I/O	FT_a	-	QUADSPI_CLK, DCMI_D11, TIM15_CH2, EVENTOUT	ADC3_IN13

Table 15. STM32L496xx pin definitions (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP100	WLCSP100_SMPS	LQFP100	UFBGA132	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	-	-	-	J7	50	50	N6	N6	PF12	I/O	FT	-	FMC_A6, EVENTOUT	-
-	-	-	-	-	51	51	-	-	VSS	S	-	-	-	-
-	-	-	-	-	52	52	A8	A8	VDD	S	-	-	-	-
-	-	-	-	K7	53	53	M6	M6	PF13	I/O	FT	-	I2C4_SMBA, DFSDM1_DATIN6, FMC_A7, EVENTOUT	-
-	-	-	-	J8	54	54	L6	L6	PF14	I/O	FT_fa	-	I2C4_SCL, DFSDM1_CKIN6, TSC_G8_IO1, FMC_A8, EVENTOUT	-
-	-	-	-	J9	55	55	K6	K6	PF15	I/O	FT_fa	-	I2C4_SDA, TSC_G8_IO2, FMC_A9, EVENTOUT	-
-	-	-	-	H9	56	56	J6	J6	PG0	I/O	FT	-	TSC_G8_IO3, FMC_A10, EVENTOUT	-
-	-	-	-	G9	57	57	H6	H6	PG1	I/O	FT	-	TSC_G8_IO4, FMC_A11, EVENTOUT	-
-	K6	K6	38	M7	58	58	L7	L7	PE7	I/O	FT	-	TIM1_ETR, DFSDM1_DATIN2, FMC_D4, SAI1_SD_B, EVENTOUT	-
-	K5	K5	39	L7	59	59	K7	K7	PE8	I/O	FT	-	TIM1_CH1N, DFSDM1_CKIN2, FMC_D5, SAI1_SCK_B, EVENTOUT	-
-	J5	J5	40	M8	60	60	J7	J7	PE9	I/O	FT	-	TIM1_CH1, DFSDM1_CKOUT, FMC_D6, SAI1_FS_B, EVENTOUT	-
-	-	-	-	F6	61	61	M7	M7	VSS	S	-	-	-	-
-	-	-	-	G6	62	62	N7	N7	VDD	S	-	-	-	-

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 16*) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	CAN2/ OTG_FS/DCMI/ QUADSPI	LCD	SDMMC/ COMP1/2/FM C/SWPMI1	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port I	PI0	-	-	DCMI_D13	-	-	-	-	EVENTOUT
	PI1	-	-	DCMI_D8	-	-	-	-	EVENTOUT
	PI2	-	-	DCMI_D9	-	-	-	-	EVENTOUT
	PI3	-	-	DCMI_D10	-	-	-	-	EVENTOUT
	PI4	-	-	DCMI_D5	-	-	-	-	EVENTOUT
	PI5	-	-	DCMI_VSYNC	-	-	-	-	EVENTOUT
	PI6	-	-	DCMI_D6	-	-	-	-	EVENTOUT
	PI7	-	-	DCMI_D7	-	-	-	-	EVENTOUT
	PI8	-	-	DCMI_D12	-	-	-	-	EVENTOUT
	PI9	-	CAN1_RX	-	-	-	-	-	EVENTOUT
	PI10	-	-	-	-	-	-	-	EVENTOUT
	PI11	-	-	-	-	-	-	-	EVENTOUT

Table 19. Voltage characteristics(1)

Symbol	Ratings		Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}, V_{BAT})		-0.3	4.0	V
VDD12 - VSS	External SMPS supply voltage	Range 1	-0.3	1.32	
		Range 2	-0.3		
V_{IN}(2)	Input voltage on FT_xxx pins		V_{SS}-0.3	min (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}) + 4.0(3)(4)	
	Input voltage on TT_xx pins		V_{SS}-0.3	4.0	
	Input voltage on BOOT0 pin		V_{SS}	9.0	
	Input voltage on any other pins		V_{SS}-0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DDX} power pins of the same domain		-	50	mV
$\|V_{SSx}-V_{SS}\|$	Variations between all the different ground pins(5)		-	50	mV

1. All main power (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 20: Current characteristics* for the maximum allowed injected current values.
3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

Table 20. Current characteristics

Symbol	Ratings	Max	Unit
$\sum IV_{DD}$	Total current into sum of all V_{DD} power lines (source)(1) (2)	150	mA
$\sum IV_{SS}$	Total current out of sum of all V_{SS} ground lines (sink)(1)	150	
$IV_{DD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)(2)	100	
$IV_{SS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\sum I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(3)	100	
	Total output current sourced by sum of all I/Os and control pins(3)	100	
$I_{INJ(PIN)}$(4)	Injected current on FT_xxx, TT_xx, RST and B pins, except PA4, PA5	-5/+0(5)	
	Injected current on PA4, PA5	-5/0	
$\sum \|I_{INJ(PIN)}\|$	Total injected current (sum of all I/Os and control pins)(6)	25	

1. All main power (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. Valid also for VDD12 on SMPS Package

Table 44. Current consumption in Stop 2 mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL}(wake up from Stop2)	Supply current during wakeup from Stop 2 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1. See (4).	3 V	1.69	-	-	-	-	-	-	-	-	-	mA
		Wakeup clock is MSI = 4 MHz, voltage Range 2. See (4).	3 V	1.35	-	-	-	-	-	-	-	-	-	
		Wakeup clock is HSI16 = 16 MHz, voltage Range 1. See (4).	3 V	1.7	-	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. LCD enabled with external voltage source. Consumption from VLCD excluded. Refer to LCD controller characteristics for I_{VLCD}.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 51: Low-power mode wakeup timings*.

On-chip peripheral current consumption

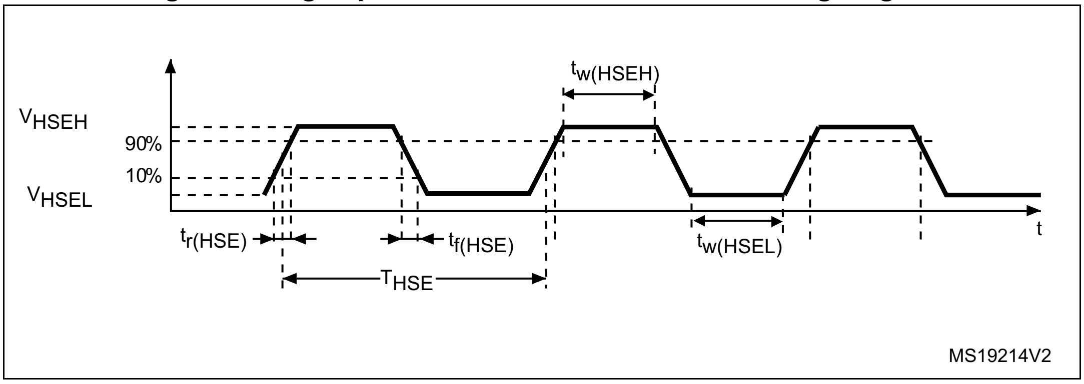
The current consumption of the on-chip peripherals is given in *Table 50*. The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in *Table 19: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in *Table 50*. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 50. Peripheral current consumption

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
AHB	Bus Matrix[(1)]	4.44	3.75	4.00	μA/MHz
	ADC independent clock domain	0.40	0.08	0.30	
	ADC AHB clock domain	5.55	4.63	5.00	
	CRC	0.48	0.42	0.50	
	DMA1	2.00	1.60	2.00	
	DMA2	1.76	1.50	1.50	
	DMA2D	24.33	20.21	24.50	
	FLASH	8.50	7.10	8.00	
	FMC	7.58	6.29	7.00	
	GPIOA[(2)]	1.59	1.25	1.50	
	GPIOB[(2)]	1.56	1.25	1.50	
	GPIOC[(2)]	1.58	1.29	1.50	
	GPIOD[(2)]	1.40	1.17	1.40	
	GPIOE[(2)]	1.36	1.13	1.40	
	GPIOF[(2)]	1.70	1.40	1.50	
	GPIOG[(2)]	1.80	1.50	1.80	
	GPIOH[(2)]	1.50	1.30	1.50	
	GPIOI[(2)]	1.18	0.96	1.00	
	DCMI	1.6	1.3	1.2	
	OTG_FS independent clock domain	23.20	NA	NA	
	OTG_FS AHB clock domain	14.30	NA	NA	
	QUADSPI	6.84	5.67	6.50	

Figure 21. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 22*.

Table 55. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	250	-	-	ns

1. Guaranteed by design.

Figure 22. Low-speed external clock source AC timing diagram

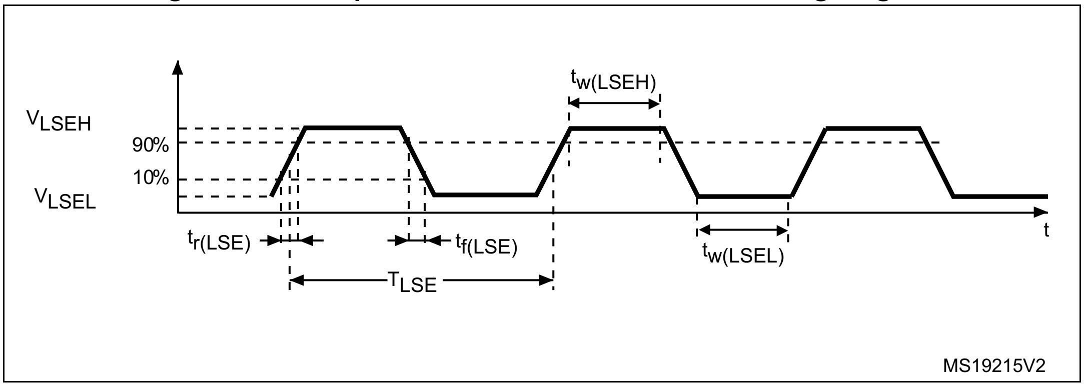
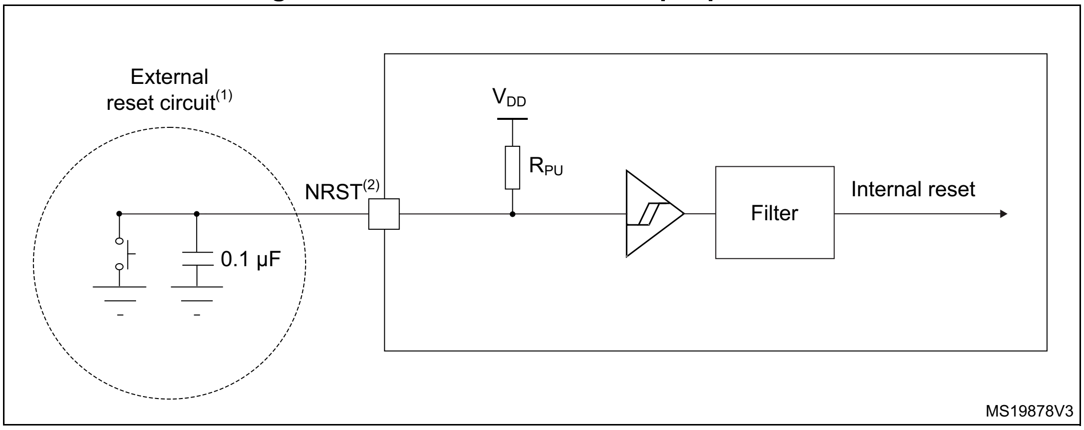


Table 72. I/O AC characteristics[(1)][(2)]

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	0.1	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	10	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1.5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	0.1	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	52	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	140	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	17	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	110	
01	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	10	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	1	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	15	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	1	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	9	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	16	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	40	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	4.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	9	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	21	

Figure 30. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 73: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

6.3.16 Analog switches booster

Table 74. Analog switches booster characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.62	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	240	µs
$I_{DD(BOOST)}$	Booster consumption for $1.62\ V \leq V_{DD} \leq 2.0\ V$	-	-	250	µA
	Booster consumption for $2.0\ V \leq V_{DD} \leq 2.7\ V$	-	-	500	
	Booster consumption for $2.7\ V \leq V_{DD} \leq 3.6\ V$	-	-	900	

1. Guaranteed by design.

SPI characteristics

Unless otherwise specified, the parameters given in *Table 95* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 22: General operating conditions*.

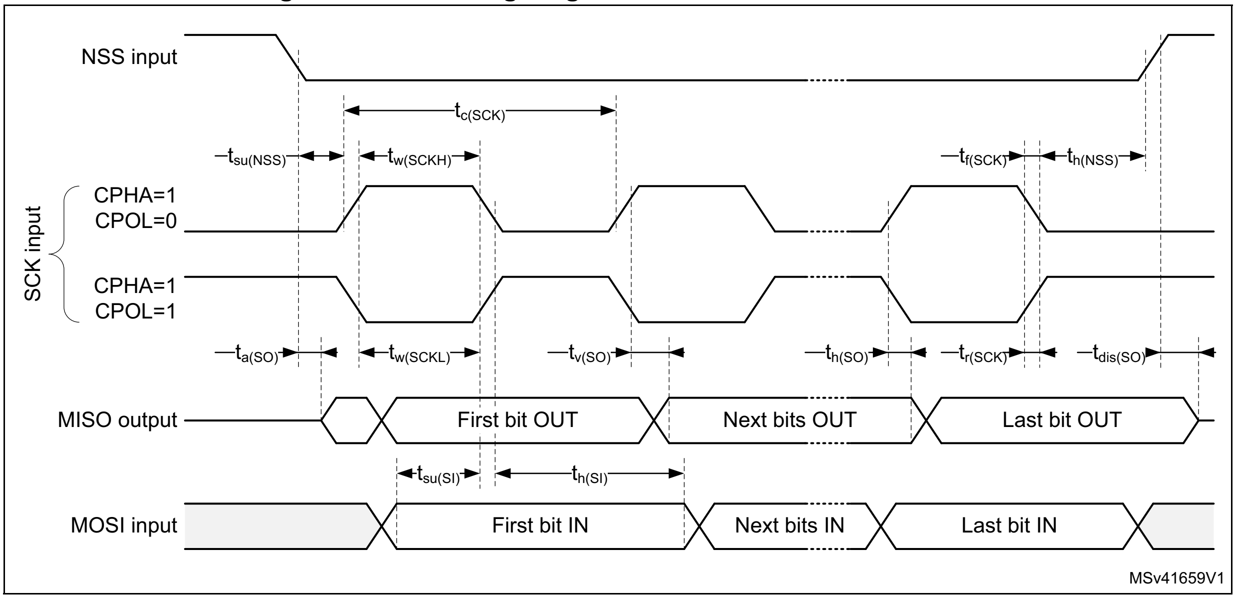
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 95. SPI characteristics[1]

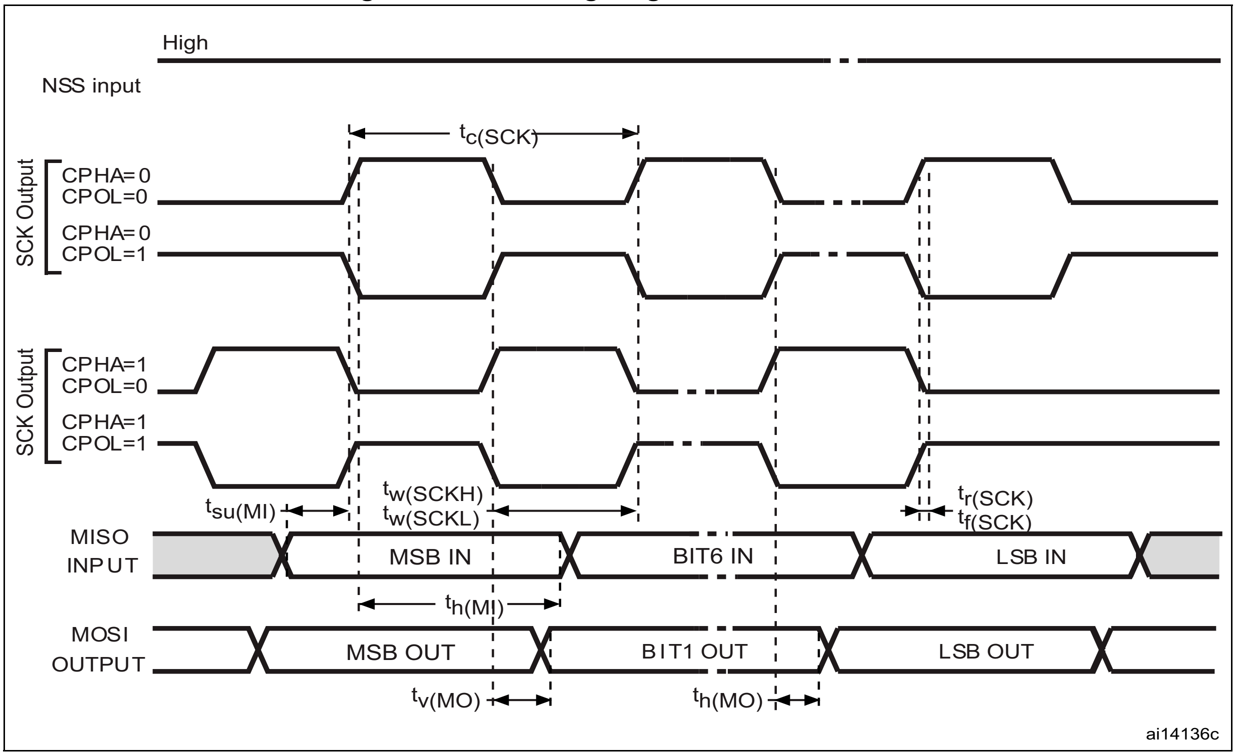
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode receiver/full duplex 2.7 V < V_{DD} < 3.6 V Voltage Range 1	-	-	40	MHz
		Master mode receiver/full duplex 1.71 V < V_{DD} < 3.6 V Voltage Range 1			16	
		Master mode transmitter 1.71 V < V_{DD} < 3.6 V Voltage Range 1			40	
		Slave mode receiver 1.71 V < V_{DD} < 3.6 V Voltage Range 1			40	
		Slave mode transmitter/full duplex 2.7 V < V_{DD} < 3.6 V Voltage Range 1			31[2]	
		Slave mode transmitter/full duplex 1.71 V < V_{DD} < 3.6 V Voltage Range 1			18.5[2]	
		Voltage Range 2			13	
		1.08 V < V_{DDIO2} < 1.32 V[3]			8	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI prescaler = 2	4_xT_{PCLK}	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI prescaler = 2	2_xT_{PCLK}	-	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	T_{PCLK}-2	T_{PCLK}	T_{PCLK}+2	ns
$t_{su(MI)}$	Data input setup time	Master mode	1	-	-	ns
$t_{su(SI)}$		Slave mode	1.5	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	-	ns
$t_{h(SI)}$		Slave mode	1.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	-	34	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	9	-	16	ns

Figure 35. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 36. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 54. NAND controller waveforms for common memory write access

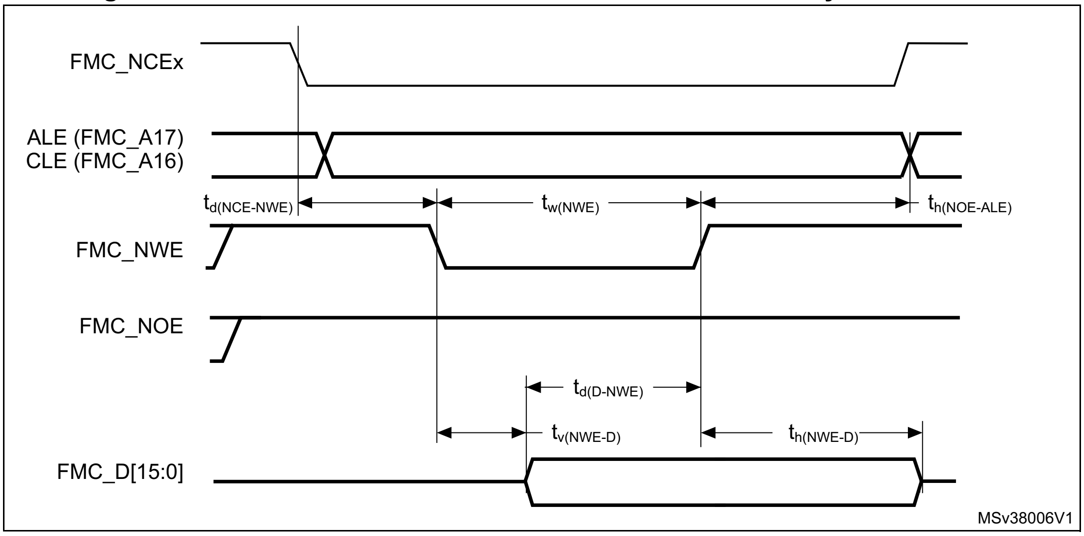


Table 114. Switching characteristics for NAND Flash read cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$T_{w(NOE)}$	FMC_NOE low width	$4T_{HCLK}$-0.5	$4T_{HCLK}$+0.5	ns
$T_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	12	-	
$T_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$T_{d(NCE-NOE)}$	FMC_NCE valid before FMC_NOE low	-	$3T_{HCLK}$+1	
$T_{h(NOE-ALE)}$	FMC_NOE high to FMC_ALE invalid	$4T_{HCLK}$-2	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 115. Switching characteristics for NAND Flash write cycles(1)(2)

Symbol	Parameter	Min	Max	Unit
$T_{w(NWE)}$	FMC_NWE low width	$4T_{HCLK}$-0.5	$4T_{HCLK}$+0.5	ns
$T_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	5	-	
$T_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$2T_{HCLK}$-1	-	
$T_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{HCLK}$-1	-	
$T_{d(NCE\_NWE)}$	FMC_NCE valid before FMC_NWE low	-	$3T_{HCLK}$+1	
$T_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$2T_{HCLK}$-2	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

6.3.30 SWPMI characteristics

The Single Wire Protocol Master Interface (SWPMI) and the associated SWPMI_IO transceiver are compliant with the ETSI TS 102 613 technical specification.

Table 117. SWPMI electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SWPSTART}$	SWPMI regulator startup time	SWP Class B 2.7 V ≤ V_{DD} ≤ 3,3V	-	-	300	µs
t_{SWPBIT}	SWP bit duration	V_{CORE} voltage range 1	500	-	-	ns
		V_{CORE} voltage range 2	620	-	-	

6.3.31 SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in *Table 118* for the SDIO/MMC interface are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DD} supply voltage conditions summarized in *Table 22*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output characteristics.

Figure 56. SDIO high-speed mode

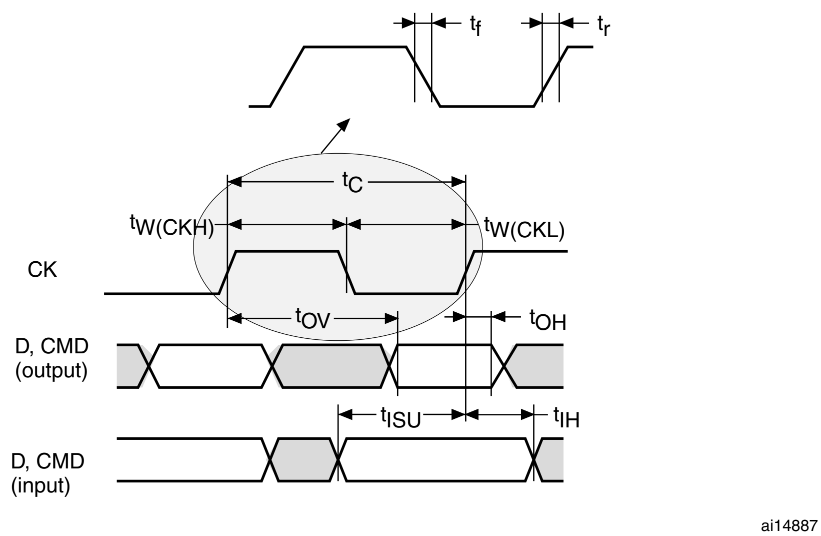


Table 120. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[(1)]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
b	0.230	0.280	0.330	0.0091	0.0110	0.0130
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
D1	5.950	6.000	6.050	0.2343	0.2362	0.2382
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
E1	5.950	6.000	6.050	0.2343	0.2362	0.2382
e	-	0.500	-	-	0.0197	-
F	0.450	0.500	0.550	0.0177	0.0197	0.0217
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 59. UFBGA169 - 169-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array recommended footprint

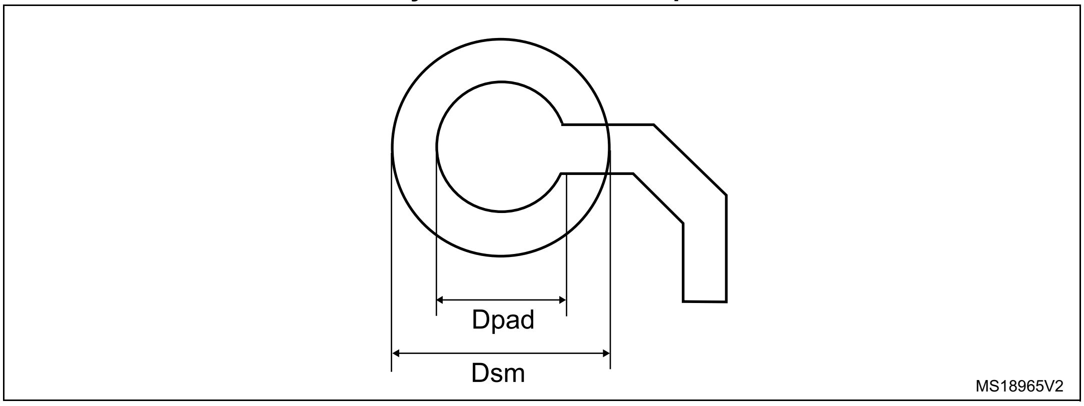


Table 121. UFBGA169 recommended PCB design rules (0.5 mm pitch BGA)

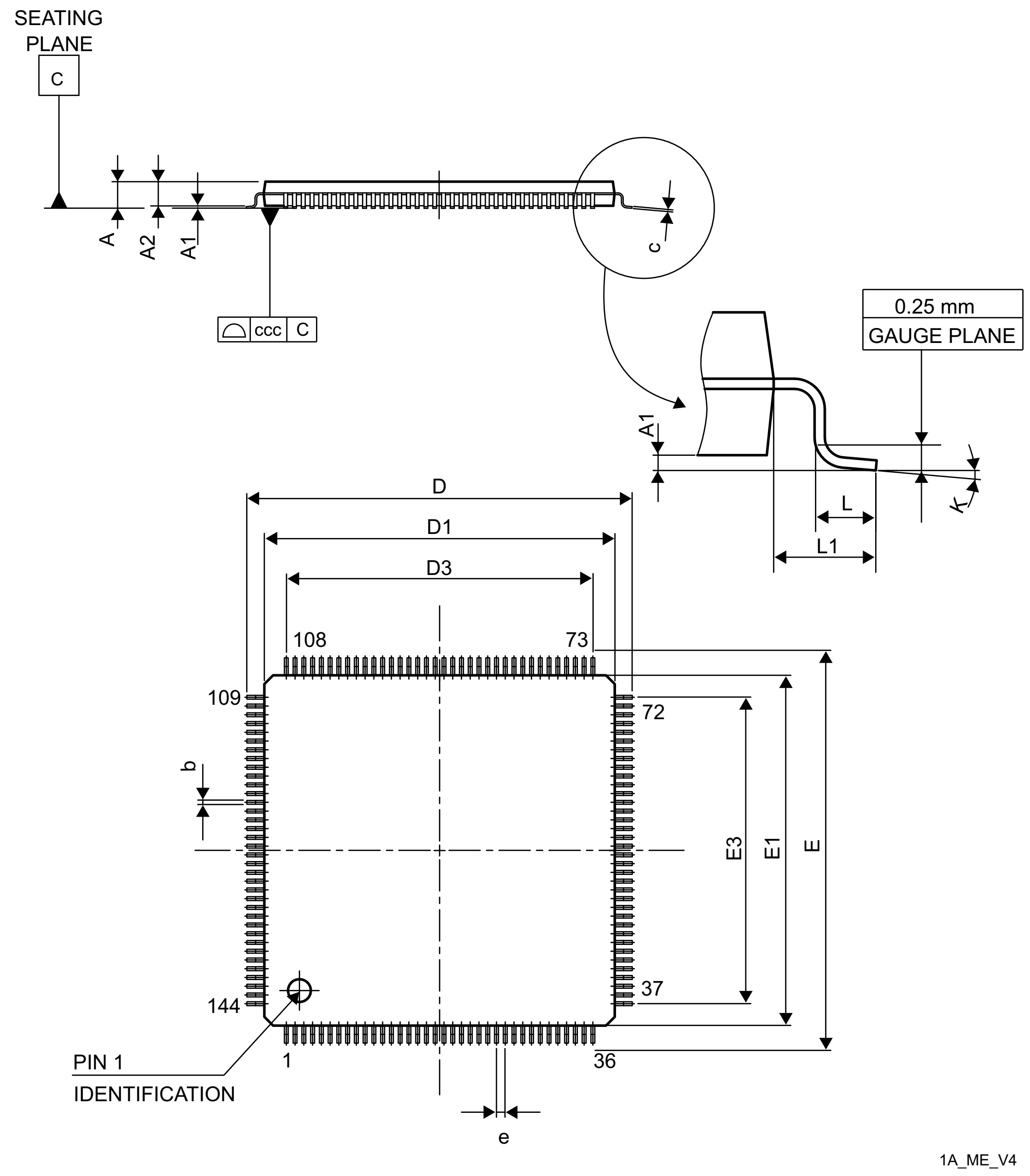
Dimension	Recommended values
Pitch	0.5 mm
Dpad	0.27 mm
Dsm	0.35 mm typ. (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter.

Note: Non-solder mask defined (NSMD) pads are recommended.

Note: 4 to 6 mils solder paste screen printing process.

7.2 LQFP144 package information

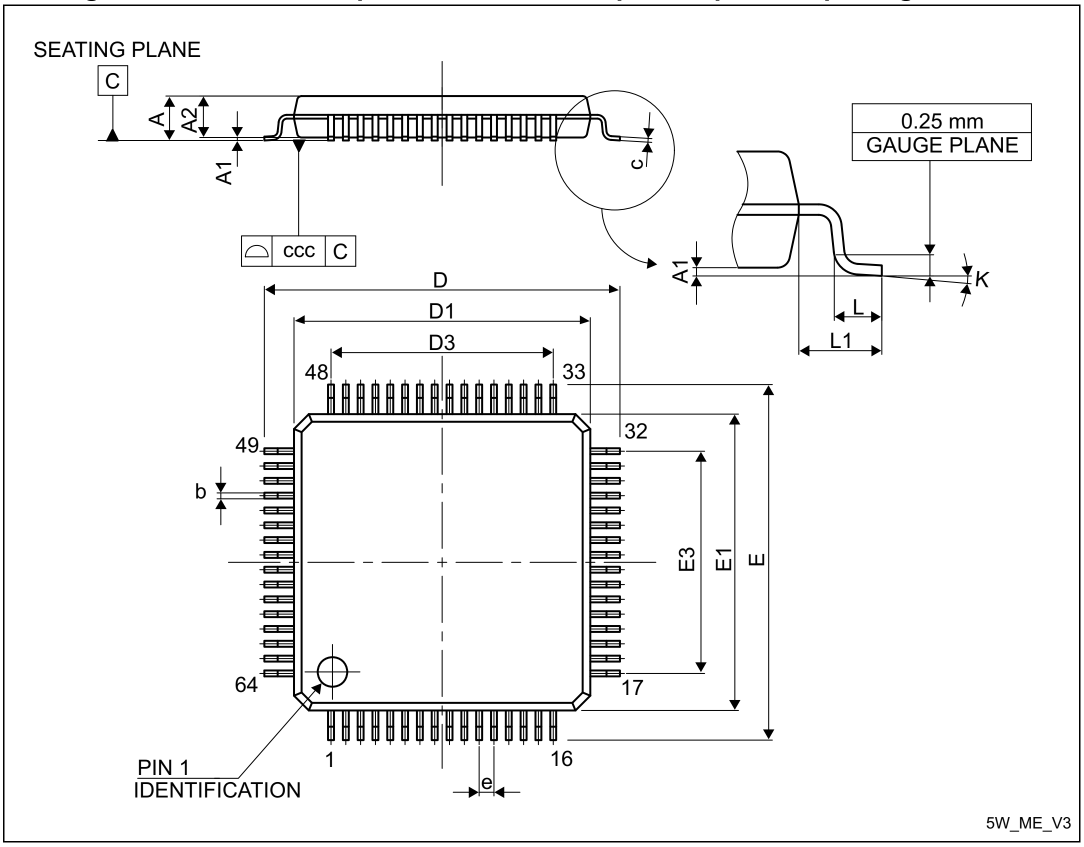
Figure 62. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



1. Drawing is not to scale.

7.6 LQFP64 package information

Figure 76. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 128. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-