STMicroelectronics - STM32L496QGI6P Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	110
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 19x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	132-UFBGA
Supplier Device Package	132-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l496qgi6p

3 Functional overview

3.1 ARM® Cortex®-M4 core with FPU

The ARM® Cortex®-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32L496xx family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32L496xx family devices.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 processors. It balances the inherent performance advantage of the ARM® Cortex®-M4 over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor near 100 DMIPS performance at 80MHz, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 64-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 80 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

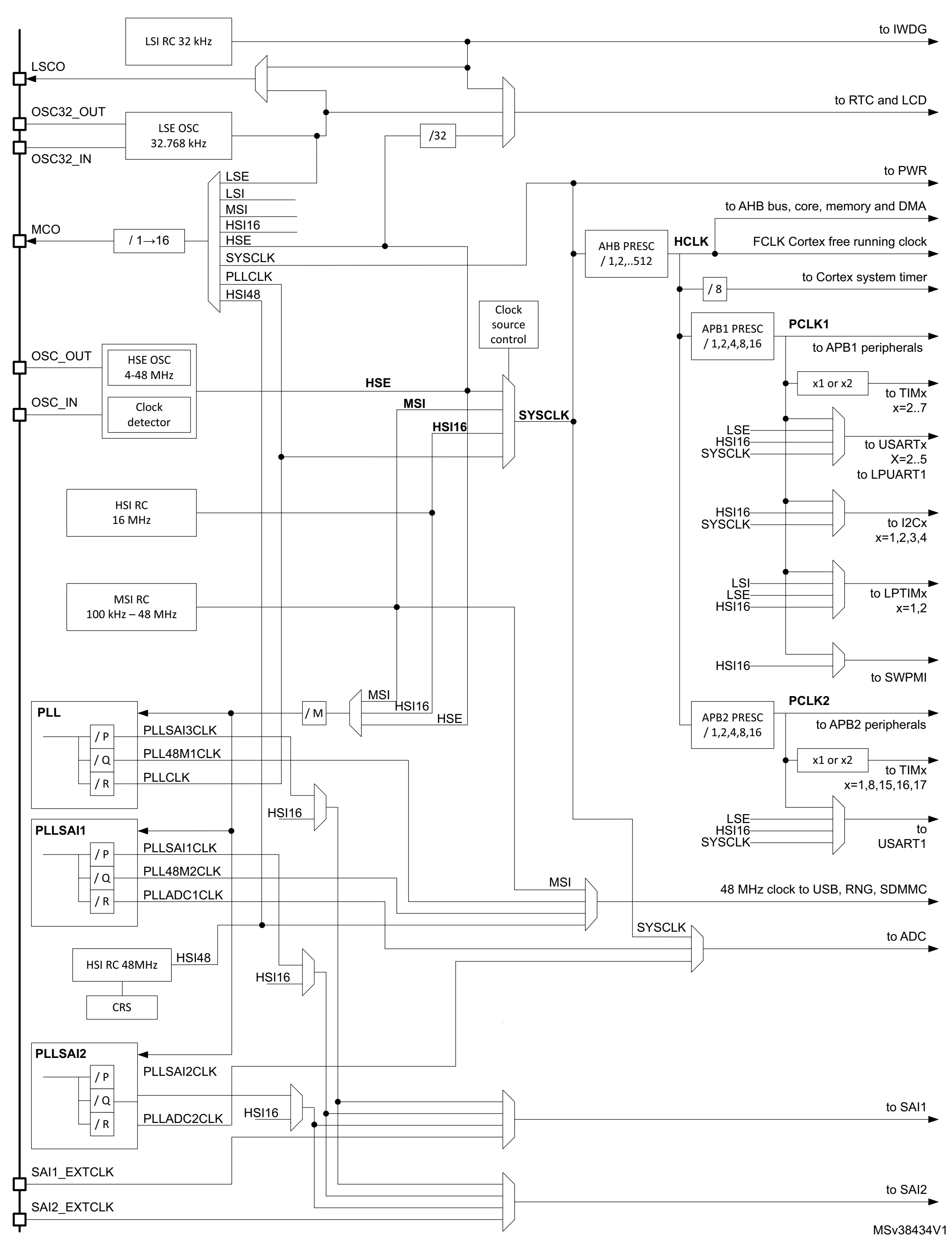


Figure 4. Clock tree

3.13 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.14 Direct memory access controller (DMA)

The device embeds 2 DMAs. Refer to *Table 7: DMA implementation* for the features implementation.

Direct memory access (DMA) is used in order to provide high-speed data transfer between peripherals and memory as well as memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps CPU resources free for other operations.

The two DMA controllers have 14 channels in total, each dedicated to managing memory access requests from one or more peripherals. Each has an arbiter for handling the priority between DMA requests.

The DMA supports:

- 14 independently configurable channels (requests)
- Each channel is connected to dedicated hardware DMA requests, software trigger is also supported on each channel. This configuration is done by software.
- Priorities between requests from channels of one DMA are software programmable (4 levels consisting of very high, high, medium, low) or hardware in case of equality (request 1 has priority over request 2, etc.)
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size.
- Support for circular buffer management
- 3 event flags (DMA Half Transfer, DMA Transfer complete and DMA Transfer Error) logically ORed together in a single interrupt request for each channel
- Memory-to-memory transfer
- Peripheral-to-memory and memory-to-peripheral, and peripheral-to-peripheral transfers
- Access to Flash, SRAM, APB and AHB peripherals as source and destination
- Programmable number of data to be transferred: up to 65536.

Table 7. DMA implementation

DMA features	DMA1	DMA2
Number of regular channels	7	7

3.17 Analog to digital converter (ADC)

The device embeds 3 successive approximation analog-to-digital converters with the following features:

- 12-bit native resolution, with built-in calibration
- 5.33 Msps maximum conversion rate with full resolution
  - Down to 18.75 ns sampling time
  - Increased conversion rate for lower resolution (up to 8.88 Msps for 6-bit resolution)
- Up to 24 external channels, some of them shared between ADC1 and ADC2, or ADC1, ADC2 and ADC3.
- 5 internal channels: internal reference voltage, temperature sensor, VBAT/3, DAC1 and DAC2 outputs.
- One external reference pin is available on some package, allowing the input voltage range to be independent from the power supply
- Single-ended and differential mode inputs
- Low-power design
  - Capable of low-current operation at low conversion rate (consumption decreases linearly with speed)
  - Dual clock domain architecture: ADC speed independent from CPU frequency
- Highly versatile digital interface
  - Single-shot or continuous/discontinuous sequencer-based scan mode: 2 groups of analog signals conversions can be programmed to differentiate background and high-priority real-time conversions
  - Handles two ADC converters for dual mode operation (simultaneous or interleaved sampling modes)
  - Each ADC support multiple trigger inputs for synchronization with on-chip timers and external signals
  - Results stored into 3 data register or in RAM with DMA controller support
  - Data pre-processing: left/right alignment and per channel offset compensation
  - Built-in oversampling unit for enhanced SNR
  - Channel-wise programmable sampling time
  - Three analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers
  - Hardware assistant to prepare the context of the injected channels to allow fast context switching

3.17.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1_IN17 and ADC3_IN17 input channels which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

Table 15. STM32L496xx pin definitions (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP100	WLCSP100_SMPS	LQFP100	UFBGA132	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	-	-	-	D6	10	10	F5	F5	PF0	I/O	FT_f	-	I2C2_SDA, FMC_A0, EVENTOUT	-
-	-	-	-	D5	11	11	F4	F4	PF1	I/O	FT_f	-	I2C2_SCL, FMC_A1, EVENTOUT	-
-	-	-	-	D4	12	12	F3	F3	PF2	I/O	FT	-	I2C2_SMBA, FMC_A2, EVENTOUT	-
-	-	-	-	E4	13	13	G3	G3	PF3	I/O	FT_a	-	FMC_A3, EVENTOUT	ADC3_IN6
-	-	-	-	F3	14	14	G4	G4	PF4	I/O	FT_a	-	FMC_A4, EVENTOUT	ADC3_IN7
-	-	-	-	F4	15	15	G5	G5	PF5	I/O	FT_a	-	FMC_A5, EVENTOUT	ADC3_IN8
-	D9	E10	10	F2	16	16	F2	F2	VSS	S	-	-	-	-
-	E9	E9	11	G2	17	17	G2	G2	VDD	S	-	-	-	-
-	-	-	-	-	18	18	-	-	PF6	I/O	FT_a	-	TIM5_ETR, TIM5_CH1, QUADSPI_BK1_IO3, SAI1_SD_B, EVENTOUT	ADC3_IN9
-	-	-	-	-	19	19	-	-	PF7	I/O	FT_a	-	TIM5_CH2, QUADSPI_BK1_IO2, SAI1_MCLK_B, EVENTOUT	ADC3_IN10
-	-	-	-	-	20	20	-	-	PF8	I/O	FT_a	-	TIM5_CH3, QUADSPI_BK1_IO0, SAI1_SCK_B, EVENTOUT	ADC3_IN11
-	-	-	-	-	21	21	-	-	PF9	I/O	FT_a	-	TIM5_CH4, QUADSPI_BK1_IO1, SAI1_FS_B, TIM15_CH1, EVENTOUT	ADC3_IN12
-	-	-	-	-	22	22	H4	H4	PF10	I/O	FT_a	-	QUADSPI_CLK, DCMI_D11, TIM15_CH2, EVENTOUT	ADC3_IN13

Table 15. STM32L496xx pin definitions (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP100	WLCSP100_SMPS	LQFP100	UFBGA132	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	-	-	60	H12	82	82	K13	K13	PD13	I/O	FT_fl	-	TIM4_CH2, I2C4_SDA, TSC_G6_IO4, LCD_SEG33, FMC_A18, LPTIM2_OUT, EVENTOUT	-
-	-	-	-	-	83	83	H12	H12	VSS	S	-	-	-	-
-	F1	F1	-	-	84	84	H13	H13	VDD	S	-	-	-	-
-	G3	F3	61	H11	85	85	K10	K10	PD14	I/O	FT_l	-	TIM4_CH3, LCD_SEG34, FMC_D0, EVENTOUT	-
-	F4	F2	62	H10	86	86	H11	H11	PD15	I/O	FT_l	-	TIM4_CH4, LCD_SEG35, FMC_D1, EVENTOUT	-
-	-	-	-	G10	87	87	J12	J12	PG2	I/O	FT_s	-	SPI1_SCK, FMC_A12, SAI2_SCK_B, EVENTOUT	-
-	-	-	-	F9	88	88	J11	J11	PG3	I/O	FT_s	-	SPI1_MISO, FMC_A13, SAI2_FS_B, EVENTOUT	-
-	-	-	-	F10	89	89	J10	J10	PG4	I/O	FT_s	-	SPI1_MOSI, FMC_A14, SAI2_MCLK_B, EVENTOUT	-
-	-	-	-	E9	90	90	J9	J9	PG5	I/O	FT_s	-	SPI1_NSS, LPUART1_CTS, FMC_A15, SAI2_SD_B, EVENTOUT	-
-	-	-	-	G4	91	91	G11	G11	PG6	I/O	FT_s	-	I2C3_SMBA, LPUART1_RTS_DE, EVENTOUT	-
-	-	-	-	H4	92	92	H10	H10	PG7	I/O	FT_fs	-	I2C3_SCL, LPUART1_TX, FMC_INT, SAI1_MCLK_A, EVENTOUT	-
-	-	-	-	J6	93	93	H9	H9	PG8	I/O	FT_fs	-	I2C3_SDA, LPUART1_RX, EVENTOUT	-
-	-	-	-	-	94	94	F13	F13	VSS	S	-	-	-	-

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 17*)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/ LPTIM1	TIM1/2/3/4/5	SPI2/USART2/ CAN2/TIM8/ QUADSPI	I2C1/2/3/4/ DCMI	SPI1/2/DCMI/ QUADSPI	SPI3/I2C3/ DFSDM/ COMP1/ QUADSPI	USART1/2/3
Port A	PA0	-	TIM2_CH1	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS
	PA1	-	TIM2_CH2	TIM5_CH2	-	I2C1_SMBA	SPI1_SCK	-	USART2_RTS_ DE
	PA2	-	TIM2_CH3	TIM5_CH3	-	-	-	-	USART2_TX
	PA3	-	TIM2_CH4	TIM5_CH4	-	-	-	-	USART2_RX
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS	USART2_CK
	PA5	-	TIM2_CH1	TIM2_ETR	TIM8_CH1N	-	SPI1_SCK	-	-
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	DCMI_PIXCLK	SPI1_MISO	-	USART3_CTS
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	I2C3_SCL	SPI1_MOSI	-	-
	PA8	MCO	TIM1_CH1	-	-	-	-	-	USART1_CK
	PA9	-	TIM1_CH2	-	SPI2_SCK	I2C1_SCL	DCMI_D0	-	USART1_TX
	PA10	-	TIM1_CH3	-	-	I2C1_SDA	DCMI_D1	-	USART1_RX
	PA11	-	TIM1_CH4	TIM1_BKIN2	-	-	SPI1_MISO	-	USART1_CTS
	PA12	-	TIM1_ETR	-	-	-	SPI1_MOSI	-	USART1_RTS_ DE
	PA13	JTMS/SWDIO	IR_OUT	-	-	-	-	-	-
	PA14	JTCK/SWCLK	LPTIM1_OUT	-	-	I2C1_SMBA	I2C4_SMBA	-	-
	PA15	JTDI	TIM2_CH1	TIM2_ETR	USART2_RX	-	SPI1_NSS	SPI3_NSS	USART3_RTS_ DE

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 16*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 17*.

Figure 16. Pin loading conditions

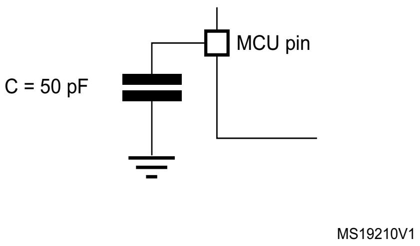
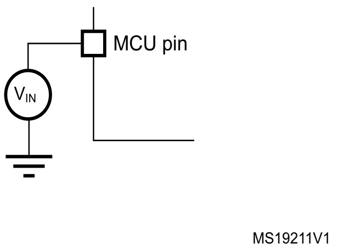


Figure 17. Pin input voltage



6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 23* are derived from tests performed under the ambient temperature condition summarized in *Table 22*.

Table 23. Operating conditions at power-up / power-down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		10	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	µs/V
	V_{DDA} fall time rate		10	∞	
t_{VDDUSB}	V_{DDUSB} rise time rate	-	0	∞	µs/V
	V_{DDUSB} fall time rate		10	∞	
t_{VDDIO2}	V_{DDIO2} rise time rate	-	0	∞	µs/V
	V_{DDIO2} fall time rate		10	∞	

1. At Power up, the VDD12 voltage should not be forced externally

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 24* are derived from tests performed under the ambient temperature conditions summarized in *Table 22: General operating conditions*.

Table 24. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(2)	Reset temporization after BOR0 is detected	V_{DD} rising	-	250	400	µs
V_{BOR0}(2)	Brown-out reset threshold 0	Rising edge	1.62	1.66	1.7	V
		Falling edge	1.6	1.64	1.69	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.06	2.1	2.14	V
		Falling edge	1.96	2	2.04	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.26	2.31	2.35	V
		Falling edge	2.16	2.20	2.24	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{BOR4}	Brown-out reset threshold 4	Rising edge	2.85	2.90	2.95	V
		Falling edge	2.76	2.81	2.86	
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	2.1	2.15	2.19	V
		Falling edge	2	2.05	2.1	
V_{PVD1}	PVD threshold 1	Rising edge	2.26	2.31	2.36	V
		Falling edge	2.15	2.20	2.25	

Table 40. Typical current consumption in Run, with different codesrunning from SRAM1 and power supplied by external SMPS (VDD12 = 1.05 V)

Symbol	Parameter	Conditions[1]			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	f_{HCLK} = 26 MHz	Reduced code[2]	1.07	mA	41	µA/MHz
				Coremark	1.07		41	
				Dhrystone 2.1	1.04		40	
				Fibonacci	0.97		37	
				While(1)	0.93		36	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, VDD12 = 1.05 V
2. Reduced code used for characterization results provided in *Table 26*, *Table 28*, *Table 30*.

Table 44. Current consumption in Stop 2 mode (continued)

Symbol	Parameter	Conditions		TYP					MAX[1]					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL}(Stop 2 with RTC)	Supply current in Stop 2 mode, RTC enabled	RTC clocked by LSI, LCD disabled	1.8 V	2.97	7.46	26.2	61.4	139	6.1	17.2	64.8	155.4	354	µA
			2.4 V	3.09	7.61	26.5	62.3	140	6.2	17.5	65.7	157.6	360	
			3 V	3.15	7.81	27	63.5	144	6.5	17.9	67.2	160.6	367	
			3.6 V	3.4	8.05	27.7	65.2	147	7.1	18.7	69.0	164.9	376	
		RTC clocked by LSI, LCD enabled[3]	1.8 V	2.98	7.31	25.5	60	135	5.5	16.8	65.1	155.8	355	
			2.4 V	3.08	7.46	25.8	60.7	137	5.8	17.1	66.3	158.2	360	
			3 V	3.23	7.63	26.4	62.1	141	6.2	17.5	67.6	161.4	367	
			3.6 V	3.47	7.95	27.1	63.6	144	6.58	18.3	69.5	165.5	376	
		RTC clocked by LSE bypassed at 32768Hz,LCD disabled	1.8 V	2.93	7.22	25.7	60.7	135.6	-	-	-	-	-	
			2.4 V	3.1	7.38	26.1	61.1	137.5	-	-	-	-	-	
			3 V	3.3	7.51	26.4	62.1	140.5	-	-	-	-	-	
			3.6 V	3.48	7.87	27.1	63.6	143.5	-	-	-	-	-	
		RTC clocked by LSE quartz[3] in low drive mode, LCD disabled	1.8 V	2.86	7.08	25.2	60.4	-	-	-	-	-	-	
			2.4 V	3.01	7.16	25.5	60.9	-	-	-	-	-	-	
			3 V	3.18	7.25	25.8	61.8	-	-	-	-	-	-	
			3.6 V	3.31	7.54	26.5	63.2	-	-	-	-	-	-	

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 70* are derived from tests performed under the conditions summarized in *Table 22: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Table 70. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}(1)	I/O input low level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	-	-	0.3xV_{DDIOx} (2)	V
	I/O input low level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	-	-	0.39xV_{DDIOx}-0.06 (3)	
	I/O input low level voltage except BOOT0	1.08 V<V_{DDIOx}<1.62 V	-	-	0.43xV_{DDIOx}-0.1 (3)	
	BOOT0 I/O input low level voltage	1.62 V<V_{DDIOx}<3.6 V	-	-	0.17xV_{DDIOx} (3)	
V_{IH}(1)	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	0.7xV_{DDIOx} (2)	-	-	V
	I/O input high level voltage except BOOT0	1.62 V<V_{DDIOx}<3.6 V	0.49xV_{DDIOX}+0.26 (3)	-	-	
	I/O input high level voltage except BOOT0	1.08 V<V_{DDIOx}<1.62 V	0.61xV_{DDIOX}+0.05 (3)	-	-	
	BOOT0 I/O input high level voltage	1.62 V<V_{DDIOx}<3.6 V	0.77xV_{DDIOX} (3)	-	-	
V_{hys}(3)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.62 V<V_{DDIOx}<3.6 V	-	200	-	mV
	FT_sx	1.08 V<V_{DDIOx}<1.62 V	-	150	-	
	BOOT0 I/O input hysteresis	1.62 V<V_{DDIOx}<3.6 V	-	200	-	

Table 76. Maximum ADC RAIN[(1)(2)] (continued)

Resolution	Sampling cycle @80 MHz	Sampling time [ns] @80 MHz	RAIN max (Ω)	
			Fast channels[(3)]	Slow channels[(4)]
6 bits	2.5	31.25	220	N/A
	6.5	81.25	560	330
	12.5	156.25	1200	1000
	24.5	306.25	2700	2200
	47.5	593.75	3900	3300
	92.5	1156.25	8200	6800
	247.5	3093.75	18000	15000
	640.5	8006.75	50000	50000

1. Guaranteed by design.
2. The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4$ V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4$V). It is disable when $V_{DDA} \geq 2.4$ V.
3. Fast channels are: PC0, PC1, PC2, PC3, PA0.
4. Slow channels are: all ADC inputs except the fast channels.

Table 79. ADC accuracy - limited test conditions 3(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	5.5	7.5	LSB
				Slow channel (max speed)	-	4.5	6.5	
			Differential	Fast channel (max speed)	-	4.5	7.5	
				Slow channel (max speed)	-	4.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	5	
				Slow channel (max speed)	-	2.5	5	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	4.5	7	
				Slow channel (max speed)	-	3.5	6	
			Differential	Fast channel (max speed)	-	3.5	4	
				Slow channel (max speed)	-	3.5	5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1.2	1.5	
				Slow channel (max speed)	-	1.2	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	3	3.5	
				Slow channel (max speed)	-	2.5	3.5	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.4	-	bits
				Slow channel (max speed)	10	10.4	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	64	-	dB
				Slow channel (max speed)	62	64	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	63	65	-	
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

6.3.19 Voltage reference buffer characteristics

Table 83. VREFBUF characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	$V_{RS} = 0$	2.4	-	3.6	V
			$V_{RS} = 1$	2.8	-	3.6	
		Degraded mode(2)	$V_{RS} = 0$	1.65	-	2.4	
			$V_{RS} = 1$	1.65	-	2.8	
V_{REFBUF_OUT}	Voltage reference output	Normal mode	$V_{RS} = 0$	2.046(3)	2.048	2.049(3)	
			$V_{RS} = 1$	2.498(3)	2.5	2.502(3)	
		Degraded mode(2)	$V_{RS} = 0$	V_{DDA}-150 mV	-	V_{DDA}	
			$V_{RS} = 1$	V_{DDA}-150 mV	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
CL	Load capacitor	-	-	0.5	1	1.5	µF
esr	Equivalent Serial Resistor of Cload	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	1000	ppm/V
			I_{load} = 4 mA	-	100	500	
I_{load_reg}	Load regulation	500 µA ≤ I_{load} ≤4 mA	Normal mode	-	50	500	ppm/mA
T_{Coeff}	Temperature coefficient	-40 °C < TJ < +125 °C		-	-	$T_{coeff\_vrefint}$ + 50	ppm/ °C
		0 °C < TJ < +50 °C		-	-	$T_{coeff\_vrefint}$ + 50	
PSRR	Power supply rejection	DC		40	60	-	dB
		100 kHz		25	40	-	
t_{START}	Start-up time	CL = 0.5 µF(4)		-	300	350	µs
		CL = 1.1 µF(4)		-	500	650	
		CL = 1.5 µF(4)		-	650	800	
I_{INRUSH}	Control of maximum DC current drive on VREFBUF_OUT during start-up phase (5)	-	-	-	8	-	mA

Table 83. VREFBUF characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDA}(VREF BUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA	-	16	25	µA
		I_{load} = 500 µA	-	18	30	
		I_{load} = 4 mA	-	35	50	

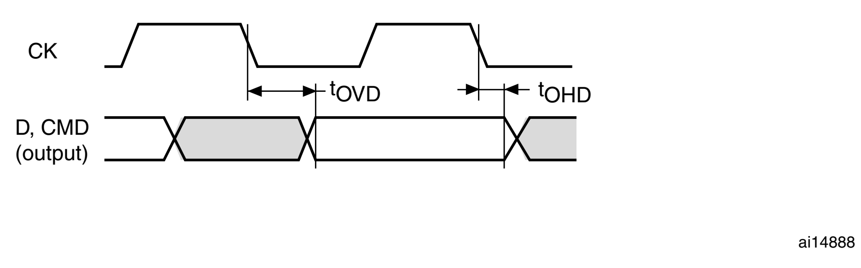
1. Guaranteed by design, unless otherwise specified.
2. In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which will follow (V_{DDA} - drop voltage).
3. Guaranteed by test in production.
4. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.
5. To correctly control the VREFBUF inrush current during start-up phase and scaling change, the V_{DDA} voltage should be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 1.

6.3.20 Comparator characteristics

Table 84. COMP characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	
V_{BG}(2)	Scaler input voltage	-		V_{REFINT}			
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	200	300	nA
		BRG_EN=1 (bridge enable)		-	0.8	1	µA
t_{START_SCALER}	Scaler startup time	-		-	100	200	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	$V_{DDA} \geq 2.7$ V	-	-	5	µs
			$V_{DDA} < 2.7$ V	-	-	7	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	-	15	
			$V_{DDA} < 2.7$ V	-	-	25	
		Ultra-low-power mode		-	-	80	
t_D(3)	Propagation delay for 200 mV step with 100 mV overdrive	High-speed mode	$V_{DDA} \geq 2.7$ V	-	55	80	ns
			$V_{DDA} < 2.7$ V	-	65	100	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	0.55	0.9	µs
			$V_{DDA} < 2.7$ V	-	0.65	1	
		Ultra-low-power mode		-	5	12	
V_{offset}	Comparator offset error	Full common mode range	-	-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	8	-	
		Medium hysteresis		-	15	-	
		High hysteresis		-	27	-	

Figure 42. SD default mode



USB characteristics

The STM32L496xx USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-speed device operation).

Table 101. USB electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDUSB}	USB transceiver operating voltage		3.0[1]	-	3.6	V
R_{PUI}	Embedded USB_DP pull-up value during idle		900	1250	1600	Ω
R_{PUR}	Embedded USB_DP pull-up value during reception		1400	2300	3200	
Z_{DRV}[2]	Output driver impedance[3]	Driving high and low	28	36	44	Ω

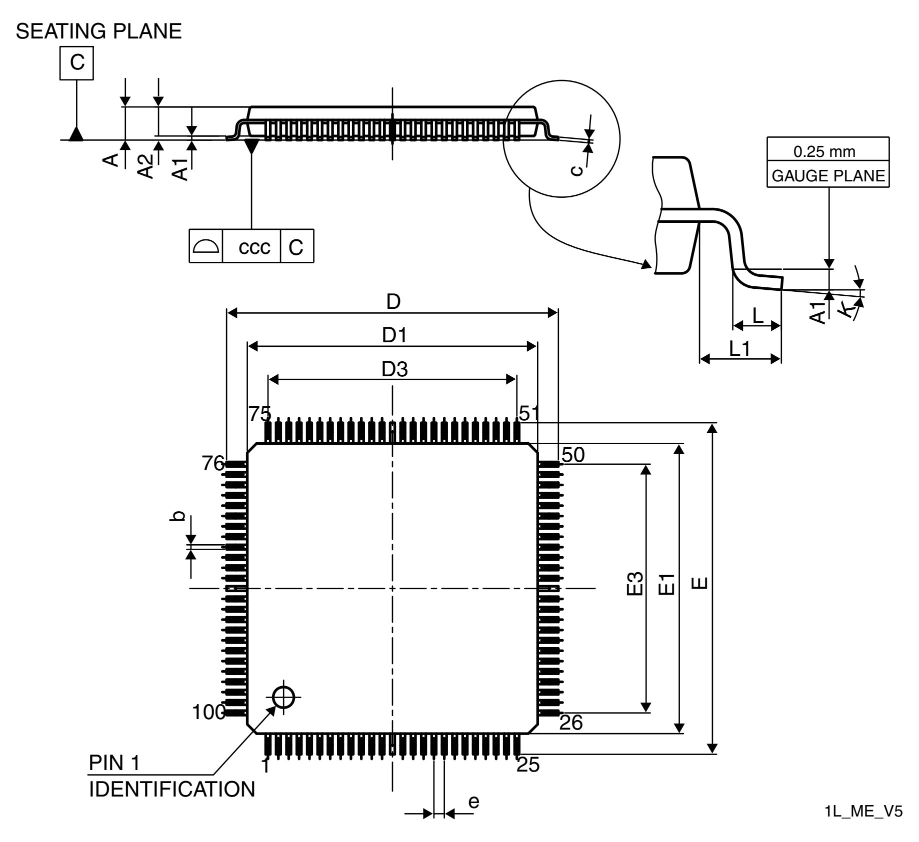
1. The STM32L496xx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V voltage range.
2. Guaranteed by design.
3. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

7.4 LQFP100 package information

Figure 69. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 125. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378