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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	52
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l496rgt6

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The synchronization for this oscillator can also be taken from the USB data stream itself (SOF signalization) which allows crystal less operation.

The major features are:

- Combined Rx and Tx FIFO size of 1.25 KB with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 1 bidirectional control endpoint + 5 IN endpoints + 5 OUT endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- Software configurable to OTG 1.3 and OTG 2.0 modes of operation
- OTG 2.0 Supports ADP (Attach detection Protocol)
- USB 2.0 LPM (Link Power Management) support
- Battery Charging Specification Revision 1.2 support
- Internal FS OTG PHY support

For OTG/Host modes, a power switch is needed in case bus-powered devices are connected.

3.38 Clock recovery system (CRS)

The STM32L496xx devices embed a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.39 Flexible static memory controller (FSMC)

The Flexible static memory controller (FSMC) includes two memory controllers:

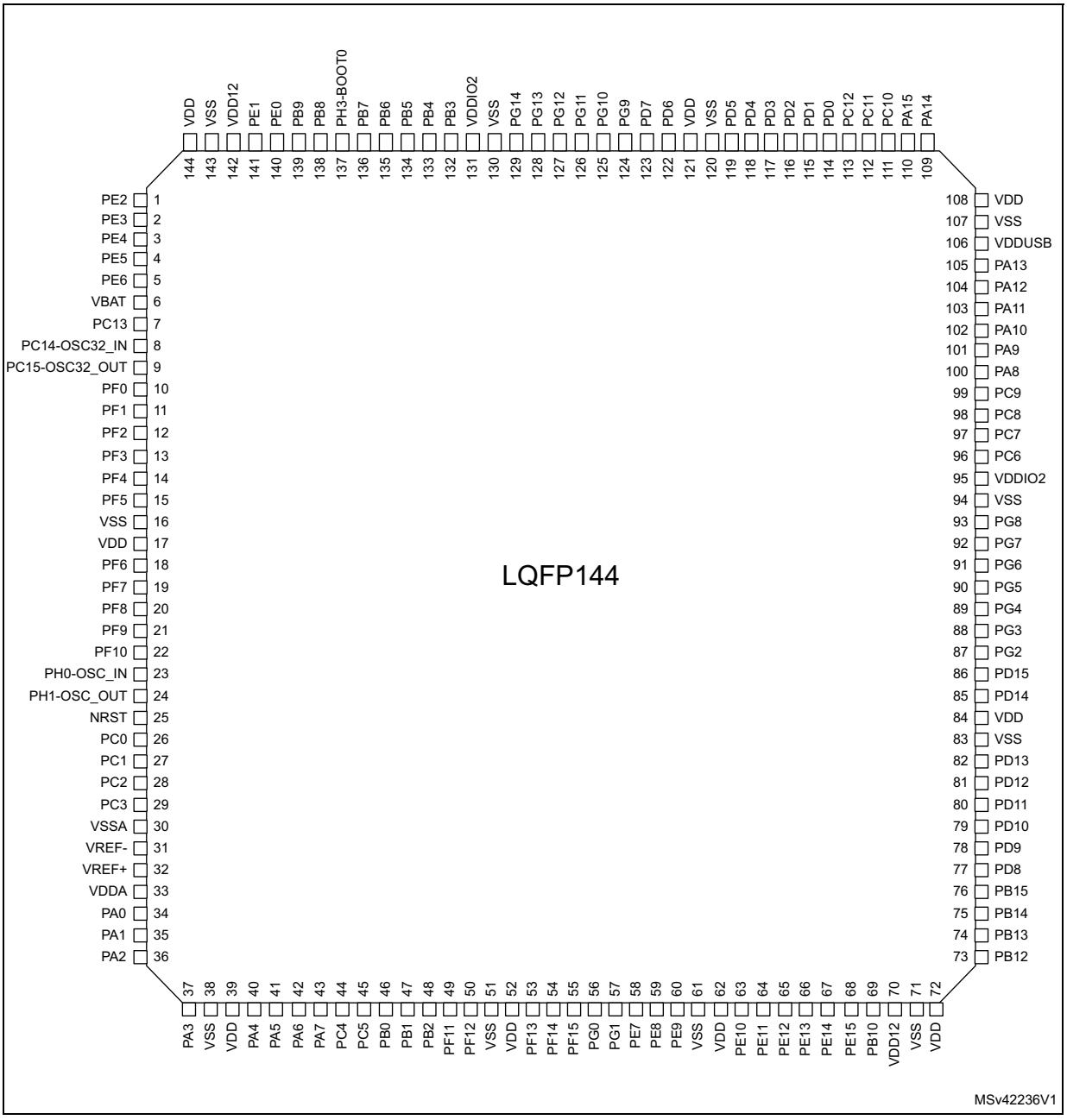
- The NOR/PSRAM memory controller
- The NAND/memory controller

This memory controller is also named Flexible memory controller (FMC).

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM (4 memory banks)
  - NAND Flash memory with ECC hardware to check up to 8 Kbyte of data
- 8-,16- bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- The Maximum FMC_CLK frequency for synchronous accesses is HCLK/2.

Figure 9. STM32L496Zx, external SMPS device, LQFP144 pinout(1)



1. The above figure shows the package top view.

Table 15. STM32L496xx pin definitions (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP100	WLCSP100_SMPS	LQFP100	UFBGA132	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
22	K9	K9	31	L4	42	42	M4	M4	PA6	I/O	FT_la	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, DCMI_PIXCLK, SPI1_MISO, USART3_CTS, LPUART1_CTS, QUADSPI_BK1_IO3, LCD_SEG3, TIM1_BKIN_COMP2, TIM8_BKIN_COMP2, TIM16_CH1, EVENTOUT	OPAMP2_VINP, ADC12_IN11
-	-	-	-	M4	-	-	N4	N4	OPAMP2_VINM	I	TT	-	-	-
23	J7	G6	32	J5	43	43	L4	L4	PA7	I/O	FT_fla	(1)	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, I2C3_SCL, SPI1_MOSI, QUADSPI_BK1_IO2, LCD_SEG4, TIM17_CH1, EVENTOUT	OPAMP2_VINM, ADC12_IN12
24	H6	K8	33	K5	44	44	H5	H5	PC4	I/O	FT_la	-	USART3_TX, QUADSPI_BK2_IO3, LCD_SEG22, EVENTOUT	COMP1_INM, ADC12_IN13
25	K8	-	34	L5	45	45	J5	J5	PC5	I/O	FT_la	-	USART3_RX, LCD_SEG23, EVENTOUT	COMP1_INP, ADC12_IN14, WKUP5
26	J6	H6	35	M5	46	46	K5	K5	PB0	I/O	TT_la	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, SPI1_NSS, USART3_CK, QUADSPI_BK1_IO1, LCD_SEG5, COMP1_OUT, SAI1_EXTCLK, EVENTOUT	OPAMP2_VOUT, ADC12_IN15
27	K7	K7	36	M6	47	47	L5	L5	PB1	I/O	FT_la	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN0, USART3_RTS_DE, LPUART1_RTS_DE, QUADSPI_BK1_IO0, LCD_SEG6, LPTIM2_IN1, EVENTOUT	COMP1_INM, ADC12_IN16
28	F5	J6	37	L6	48	48	N5	N5	PB2	I/O	FT_la	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, DFSDM1_CKIN0, LCD_VLCD, EVENTOUT	COMP1_INP
-	-	-	-	K6	49	49	M5	M5	PF11	I/O	FT	-	DCMI_D12, EVENTOUT	-

Table 15. STM32L496xx pin definitions (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP100	WLCSP100_SMPS	LQFP100	UFBGA132	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	H5	H5	41	L8	63	63	H7	H7	PE10	I/O	FT	-	TIM1_CH2N, DFSDM1_DATIN4, TSC_G5_IO1, QUADSPI_CLK, FMC_D7, SAI1_MCLK_B, EVENTOUT	-
-	K4	K4	42	M9	64	64	N8	N8	PE11	I/O	FT	-	TIM1_CH2, DFSDM1_CKIN4, TSC_G5_IO2, QUADSPI_BK1_NCS, FMC_D8, EVENTOUT	-
-	G5	J4	43	L9	65	65	M8	M8	PE12	I/O	FT	-	TIM1_CH3N, SPI1_NSS, DFSDM1_DATIN5, TSC_G5_IO3, QUADSPI_BK1_IO0, FMC_D9, EVENTOUT	-
-	G4	G5	44	M10	66	66	L8	L8	PE13	I/O	FT	-	TIM1_CH3, SPI1_SCK, DFSDM1_CKIN5, TSC_G5_IO4, QUADSPI_BK1_IO1, FMC_D10, EVENTOUT	-
-	J4	G4	45	M11	67	67	K8	K8	PE14	I/O	FT	-	TIM1_CH4, TIM1_BKIN2, TIM1_BKIN2_COMP2, SPI1_MISO, QUADSPI_BK1_IO2, FMC_D11, EVENTOUT	-
-	H4	H4	46	M12	68	68	J8	J8	PE15	I/O	FT	-	TIM1_BKIN, TIM1_BKIN_COMP1, SPI1_MOSI, QUADSPI_BK1_IO3, FMC_D12, EVENTOUT	-
29	K3	K3	47	L10	69	69	N9	N9	PB10	I/O	FT_fl	-	TIM2_CH3, I2C4_SCL, I2C2_SCL, SPI2_SCK, DFSDM1_DATIN7, USART3_TX, LPUART1_RX, TSC_SYNC, QUADSPI_CLK, LCD_SEG10, COMP1_OUT, SAI1_SCK_A, EVENTOUT	-
30	J3	J3	48	L11	70	-	H8	H8	PB11	I/O	FT_fl	-	TIM2_CH4, I2C4_SDA, I2C2_SDA, DFSDM1_CKIN7, USART3_RX, LPUART1_TX, QUADSPI_BK1_NCS, LCD_SEG11, COMP2_OUT, EVENTOUT	-
-	-	K1	-	-	-	70	-	M10	VDD12	S	-	-	-	-

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 17*) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/ LPTIM1	TIM1/2/3/4/5	SPI2/USART2/ CAN2/TIM8/ QUADSPI	I2C1/2/3/4/ DCMI	SPI1/2/DCMI/ QUADSPI	SPI3/I2C3/ DFSDM/ COMP1/ QUADSPI	USART1/2/3
Port C	PC0	-	LPTIM1_IN1	I2C4_SCL	-	I2C3_SCL	-	DFSDM1_ DATIN4	-
	PC1	TRACED0	LPTIM1_OUT	I2C4_SDA	SPI2_MOSI	I2C3_SDA	-	DFSDM1_CKIN4	-
	PC2	-	LPTIM1_IN2	-	-	-	SPI2_MISO	DFSDM1_ CKOUT	-
	PC3	-	LPTIM1_ETR	-	-	-	SPI2_MOSI	-	-
	PC4	-	-	-	-	-	-	-	USART3_TX
	PC5	-	-	-	-	-	-	-	USART3_RX
	PC6	-	-	TIM3_CH1	TIM8_CH1	-	-	DFSDM1_CKIN3	-
	PC7	-	-	TIM3_CH2	TIM8_CH2	-	-	DFSDM1_ DATIN3	-
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-
	PC9	-	TIM8_BKIN2	TIM3_CH4	TIM8_CH4	DCMI_D3	-	I2C3_SDA	-
	PC10	TRACED1	-	-	-	-	-	SPI3_SCK	USART3_TX
	PC11	-	-	-	-	-	QUADSPI_BK 2_NCS	SPI3_MISO	USART3_RX
	PC12	TRACED3	-	-	-	-	-	SPI3_MOSI	USART3_CK
	PC13	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 17*) (continued)

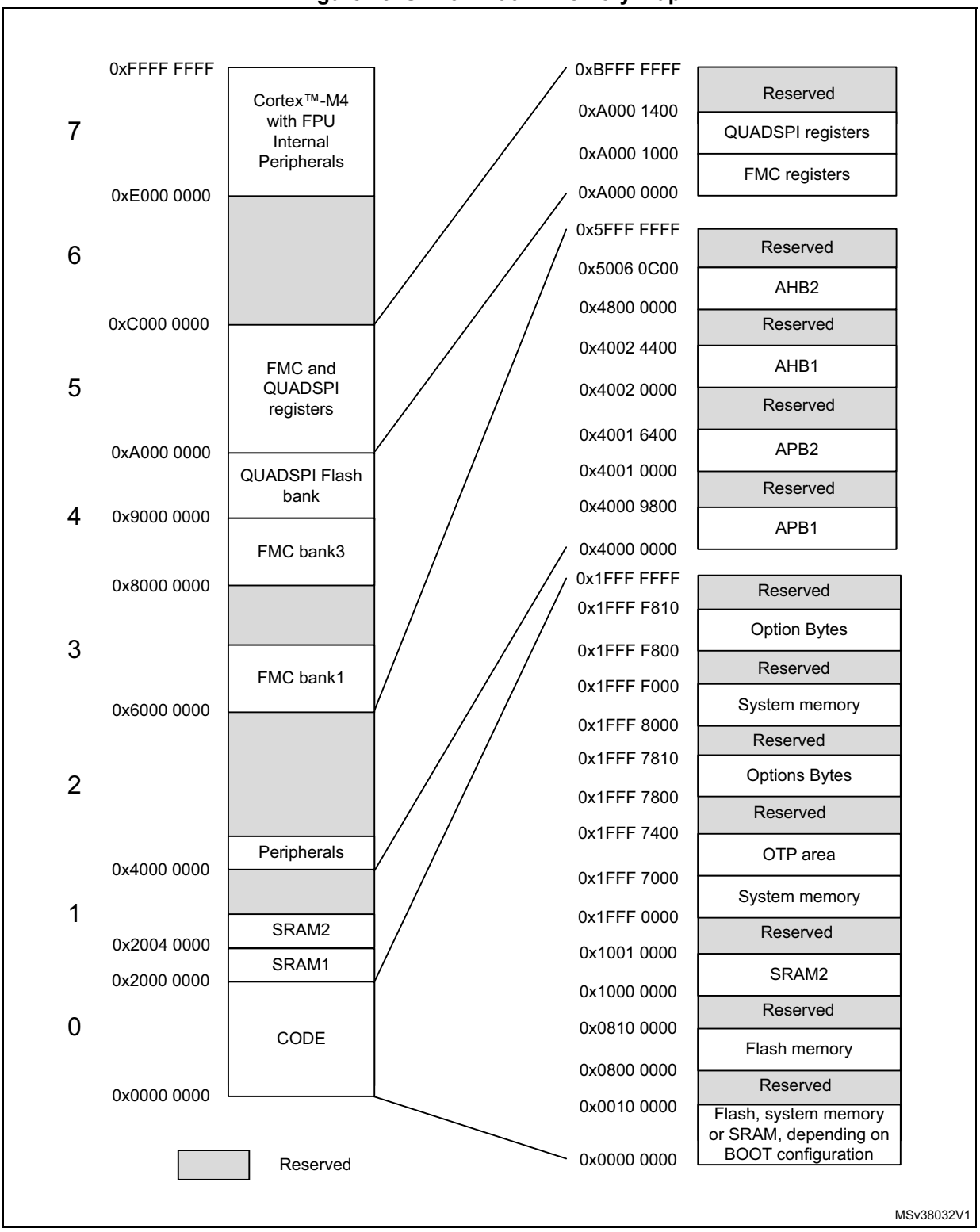
Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/ LPTIM1	TIM1/2/3/4/5	SPI2/USART2/ CAN2/TIM8/ QUADSPI	I2C1/2/3/4/ DCMI	SPI1/2/DCMI/ QUADSPI	SPI3/I2C3/ DFSDM/ COMP1/ QUADSPI	USART1/2/3
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-
	PE1	-	-	-	-	-	-	-	-
	PE2	TRACECK	-	TIM3_ETR	-	-	-	-	-
	PE3	TRACED0	-	TIM3_CH1	-	-	-	-	-
	PE4	TRACED1	-	TIM3_CH2	-	-	-	DFSDM1_ DATIN3	-
	PE5	TRACED2	-	TIM3_CH3	-	-	-	DFSDM1_CKIN3	-
	PE6	TRACED3	-	TIM3_CH4	-	-	-	-	-
	PE7	-	TIM1_ETR	-	-	-	-	DFSDM1_ DATIN2	-
	PE8	-	TIM1_CH1N	-	-	-	-	DFSDM1_CKIN2	-
	PE9	-	TIM1_CH1	-	-	-	-	DFSDM1_ CKOUT	-
	PE10	-	TIM1_CH2N	-	-	-	-	DFSDM1_ DATIN4	-
	PE11	-	TIM1_CH2	-	-	-	-	DFSDM1_CKIN4	-
	PE12	-	TIM1_CH3N	-	-	-	SPI1_NSS	DFSDM1_ DATIN5	-
	PE13	-	TIM1_CH3	-	-	-	SPI1_SCK	DFSDM1_CKIN5	-
	PE14	-	TIM1_CH4	TIM1_BKIN2	TIM1_BKIN2_ COMP2	-	SPI1_MISO	-	-
	PE15	-	TIM1_BKIN	-	TIM1_BKIN_ COMP1	-	SPI1_MOSI	-	-

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 16*)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	CAN2/ OTG_FS/DCMI/ QUADSPI	LCD	SDMMC/ COMP1/2/FMC/SWPMI1	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port A	PA0	UART4_TX	-	-	-	-	SAI1_EXTCLK	TIM2_ETR	EVENTOUT
	PA1	UART4_RX	-	-	LCD_SEG0	-	-	TIM15_CH1N	EVENTOUT
	PA2	LPUART1_TX	-	QUADSPI_BK1_NCS	LCD_SEG1	-	SAI2_EXTCLK	TIM15_CH1	EVENTOUT
	PA3	LPUART1_RX	-	QUADSPI_CLK	LCD_SEG2	-	SAI1_MCLK_A	TIM15_CH2	EVENTOUT
	PA4	-	-	DCMI_HSYNC	-	-	SAI1_FS_B	LPTIM2_OUT	EVENTOUT
	PA5	-	-	-	-	-	-	LPTIM2_ETR	EVENTOUT
	PA6	LPUART1_CTS	-	QUADSPI_BK1_IO3	LCD_SEG3	TIM1_BKIN_COMP2	TIM8_BKIN_COMP2	TIM16_CH1	EVENTOUT
	PA7	-	-	QUADSPI_BK1_IO2	LCD_SEG4	-	-	TIM17_CH1	EVENTOUT
	PA8	-	-	OTG_FS_SOF	LCD_COM0	SWPMI1_IO	SAI1_SCK_A	LPTIM2_OUT	EVENTOUT
	PA9	-	-	-	LCD_COM1	-	SAI1_FS_A	TIM15_BKIN	EVENTOUT
	PA10	-	-	OTG_FS_ID	LCD_COM2	-	SAI1_SD_A	TIM17_BKIN	EVENTOUT
	PA11	-	CAN1_RX	OTG_FS_DM	-	TIM1_BKIN2_COMP1	-	-	EVENTOUT
	PA12	-	CAN1_TX	OTG_FS_DP	-	-	-	-	EVENTOUT
	PA13	-	-	OTG_FS_NOE	-	SWPMI1_TX	SAI1_SD_B	-	EVENTOUT
	PA14	-	-	OTG_FS_SOF	-	SWPMI1_RX	SAI1_FS_B	-	EVENTOUT
	PA15	UART4_RTS_DE	TSC_G3_IO1	-	LCD_SEG17	SWPMI1_SUSPEND	SAI2_FS_B	-	EVENTOUT

5 Memory mapping

Figure 15. STM32L496xx memory map



6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 16*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 17*.

Figure 16. Pin loading conditions

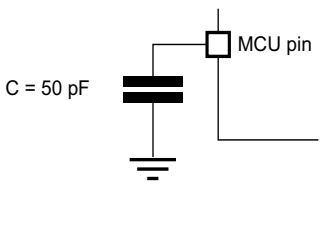


Figure 17. Pin input voltage

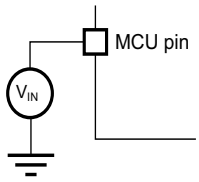


Table 19. Voltage characteristics(1)

Symbol	Ratings		Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}, V_{BAT})		-0.3	4.0	V
VDD12 - VSS	External SMPS supply voltage	Range 1	-0.3	1.32	
		Range 2	-0.3		
V_{IN}(2)	Input voltage on FT_xxx pins		V_{SS}-0.3	min (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}) + 4.0(3)(4)	
	Input voltage on TT_xx pins		V_{SS}-0.3	4.0	
	Input voltage on BOOT0 pin		V_{SS}	9.0	
	Input voltage on any other pins		V_{SS}-0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DDX} power pins of the same domain		-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins(5)		-	50	mV

1. All main power (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 20: Current characteristics* for the maximum allowed injected current values.
3. This formula has to be applied only on the power supplies related to the IO structure described in the pin definition table.
4. To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled.
5. Include VREF- pin.

Table 20. Current characteristics

Symbol	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)(1) (2)	150	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	150	
$IV_{DD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)(2)	100	
$IV_{SS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20	
	Output current sunk by any FT_f pin	20	
	Output current sourced by any I/O and control pin	20	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(3)	100	
	Total output current sourced by sum of all I/Os and control pins(3)	100	
$I_{INJ(PIN)}$(4)	Injected current on FT_xxx, TT_xx, RST and B pins, except PA4, PA5	-5/+0(5)	
	Injected current on PA4, PA5	-5/0	
$\Sigma\lvert I_{INJ(PIN)}\rvert$	Total injected current (sum of all I/Os and control pins)(6)	25	

1. All main power (V_{DD}, V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}, V_{BAT}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. Valid also for VDD12 on SMPS Package

3. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
4. Positive injection (when $V_{IN} > V_{DDIOx}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 19: Voltage characteristics* for the minimum allowed input voltage values.
6. When several inputs are submitted to a current injection, the maximum $\sum|I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 21. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 22. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	80	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	80	
f_{PCLK2}	Internal APB2 clock frequency	-	0	80	
V_{DD}	Standard operating voltage	-	1.71 (1)	3.6	V
VDD12	Standard operating voltage	full frequency range	1.08	1.32	
		up to 26MHz	1.05		
V_{DDIO2}	PG[15:2] I/Os supply voltage	At least one I/O in PG[15:2] used	1.08	3.6	V
		PG[15:2] not used	0	3.6	
V_{DDA}	Analog supply voltage	ADC or COMP used	1.62	3.6	V
		DAC or OPAMP used	1.8		
		VREFBUF used	2.4		
		ADC, DAC, OPAMP, COMP, VREFBUF not used	0		

Table 42. Current consumption in Sleep, Flash ON and power supplied by external SMPS (VDD12 = 1.10 V)

Symbol	Parameter	Conditions[1]		TYP					Unit
		-	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL}(Sleep)	Supply current in sleep mode,	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode pll ON above 48 MHz all peripherals disable	80 MHz	0.92	0.94	0.99	1.08	1.27	mA
			72 MHz	0.84	0.86	0.91	1.00	1.18	
			64 MHz	0.75	0.77	0.82	0.91	1.10	
			48 MHz	0.57	0.59	0.64	0.73	0.91	
			32 MHz	0.40	0.41	0.47	0.55	0.74	
			24 MHz	0.31	0.33	0.38	0.47	0.65	
			16 MHz	0.23	0.24	0.29	0.38	0.56	
			8 MHz	0.14	0.16	0.21	0.31	0.50	
			4 MHz	0.10	0.11	0.17	0.26	0.46	
			2 MHz	0.08	0.09	0.15	0.24	0.44	
			1 MHz	0.07	0.08	0.13	0.23	0.43	
			100 kHz	0.06	0.07	0.13	0.22	0.41	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, VDD12 = 1.10 V

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 68. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A(1)

1. Negative injection is limited to -30 mA for PF0, PF1, PG6, PG7, PG8, PG12, PG13, PG14.

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 69*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 69. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}(1)	Injected current on all pins except PA4, PA5, PB0, PF12, PF13, OPAMP1_V1NM, OPAMP2_V1NM	-5	NA	mA
	Injected current on pins PB0, PF12, PF13	0	NA	
	Injected current on OPAMP1_V1NM, OPAMP2_V1NM	0	0	
	Injected current on PA4, PA5 pins	-5	0	

1. Guaranteed by characterization.

Table 83. VREFBUF characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDA}(VREFBUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA	-	16	25	µA
		I_{load} = 500 µA	-	18	30	
		I_{load} = 4 mA	-	35	50	

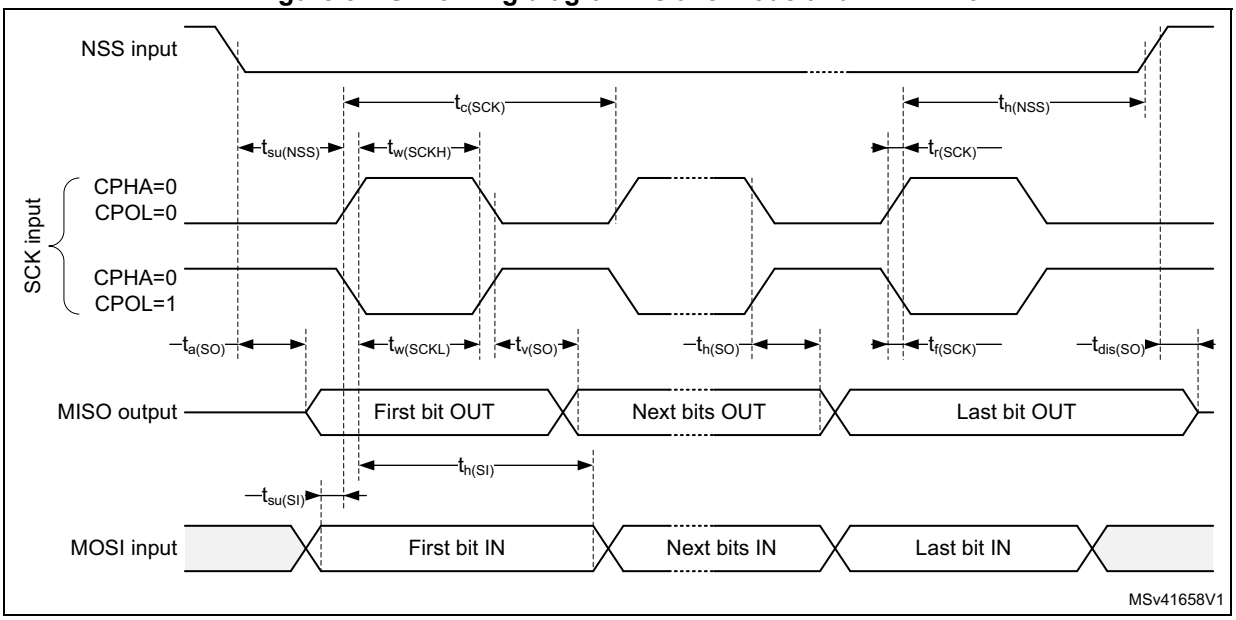
1. Guaranteed by design, unless otherwise specified.
2. In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which will follow (V_{DDA} - drop voltage).
3. Guaranteed by test in production.
4. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.
5. To correctly control the VREFBUF inrush current during start-up phase and scaling change, the V_{DDA} voltage should be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 1.

Table 95. SPI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 V < V_{DD} < 3.6 V Voltage Range 1	-	13	15.5	ns
		Slave mode 1.71 V < V_{DD} < 3.6 V Voltage Range 1	-	13	26.5	
		Slave mode 1.71 V < V_{DD} < 3.6 V Voltage Range 2	-	13	30	
-		Slave mode 1.08 V < V_{DDIO2} < 1.32 V(3)	-	26	60	
$t_{v(MO)}$		Master mode	-	4.5	6	
th(SO)	Data output hold time	Slave mode 1.71 V < V_{DD} < 3.6 V	7	-	-	
th(MO)		Master mode	0	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50 %.
3. SPI mapped on Port G.

Figure 34. SPI timing diagram - slave mode and CPHA = 0



Quad SPI characteristics

Unless otherwise specified, the parameters given in *Table 96* and *Table 97* for Quad SPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 15 or 20 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 96. Quad SPI characteristics in SDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	Quad SPI clock frequency	1.71 V < V_{DD}< 3.6 V, C_{LOAD} = 20 pF Voltage Range 1	-	-	40	MHz
		1.71 V < V_{DD}< 3.6 V, C_{LOAD} = 15 pF Voltage Range 1	-	-	48	
		2.7 V < V_{DD}< 3.6 V, C_{LOAD} = 15 pF Voltage Range 1	-	-	60	
		1.71 V < V_{DD} < 3.6 V C_{LOAD} = 20 pF Voltage Range 2	-	-	26	
$t_{w(CKH)}$	Quad SPI clock high and low time	f_{AHBCLK}= 48 MHz, presc=0	$t_{(CK)}/2$	-	$t_{(CK)}/2+1$	ns
$t_{w(CKL)}$			$t_{(CK)}/2-1$	-	$t_{(CK)}/2$	
$t_{s(IN)}$	Data input setup time	Voltage Range 1	1.5	-	-	
		Voltage Range 2	3.5	-	-	
$t_{h(IN)}$	Data input hold time	Voltage Range 1	4	-	-	
		Voltage Range 2	6.5	-	-	
$t_{v(OUT)}$	Data output valid time	Voltage Range 1	-	1	1.5	
		Voltage Range 2	-	3	5	
$t_{h(OUT)}$	Data output hold time	Voltage Range 1	0	-	-	
		Voltage Range 2	0	-	-	

1. Guaranteed by characterization results.

SAI characteristics

Unless otherwise specified, the parameters given in *Table 98* for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CK,SD,FS).

Table 98. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCLK}	SAI Main clock output	-	-	50	MHz
f_{CK}	SAI clock frequency(2)	Master transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	21.5	MHz
		Master transmitter 1.71 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	13.5	
		Master receiver Voltage Range 1	-	25	
		Slave transmitter 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	20	
		Slave transmitter 1.71 V ≤ V_{DD} ≤ 3.6 V Voltage Range 1	-	13.5	
		Slave receiver Voltage Range 1	-	25	
		Voltage Range 2	-	13	
		1.08 V ≤ V_{DD} ≤ 1.32 V	-	7	
$t_{v(FS)}$	FS valid time	Master mode 2.7 V ≤ V_{DD} ≤ 3.6 V	-	22	ns
		Master mode 1.71 V ≤ V_{DD} ≤ 3.6 V	-	40	
$t_{h(FS)}$	FS hold time	Master mode	10	-	ns
$t_{su(FS)}$	FS setup time	Slave mode	1	-	ns
$t_{h(FS)}$	FS hold time	Slave mode	2	-	ns
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	1	-	ns
$t_{su(SD\_B\_SR)}$		Slave receiver	1	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	5	-	ns
$t_{h(SD\_B\_SR)}$		Slave receiver	2	-	

Figure 43. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms

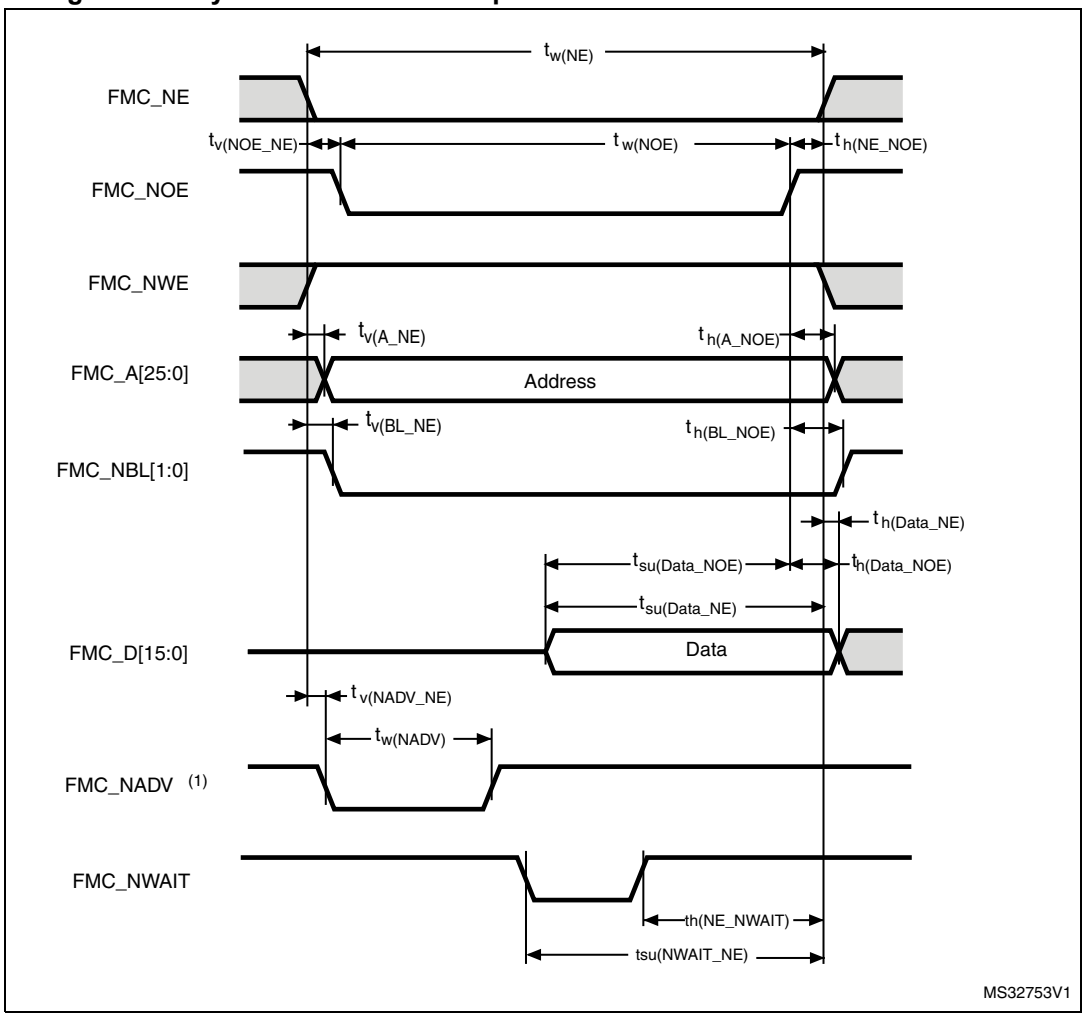


Figure 47. Synchronous multiplexed NOR/PSRAM read timings