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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	83
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l496vet6

2 Description

The STM32L496xx devices are the ultra-low-power microcontrollers based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 80 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32L496xx devices embed high-speed memories (up to 1 Mbyte of Flash memory, 320 Kbyte of SRAM), a flexible external memory controller (FSMC) for static memories (for devices with packages of 100 pins and more), a Quad SPI flash memories interface (available on all packages) and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The STM32L496xx devices embed several protection mechanisms for embedded Flash memory and SRAM: readout protection, write protection, proprietary code readout protection and Firewall.

The devices offer up to three fast 12-bit ADCs (5 Msps), two comparators, two operational amplifiers, two DAC channels, an internal voltage reference buffer, a low-power RTC, two general-purpose 32-bit timer, two 16-bit PWM timers dedicated to motor control, seven general-purpose 16-bit timers, and two 16-bit low-power timers. The devices support four digital filters for external sigma delta modulators (DFSDM).

In addition, up to 24 capacitive sensing channels are available. The devices also embed an integrated LCD driver 8x40 or 4x44, with internal step-up converter.

They also feature standard and advanced communication interfaces.

- Four I2Cs
- Three SPIs
- Three USARTs, two UARTs and one Low-Power UART.
- Two SAIs (Serial Audio Interfaces)
- One SDMMC
- Two CAN
- One USB OTG full-speed
- One SWPMI (Single Wire Protocol Master Interface)
- Camera interface
- DMA2D controller

The STM32L496xx operates in the -40 to +85 °C (+105 °C junction), -40 to +105 °C (+125 °C junction) and -40 to +125 °C (+130 °C junction) temperature ranges from a 1.71 to 3.6 V VDD power supply when using internal LDO regulator and a 1.05 to 1.32V VDD12 power supply when using external SMPS supply. A comprehensive set of power-saving modes allows the design of low-power applications.

Some independent power supplies are supported: analog independent supply input for ADC, DAC, OPAMPs and comparators, 3.3 V dedicated supply input for USB and up to 14 I/Os can be supplied independently down to 1.08V. A VBAT input allows to backup the RTC and backup registers. Dedicated VDD12 power supplies can be used to bypass the internal LDO regulator when connected to an external SMPS.

Table 4. STM32L496xx modes overview (continued)

Mode	Regulator[1]	CPU	Flash	SRAM	Clocks	DMA & Peripherals[2]	Wakeup source	Consumption[3]	Wakeup time
Standby	LPR	Powered Off	Off	SRAM 2 ON	LSE LSI	BOR, RTC, IWDG *** All other peripherals are powered off. *** I/O configuration can be floating, pull-up or pull-down	Reset pin 5 I/Os (WKUPx)[13] BOR, RTC, IWDG	0.48 µA w/o RTC 0.78 µA w/ RTC	15.3 µs
	OFF			Powered Off				0.11 µA w/o RTC 0.42 µA w/ RTC	
Shutdown	OFF	Powered Off	Off	Powered Off	LSE	RTC *** All other peripherals are powered off. *** I/O configuration can be floating, pull-up or pull-down[14]	Reset pin 5 I/Os (WKUPx)[14] RTC	0.03 µA w/o RTC 0.23 µA w/ RTC	306 µs

1. LPR means Main regulator is OFF and Low-power regulator is ON.
2. All peripherals can be active or clock gated to save power consumption.
3. Typical current at V_{DD} = 1.8 V, 25°C. Consumptions values provided running from SRAM, Flash memory Off, 80 MHz in Range 1, 26 MHz in Range 2, 2 MHz in LPRun/LPSleep.
4. The Flash memory can be put in power-down and its clock can be gated off when executing from SRAM.
5. Theoretical value based on V_{DD} = 3.3 V, DC/DC Efficiency of 85%, VCORE = 1.10 V
6. Theoretical value based on V_{DD} = 3.3 V, DC/DC Efficiency of 85%, VCORE = 1.05 V
7. The SRAM1 and SRAM2 clocks can be gated on or off independently.
8. SMPS mode can be used in STOP0 Mode, but no significant power gain can be expected.
9. U(S)ART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
10. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
11. OTG_FS wakeup by resume from suspend and attach detection protocol event.
12. SWPMI1 wakeup by resume from suspend.
13. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.
14. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

By default, the microcontroller is in Run mode after a system or a power Reset. It is up to the user to select one of the low-power modes described below:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Low-power run** mode

  This mode is achieved with VCORE supplied by the low-power regulator to minimize the regulator's operating current. The code can be executed from SRAM or from Flash, and the CPU frequency is limited to 2 MHz. The peripherals with independent clock can be clocked by HSI16.

- **Low-power sleep** mode

  This mode is entered from the low-power run mode. Only the CPU clock is stopped. When wakeup is triggered by an event or an interrupt, the system reverts to the low-power run mode.

- **Stop 0, Stop 1 and Stop 2** modes

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the VCORE domain are stopped, the PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are disabled. The LSE or LSI is still running.

  The RTC can remain active (Stop mode with RTC, Stop mode without RTC).

  Some peripherals with wakeup capability can enable the HSI16 RC during Stop mode to detect their wakeup condition.

  Three Stop modes are available: Stop 0, Stop 1 and Stop 2 modes. In Stop 2 mode, most of the VCORE domain is put in a lower leakage mode.

  Stop 1 offers the largest number of active peripherals and wakeup sources, a smaller wakeup time but a higher consumption than Stop 2. In Stop 0 mode, the main regulator remains ON, allowing a very fast wakeup time but with much higher consumption.

  The system clock when exiting from Stop 0, Stop1 or Stop2 modes can be either MSI up to 48 MHz or HSI16, depending on software configuration.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption with BOR. The internal regulator is switched off so that the VCORE domain is powered off. The PLL, the MSI RC, the HSI16 RC and the HSE crystal oscillators are also switched off.

  The RTC can remain active (Standby mode with RTC, Standby mode without RTC).

  The brown-out reset (BOR) always remains active in Standby mode.

  The state of each I/O during standby mode can be selected by software: I/O with internal pull-up, internal pull-down or floating.

  After entering Standby mode, SRAM1 and register contents are lost except for registers in the Backup domain and Standby circuitry. Optionally, SRAM2 can be retained in Standby mode, supplied by the low-power Regulator (Standby with RAM2 retention mode).

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, WKUP pin event (configurable rising or falling edge), or an RTC event occurs (alarm, periodic wakeup, timestamp, tamper) or a failure is detected on LSE (CSS on LSE).

  The system clock after wakeup is MSI up to 8 MHz.

3.12 Clocks and startup

The clock controller (see *Figure 4*) distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** four different clock sources can be used to drive the master clock SYSCLK:
  - 4-48 MHz high-speed external crystal or ceramic resonator (HSE), that can supply a PLL. The HSE can also be configured in bypass mode for an external clock.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 12 frequencies from 100 kHz to 48 MHz. When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be automatically trimmed by hardware to reach better than ±0.25% accuracy. In this mode the MSI can feed the USB device, saving the need of an external high-speed crystal (HSE). The MSI can supply a PLL.
  - System PLL which can be fed by HSE, HSI16 or MSI, with a maximum frequency at 80 MHz.
- RC48 with clock recovery system (HSI48): internal 48 MHz clock source (HSI48)can be used to drive the USB, the SDMMC or the RNG peripherals. This clock can be output on the MCO.
- **Auxiliary clock source:** two ultralow-power clock sources that can be used to drive the LCD controller and the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - 32 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock accuracy is ±5% accuracy.
- **Peripheral clock sources:** Several peripherals (USB, SDMMC, RNG, SAI, USARTs, I2Cs, LPTimers, ADC, SWPMI) have their own independent clock whatever the system clock. Three PLLs, each having three independent outputs allowing the highest flexibility, can generate independent clocks for the ADC, the USB/SDMMC/RNG and the two SAIs.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 4 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI16 and a software

Figure 4. Clock tree

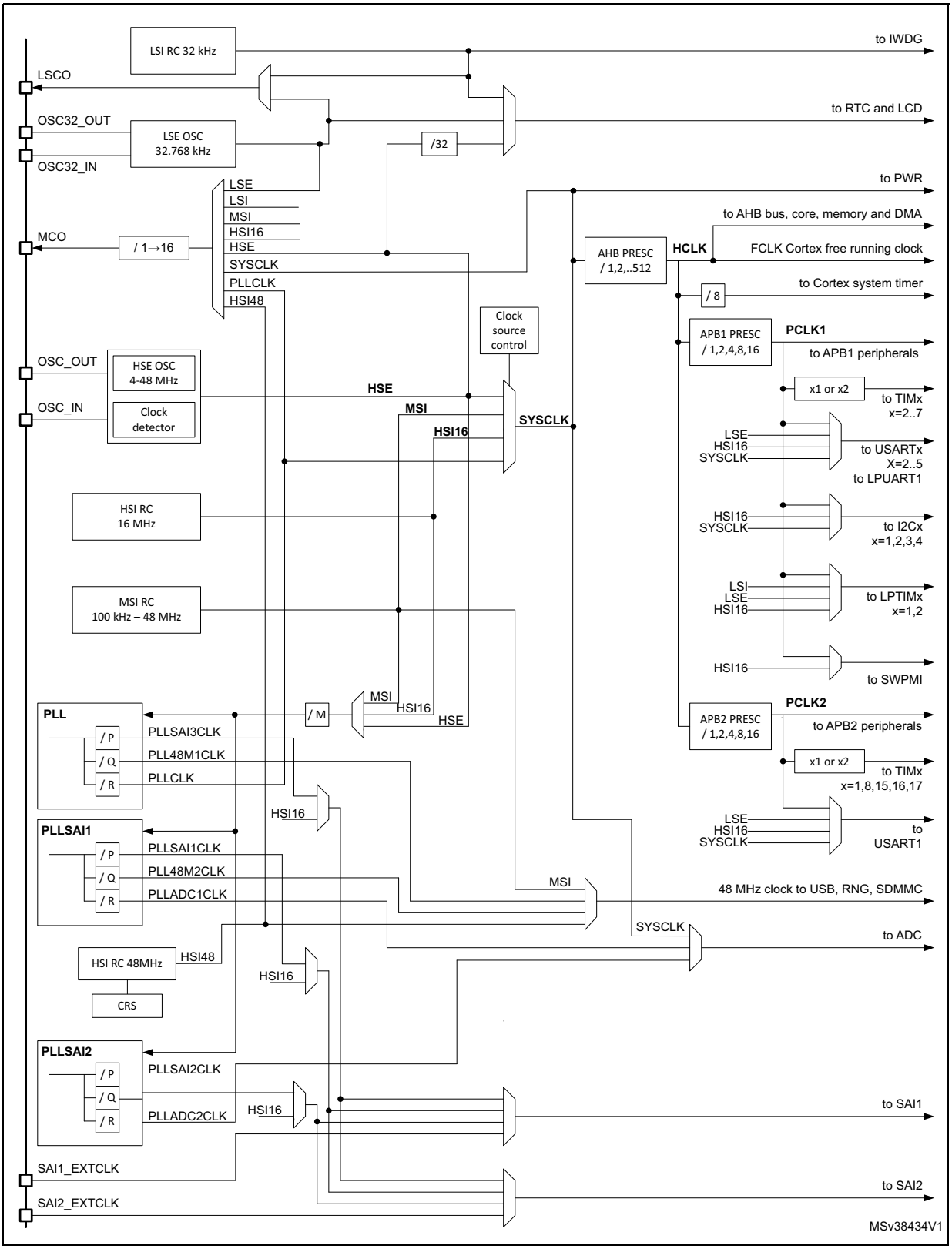
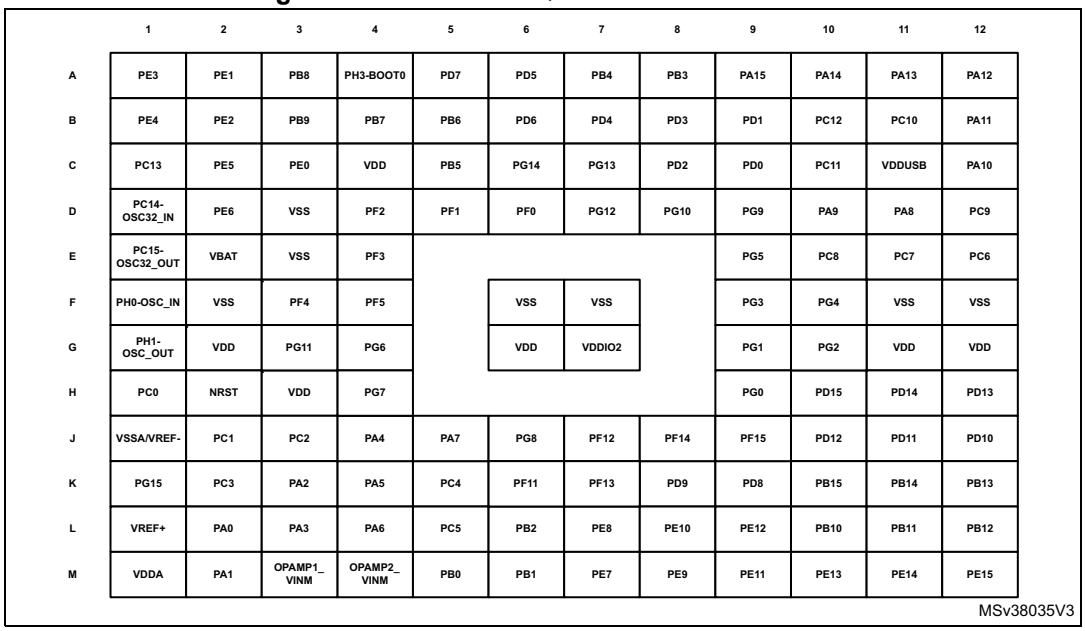


Figure 10. STM32L496Qx UFBGA132 ballout(1)



1. The above figure shows the package top view.

Table 15. STM32L496xx pin definitions (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP100	WLCSP100_SMPS	LQFP100	UFBGA132	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
5	F10	F10	12	F1	23	23	H1	H1	PH0-OSC_IN (PH0)	I/O	FT	-	EVENTOUT	OSC_IN
6	G10	F9	13	G1	24	24	J1	J1	PH1-OSC_OUT (PH1)	I/O	FT	-	EVENTOUT	OSC_OUT
7	E8	F8	14	H2	25	25	H3	H3	NRST	I/O	RST	-	-	-
8	F9	G10	15	H1	26	26	J2	J2	PC0	I/O	FT_fla	-	LPTIM1_IN1, I2C4_SCL, I2C3_SCL, DFSDM1_DATIN4, LPUART1_RX, LCD_SEG18, LPTIM2_IN1, EVENTOUT	ADC123_IN1
9	F8	F7	16	J2	27	27	J3	J3	PC1	I/O	FT_fla	-	TRACED0, LPTIM1_OUT, I2C4_SDA, SPI2_MOSI, I2C3_SDA, DFSDM1_CKIN4, LPUART1_TX, QUADSPI_BK2_IO0, LCD_SEG19, SAI1_SD_A, EVENTOUT	ADC123_IN2
10	H10	G9	17	J3	28	28	J4	J4	PC2	I/O	FT_la	-	LPTIM1_IN2, SPI2_MISO, DFSDM1_CKOUT, QUADSPI_BK2_IO1, LCD_SEG20, EVENTOUT	ADC123_IN3
11	F7	F6	18	K2	29	29	K1	K1	PC3	I/O	FT_la	-	LPTIM1_ETR, SPI2_MOSI, QUADSPI_BK2_IO2, LCD_VLCD, SAI1_SD_A, LPTIM2_ETR, EVENTOUT	ADC123_IN4
-	H9	H9	19	-	30	30	-	-	VSSA	S	-	-	-	-
-	G8	-	20	-	31	31	-	-	VREF-	S	-	-	-	-
12	-	-	-	J1	-	-	K2	K2	VSSA/VREF-	S	-	-	-	-
-	G7	H10	21	L1	32	32	L1	L1	VREF+	S	-	-	-	VREFBUF_OUT

Table 15. STM32L496xx pin definitions (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP100	WLCSP100_SMPS	LQFP100	UFBGA132	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	-	-	-	-	95	95	F12	F12	VDDIO2	S	-	-	-	-
37	F2	F4	63	E12	96	96	F11	F11	PC6	I/O	FT_l	-	TIM3_CH1, TIM8_CH1, DFSDM1_CKIN3, TSC_G4_IO1, DCMI_D0, LCD_SEG24, SDMMC1_D6, SAI2_MCLK_A, EVENTOUT	-
38	F3	E4	64	E11	97	97	G12	G12	PC7	I/O	FT_l	-	TIM3_CH2, TIM8_CH2, DFSDM1_DATIN3, TSC_G4_IO2, DCMI_D1, LCD_SEG25, SDMMC1_D7, SAI2_MCLK_B, EVENTOUT	-
39	E1	E1	65	E10	98	98	G10	G10	PC8	I/O	FT_l	-	TIM3_CH3, TIM8_CH3, TSC_G4_IO3, DCMI_D2, LCD_SEG26, SDMMC1_D0, EVENTOUT	-
40	E2	E2	66	D12	99	99	G9	G9	PC9	I/O	FT_fl	-	TIM8_BKIN2, TIM3_CH4, TIM8_CH4, DCMI_D3, I2C3_SDA, TSC_G4_IO4, OTG_FS_NOE, LCD_SEG27, SDMMC1_D1, SAI2_EXTCLK, TIM8_BKIN2_COMP1, EVENTOUT	-
41	E3	E3	67	D11	100	100	G8	G8	PA8	I/O	FT_l	-	MCO, TIM1_CH1, USART1_CK, OTG_FS_SOF, LCD_COM0, SWPMI1_IO, SAI1_SCK_A, LPTIM2_OUT, EVENTOUT	-
42	D3	D3	68	D10	101	101	F10	F10	PA9	I/O	FT_lu	-	TIM1_CH2, SPI2_SCK, DCMI_D0, USART1_TX, LCD_COM1, SAI1_FS_A, TIM15_BKIN, EVENTOUT	OTG_FS_VBUS
43	D2	D2	69	C12	102	102	F9	F9	PA10	I/O	FT_lu	-	TIM1_CH3, DCMI_D1, USART1_RX, OTG_FS_ID, LCD_COM2, SAI1_SD_A, TIM17_BKIN, EVENTOUT	-
44	D1	D1	70	B12	103	103	E13	E13	PA11	I/O	FT_u	-	TIM1_CH4, TIM1_BKIN2, SPI1_MISO, USART1_CTS, CAN1_RX, OTG_FS_DM, TIM1_BKIN2_COMP1, EVENTOUT	-

Table 15. STM32L496xx pin definitions (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP100	WLCSP100_SMPS	LQFP100	UFBGA132	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	A4	A4	-	-	121	121	-	-	VDD	S	-	-	-	-
-	D5	B5	87	B6	122	122	E7	E7	PD6	I/O	FT	-	DCMI_D10, QUADSPI_BK2_IO1, DFSDM1_DATIN1, USART2_RX, QUADSPI_BK2_IO2, FMC_NWAIT, SAI1_SD_A, EVENTOUT	-
-	C5	C6	88	A5	123	123	F7	F7	PD7	I/O	FT	-	DFSDM1_CKIN1, USART2_CK, QUADSPI_BK2_IO3, FMC_NE1, EVENTOUT	-
-	B5	D6	-	D9	124	124	B7	B7	PG9	I/O	FT_s	-	SPI3_SCK, USART1_TX, FMC_NCE/FMC_NE2, SAI2_SCK_A, TIM15_CH1N, EVENTOUT	-
-	A5	A5	-	D8	125	125	D6	D6	PG10	I/O	FT_s	-	LPTIM1_IN1, SPI3_MISO, USART1_RX, FMC_NE3, SAI2_FS_A, TIM15_CH1, EVENTOUT	-
-	D6	E5	-	G3	126	126	E6	E6	PG11	I/O	FT_s	-	LPTIM1_IN2, SPI3_MOSI, USART1_CTS, SAI2_MCLK_A, TIM15_CH2, EVENTOUT	-
-	B6	B6	-	D7	127	127	F6	F6	PG12	I/O	FT_s	-	LPTIM1_ETR, SPI3_NSS, USART1_RTS_DE, FMC_NE4, SAI2_SD_A, EVENTOUT	-
-	-	-	-	C7	128	128	G7	G7	PG13	I/O	FT_fs	-	I2C1_SDA, USART1_CK, FMC_A24, EVENTOUT	-
-	-	-	-	C6	129	129	G6	G6	PG14	I/O	FT_fs	-	I2C1_SCL, FMC_A25, EVENTOUT	-
-	-	-	-	F7	130	130	A7	A7	VSS	S	-	-	-	-
-	A6	A6	-	G7	131	131	B6	B6	VDDIO2	S	-	-	-	-

Table 16. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 17*) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/2/5/8/ LPTIM1	TIM1/2/3/4/5	SPI2/USART2/ CAN2/TIM8/ QUADSPI	I2C1/2/3/4/ DCMI	SPI1/2/DCMI/ QUADSPI	SPI3/I2C3/ DFSDM/ COMP1/ QUADSPI	USART1/2/3
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-
	PF1	-	-	-	-	I2C2_SCL	-	-	-
	PF2	-	-	-	-	I2C2_SMBA	-	-	-
	PF3	-	-	-	-	-	-	-	-
	PF4	-	-	-	-	-	-	-	-
	PF5	-	-	-	-	-	-	-	-
	PF6	-	TIM5_ETR	TIM5_CH1	-	-	-	-	-
	PF7	-	-	TIM5_CH2	-	-	-	-	-
	PF8	-	-	TIM5_CH3	-	-	-	-	-
	PF9	-	-	TIM5_CH4	-	-	-	-	-
	PF10	-	-	-	QUADSPI_CLK	-	-	-	-
	PF11	-	-	-	-	-	-	-	-
	PF12	-	-	-	-	-	-	-	-
	PF13	-	-	-	-	I2C4_SMBA	-	DFSDM1_ DATIN6	-
	PF14	-	-	-	-	I2C4_SCL	-	DFSDM1_CKIN6	-
	PF15	-	-	-	-	I2C4_SDA	-	-	-

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 16*) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	CAN2/ OTG_FS/DCMI/ QUADSPI	LCD	SDMMC/ COMP1/2/FMC/SWPMI1	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port I	PI0	-	-	DCMI_D13	-	-	-	-	EVENTOUT
	PI1	-	-	DCMI_D8	-	-	-	-	EVENTOUT
	PI2	-	-	DCMI_D9	-	-	-	-	EVENTOUT
	PI3	-	-	DCMI_D10	-	-	-	-	EVENTOUT
	PI4	-	-	DCMI_D5	-	-	-	-	EVENTOUT
	PI5	-	-	DCMI_VSYNC	-	-	-	-	EVENTOUT
	PI6	-	-	DCMI_D6	-	-	-	-	EVENTOUT
	PI7	-	-	DCMI_D7	-	-	-	-	EVENTOUT
	PI8	-	-	DCMI_D12	-	-	-	-	EVENTOUT
	PI9	-	CAN1_RX	-	-	-	-	-	EVENTOUT
	PI10	-	-	-	-	-	-	-	EVENTOUT
	PI11	-	-	-	-	-	-	-	EVENTOUT

3. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
4. Positive injection (when $V_{IN} > V_{DDIOx}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 19: Voltage characteristics* for the minimum allowed input voltage values.
6. When several inputs are submitted to a current injection, the maximum $\sum|I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 21. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 22. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	80	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	80	
f_{PCLK2}	Internal APB2 clock frequency	-	0	80	
V_{DD}	Standard operating voltage	-	1.71 (1)	3.6	V
VDD12	Standard operating voltage	full frequency range	1.08	1.32	
		up to 26MHz	1.05		
V_{DDIO2}	PG[15:2] I/Os supply voltage	At least one I/O in PG[15:2] used	1.08	3.6	V
		PG[15:2] not used	0	3.6	
V_{DDA}	Analog supply voltage	ADC or COMP used	1.62	3.6	V
		DAC or OPAMP used	1.8		
		VREFBUF used	2.4		
		ADC, DAC, OPAMP, COMP, VREFBUF not used	0		

Table 26. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART enable (Cache ON Prefetch OFF)

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.65	2.69	2.82	3.05	3.51	2.9	3.0	3.3	3.8	4.7	mA
				16 MHz	1.68	1.72	1.85	2.07	2.53	1.9	2.0	2.2	2.7	3.7	
				8 MHz	0.91	0.94	1.07	1.29	1.74	1.0	1.1	1.4	1.8	2.8	
				4 MHz	0.52	0.55	0.68	0.9	1.35	0.6	0.7	0.9	1.4	2.4	
				2 MHz	0.33	0.36	0.48	0.7	1.15	0.4	0.5	0.7	1.2	2.2	
				1 MHz	0.23	0.26	0.38	0.6	1.06	0.3	0.4	0.6	1.1	2.0	
				100 kHz	0.14	0.17	0.3	0.52	0.97	0.2	0.3	0.5	1.0	2.0	
			Range 1	80 MHz	9.44	9.5	9.67	9.93	10.4	10.3	10.4	10.7	11.3	12.4	
				72 MHz	8.52	8.59	8.75	9.01	9.53	9.3	9.4	9.7	10.3	11.4	
				64 MHz	7.61	7.67	7.83	8.09	8.61	8.3	8.4	8.7	9.3	10.4	
				48 MHz	5.72	5.78	5.94	6.2	6.72	6.3	6.4	6.7	7.3	8.4	
				32 MHz	3.87	3.92	4.07	4.33	4.84	4.2	4.4	4.7	5.2	6.3	
				24 MHz	2.94	2.99	3.14	3.39	3.9	3.2	3.4	3.6	4.2	5.3	
				16 MHz	2.01	2.06	2.2	2.45	2.95	2.2	2.3	2.6	3.2	4.2	
I_{DD_ALL} (LPRun)	Supply current in Low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	274	307	444	678	1150	318	425	656	1167	2197	µA
				1 MHz	158	195	328	564	1040	195	309	558	1047	2084	
				400 kHz	88.2	123	256	490	969	116	232	485	973	2012	
				100 kHz	63	90.6	223	457	934	79	195	447	942	1975	

1. Guaranteed by characterization results, unless otherwise specified.

Table 40. Typical current consumption in Run, with different codesrunning from SRAM1 and power supplied by external SMPS (VDD12 = 1.05 V)

Symbol	Parameter	Conditions(1)			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	f_{HCLK} = 26 MHz	Reduced code(2)	1.07	mA	41	µA/MHz
				Coremark	1.07		41	
				Dhrystone 2.1	1.04		40	
				Fibonacci	0.97		37	
				While(1)	0.93		36	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, VDD12 = 1.05 V
2. Reduced code used for characterization results provided in *Table 26*, *Table 28*, *Table 30*.

Figure 25. HSI16 frequency versus temperature

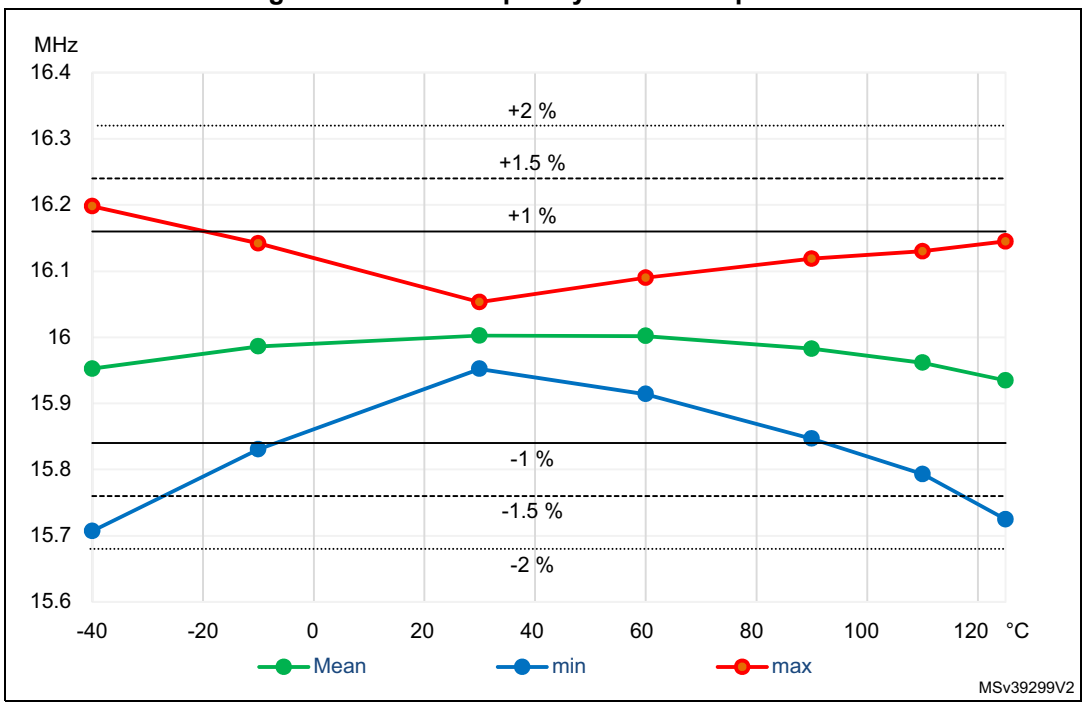


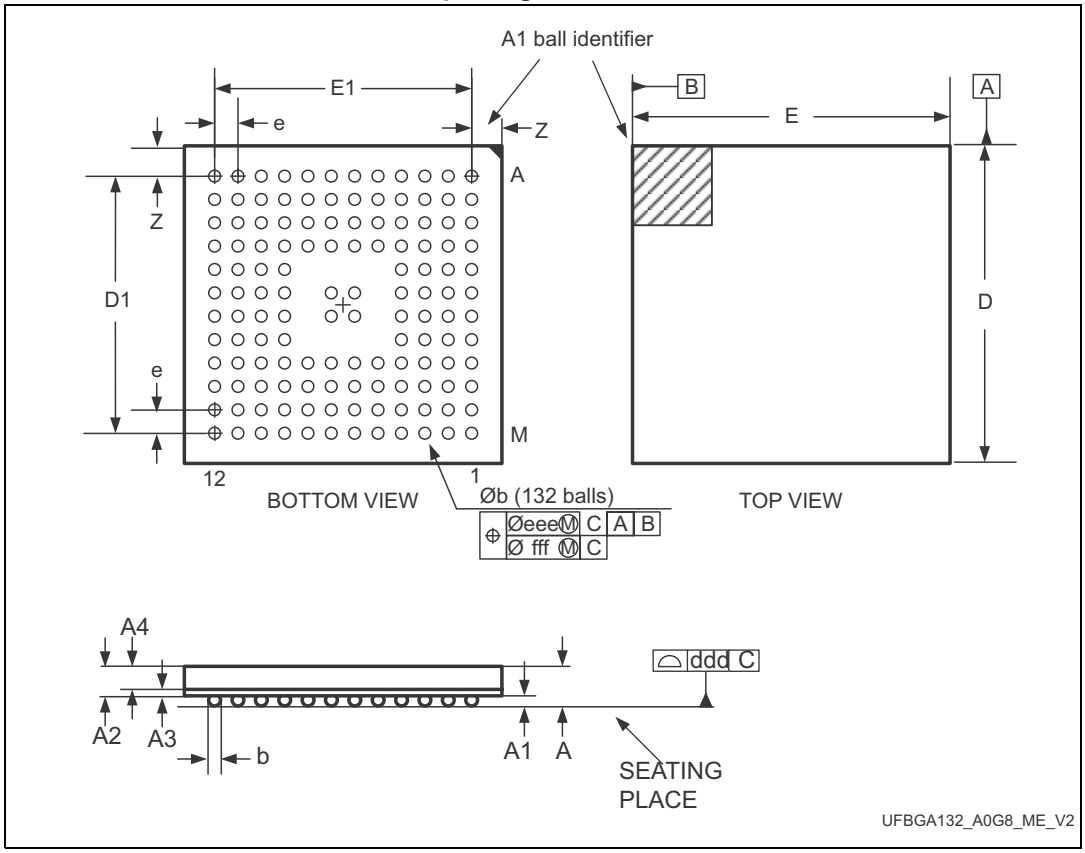
Table 72. I/O AC characteristics(1)(2) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
10	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	25	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	5	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	100(3)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37.5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5.8	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	11	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	28	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	2.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	12	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	120(3)	MHz
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	50	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	10	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	180(3)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	75	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	10	
	Tr/Tf	Output rise and fall time	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	3.3	ns
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	6	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	16	
Fm+	Fmax	Maximum frequency	C=50 pF, 1.6 V≤V_{DDIOx}≤3.6 V	-	1	MHz
	Tf	Output fall time(4)		-	5	ns

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the RM0351 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. This value represents the I/O capability but the maximum system frequency is limited to 80 MHz.
4. The fall time is defined between 70% and 30% of the output waveform accordingly to I^2C specification.

7.3 UFBGA132 package information

Figure 66. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package outline



1. Drawing is not to scale.

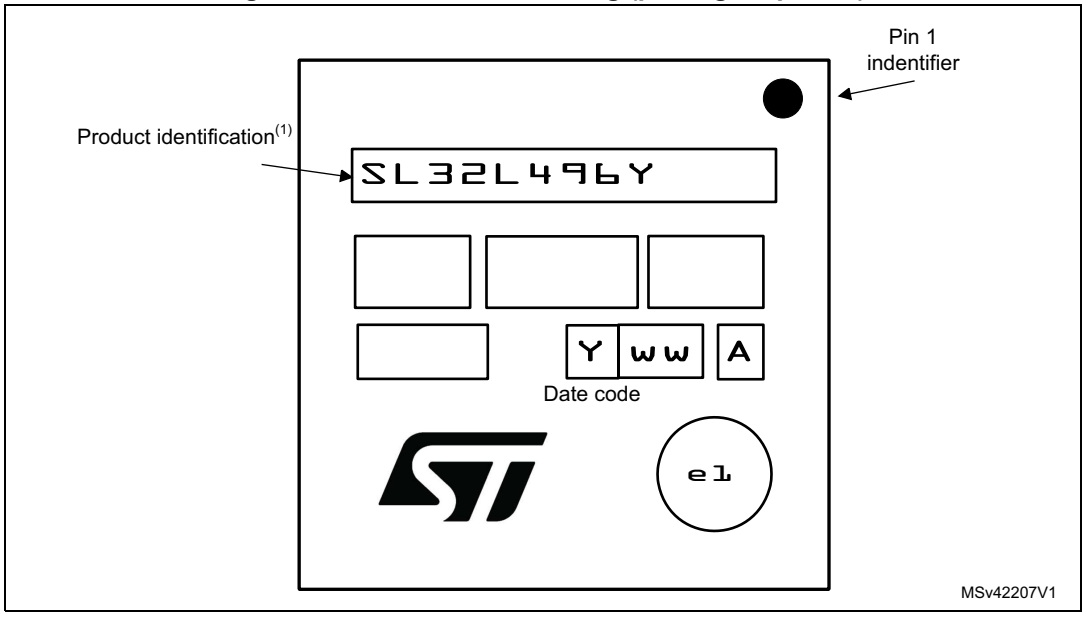
Table 123. UFBGA132 - 132-ball, 7 x 7 mm ultra thin fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-

Table 127. WLCSP100L recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm
Stencil thickness	0.1 mm

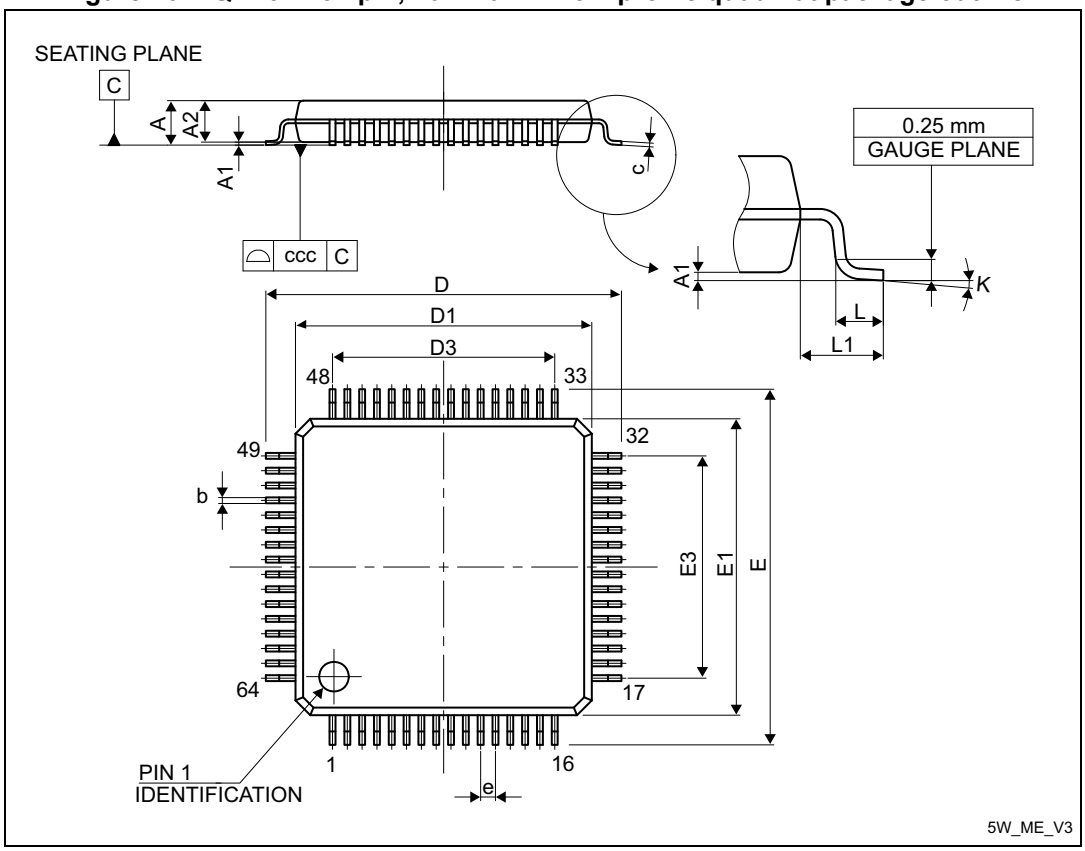
Figure 74. WLCSP100L marking (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.6 LQFP64 package information

Figure 76. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 128. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

9 Revision history

Table 131. Document revision history

Date	Revision	Changes
22-Feb-2017	1	Initial release.