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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

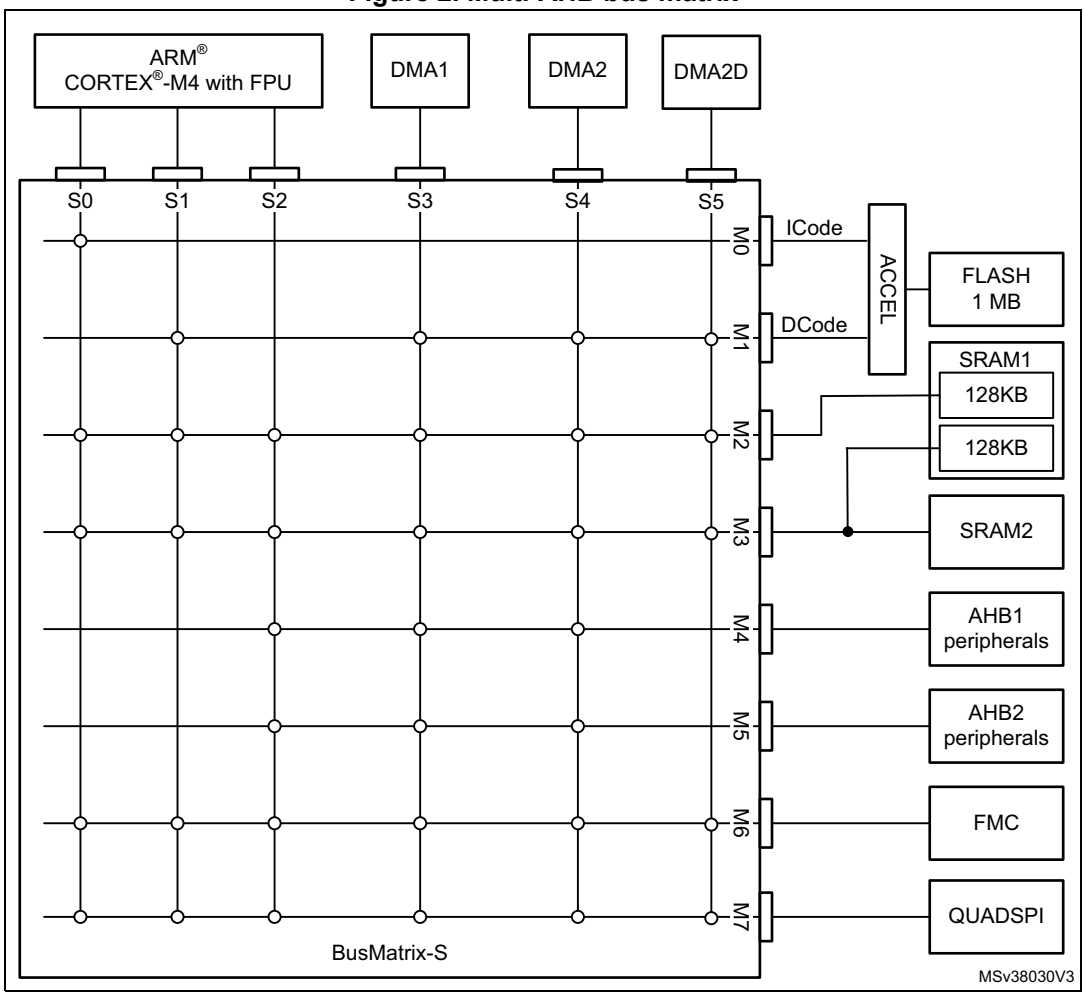
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	83
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l496vgt6p

3.6 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs and the DMA2D) and the slaves (Flash memory, RAM, FMC, QUADSPI, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high speed peripherals work simultaneously.

Figure 2. Multi-AHB bus matrix



3.7 Firewall

The device embeds a Firewall which protects code sensitive and secure data from any access performed by a code executed outside of the protected areas.

Each illegal access generates a reset which kills immediately the detected intrusion.

3.17 Analog to digital converter (ADC)

The device embeds 3 successive approximation analog-to-digital converters with the following features:

- 12-bit native resolution, with built-in calibration
- 5.33 Msps maximum conversion rate with full resolution
  - Down to 18.75 ns sampling time
  - Increased conversion rate for lower resolution (up to 8.88 Msps for 6-bit resolution)
- Up to 24 external channels, some of them shared between ADC1 and ADC2, or ADC1, ADC2 and ADC3.
- 5 internal channels: internal reference voltage, temperature sensor, VBAT/3, DAC1 and DAC2 outputs.
- One external reference pin is available on some package, allowing the input voltage range to be independent from the power supply
- Single-ended and differential mode inputs
- Low-power design
  - Capable of low-current operation at low conversion rate (consumption decreases linearly with speed)
  - Dual clock domain architecture: ADC speed independent from CPU frequency
- Highly versatile digital interface
  - Single-shot or continuous/discontinuous sequencer-based scan mode: 2 groups of analog signals conversions can be programmed to differentiate background and high-priority real-time conversions
  - Handles two ADC converters for dual mode operation (simultaneous or interleaved sampling modes)
  - Each ADC support multiple trigger inputs for synchronization with on-chip timers and external signals
  - Results stored into 3 data register or in RAM with DMA controller support
  - Data pre-processing: left/right alignment and per channel offset compensation
  - Built-in oversampling unit for enhanced SNR
  - Channel-wise programmable sampling time
  - Three analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers
  - Hardware assistant to prepare the context of the injected channels to allow fast context switching

3.17.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1_IN17 and ADC3_IN17 input channels which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

Table 10. Timer feature comparison (continued)

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.27.1 Advanced-control timer (TIM1, TIM8)

The advanced-control timer can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as complete general-purpose timers. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes) with full modulation capability (0-100%)
- One-pulse mode output

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switches driven by these outputs.

Many features are shared with those of the general-purpose TIMx timers (described in *Section 3.27.2*) using the same architecture, so the advanced-control timers can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

3.40 Dual-flash Quad SPI memory interface (QUADSPI)

The Dual-flash Quad SPI is a specialized communication interface targeting single, dual or quad SPI flash memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the QUADSPI registers
- Status polling mode: the external flash status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external Flash is memory mapped and is seen by the system as if it were an internal memory

Both throughput and capacity can be increased two-fold using dual-flash mode, where two Quad SPI flash memories are accessed simultaneously.

The Dual-flash Quad SPI interface supports:

- Three functional modes: indirect, status-polling, and memory-mapped
- Dual-flash mode, where 8 bits can be sent/received simultaneously by accessing two flash memories in parallel.
- SDR and DDR support
- Fully programmable opcode for both indirect and memory mapped mode
- Fully programmable frame format for both indirect and memory mapped mode
- Each of the 5 following phases can be configured independently (enable, length, single/dual/quad communication)
  - Instruction phase
  - Address phase
  - Alternate bytes phase
  - Dummy cycles phase
  - Data phase
- Integrated FIFO for reception and transmission
- 8, 16, and 32-bit data accesses are allowed
- DMA channel for indirect mode operations
- Programmable masking for external flash flag management
- Timeout management
- Interrupt generation on FIFO threshold, timeout, status match, operation complete, and access error

Table 15. STM32L496xx pin definitions (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP100	WLCSP100_SMPS	LQFP100	UFBGA132	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
52	C3	D4	79	C10	112	112	E9	E9	PC11	I/O	FT_l	-	QUADSPI_BK2_NCS, SPI3_MISO, USART3_RX, UART4_RX, TSC_G3_IO3, DCMI_D4, LCD_COM5/LCD_SEG29/LCD_SEG41, SDMMC1_D3, SAI2_MCLK_B, EVENTOUT	-
53	C4	C4	80	B10	113	113	F8	F8	PC12	I/O	FT_l	-	TRACED3, SPI3_MOSI, USART3_CK, UART5_TX, TSC_G3_IO4, DCMI_D9, LCD_COM6/LCD_SEG30/LCD_SEG42, SDMMC1_CK, SAI2_SD_B, EVENTOUT	-
-	B3	B3	81	C9	114	114	B8	B8	PD0	I/O	FT	-	SPI2_NSS, DFSDM1_DATIN7, CAN1_RX, FMC_D2, EVENTOUT	-
-	A3	A3	82	B9	115	115	C8	C8	PD1	I/O	FT	-	SPI2_SCK, DFSDM1_CKIN7, CAN1_TX, FMC_D3, EVENTOUT	-
54	E4	D5	83	C8	116	116	D8	D8	PD2	I/O	FT_l	-	TRACED2, TIM3_ETR, USART3_RTS_DE, UART5_RX, TSC_SYNC, DCMI_D11, LCD_COM7/LCD_SEG31/LCD_SEG43, SDMMC1_CMD, EVENTOUT	-
-	-	-	84	B8	117	117	E8	E8	PD3	I/O	FT	-	SPI2_SCK, DCMI_D5, SPI2_MISO, DFSDM1_DATIN0, USART2_CTS, QUADSPI_BK2_NCS, FMC_CLK, EVENTOUT	-
-	B4	C5	85	B7	118	118	C7	C7	PD4	I/O	FT	-	SPI2_MOSI, DFSDM1_CKIN0, USART2_RTS_DE, QUADSPI_BK2_IO0, FMC_NOE, EVENTOUT	-
-	E5	B4	86	A6	119	119	D7	D7	PD5	I/O	FT	-	USART2_TX, QUADSPI_BK2_IO1, FMC_NWE, EVENTOUT	-
-	-	-	-	-	120	120	-	-	VSS	S	-	-	-	-

Table 15. STM32L496xx pin definitions (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP100	WLCSP100_SMPS	LQFP100	UFBGA132	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
61	B8	B8	95	A3	139	138	C4	C4	PB8	I/O	FT_fl	-	TIM4_CH3, I2C1_SCL, DFSDM1_DATIN6, CAN1_RX, DCMI_D6, LCD_SEG16, SDMMC1_D4, SAI1_MCLK_A, TIM16_CH1, EVENTOUT	-
62	A8	A8	96	B3	140	139	D4	D4	PB9	I/O	FT_fl	-	IR_OUT, TIM4_CH4, I2C1_SDA, SPI2_NSS, DFSDM1_CKIN6, CAN1_TX, DCMI_D7, LCD_COM3, SDMMC1_D5, SAI1_FS_A, TIM17_CH1, EVENTOUT	-
-	-	-	-	-	-	-	-	C6	VDD12	S	-	-	-	-
-	-	-	97	C3	141	140	A4	A4	PE0	I/O	FT_l	-	TIM4_ETR, DCMI_D2, LCD_SEG36, FMC_NBL0, TIM16_CH1, EVENTOUT	-
-	-	-	98	A2	142	141	B4	B4	PE1	I/O	FT_l	-	DCMI_D3, LCD_SEG37, FMC_NBL1, TIM17_CH1, EVENTOUT	-
-	-	A9	-	-	-	142	-	-	VDD12	S	-	-	-	-
63	A9	B9	99	D3	143	143	B3	B3	VSS	S	-	-	-	-
64	A10	A10	100	C4	144	144	A3	A3	VDD	S	-	-	-	-
-	-	-	-	-	-	-	C2	C2	VSS	S	-	-	-	-
-	-	-	-	-	-	-	C1	C1	VDD	S	-	-	-	-
-	-	-	-	-	-	-	A2	A2	PH2	I/O	FT	-	QUADSPI_BK2_IO0, EVENTOUT	-

1. OPAMPx_VINM pins are not available as additional functions on pins PA1 and PA7 on UFBGA packages. On UFBGA packages, use the OPAMPx_VINM dedicated pins available on M3 and M4 balls.

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 16*)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	CAN2/ OTG_FS/DCMI/ QUADSPI	LCD	SDMMC/ COMP1/2/FMC/SWPMI1	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port A	PA0	UART4_TX	-	-	-	-	SAI1_EXTCLK	TIM2_ETR	EVENTOUT
	PA1	UART4_RX	-	-	LCD_SEG0	-	-	TIM15_CH1N	EVENTOUT
	PA2	LPUART1_TX	-	QUADSPI_BK1_NCS	LCD_SEG1	-	SAI2_EXTCLK	TIM15_CH1	EVENTOUT
	PA3	LPUART1_RX	-	QUADSPI_CLK	LCD_SEG2	-	SAI1_MCLK_A	TIM15_CH2	EVENTOUT
	PA4	-	-	DCMI_HSYNC	-	-	SAI1_FS_B	LPTIM2_OUT	EVENTOUT
	PA5	-	-	-	-	-	-	LPTIM2_ETR	EVENTOUT
	PA6	LPUART1_CTS	-	QUADSPI_BK1_IO3	LCD_SEG3	TIM1_BKIN_COMP2	TIM8_BKIN_COMP2	TIM16_CH1	EVENTOUT
	PA7	-	-	QUADSPI_BK1_IO2	LCD_SEG4	-	-	TIM17_CH1	EVENTOUT
	PA8	-	-	OTG_FS_SOF	LCD_COM0	SWPMI1_IO	SAI1_SCK_A	LPTIM2_OUT	EVENTOUT
	PA9	-	-	-	LCD_COM1	-	SAI1_FS_A	TIM15_BKIN	EVENTOUT
	PA10	-	-	OTG_FS_ID	LCD_COM2	-	SAI1_SD_A	TIM17_BKIN	EVENTOUT
	PA11	-	CAN1_RX	OTG_FS_DM	-	TIM1_BKIN2_COMP1	-	-	EVENTOUT
	PA12	-	CAN1_TX	OTG_FS_DP	-	-	-	-	EVENTOUT
	PA13	-	-	OTG_FS_NOE	-	SWPMI1_TX	SAI1_SD_B	-	EVENTOUT
	PA14	-	-	OTG_FS_SOF	-	SWPMI1_RX	SAI1_FS_B	-	EVENTOUT
	PA15	UART4_RTS_DE	TSC_G3_IO1	-	LCD_SEG17	SWPMI1_SUSPEND	SAI2_FS_B	-	EVENTOUT

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 16*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 17*.

Figure 16. Pin loading conditions

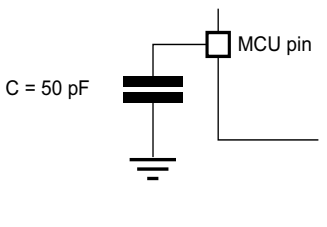
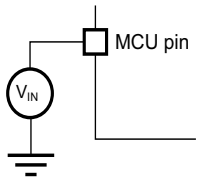
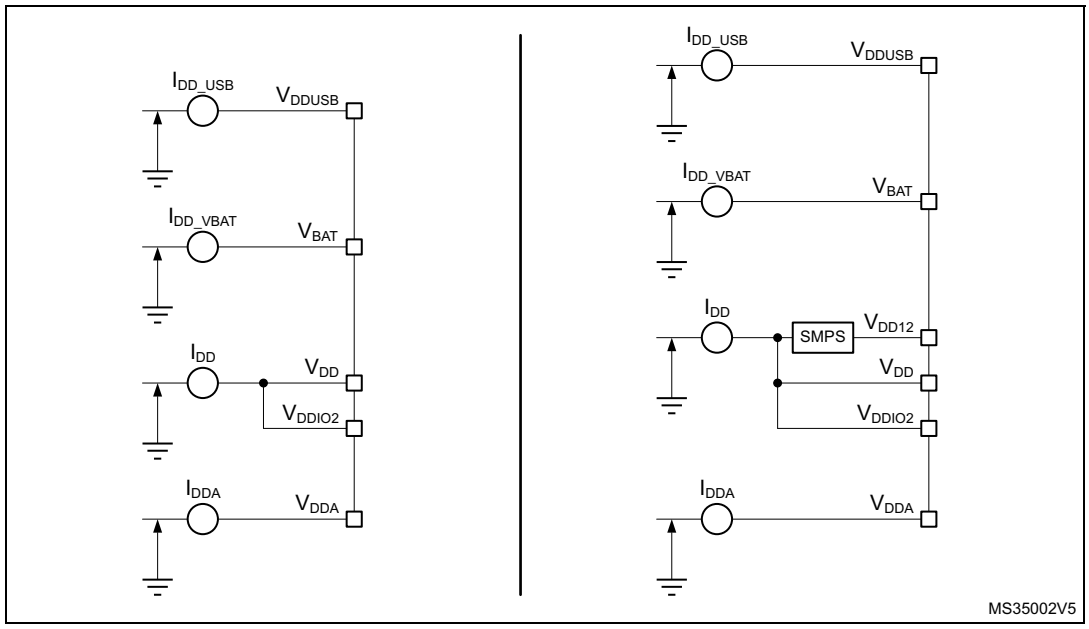


Figure 17. Pin input voltage



6.1.7 Current consumption measurement

Figure 19. Current consumption measurement scheme with and without external SMPS power supply



The current consumption for RUN modes and Low Power modes is measured on IDD_ALL = IDD + IDDA + IDD_USB + IDD_VBAT unless otherwise specified.

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 19: Voltage characteristics*, *Table 20: Current characteristics* and *Table 21: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

Table 44. Current consumption in Stop 2 mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL}(wake up from Stop2)	Supply current during wakeup from Stop 2 mode	Wakeup clock is MSI = 48 MHz, voltage Range 1. See (4).	3 V	1.69	-	-	-	-	-	-	-	-	-	mA
		Wakeup clock is MSI = 4 MHz, voltage Range 2. See (4).	3 V	1.35	-	-	-	-	-	-	-	-	-	
		Wakeup clock is HSI16 = 16 MHz, voltage Range 1. See (4).	3 V	1.7	-	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. LCD enabled with external voltage source. Consumption from VLCD excluded. Refer to LCD controller characteristics for I_{VLCD}.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 51: Low-power mode wakeup timings*.

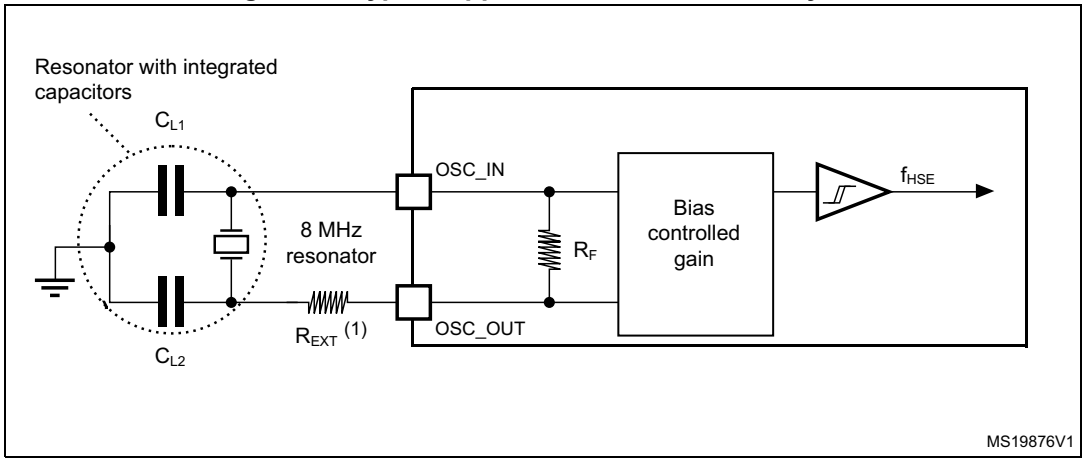
Table 47. Current consumption in Standby mode (continued)

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Standby with RTC)	Supply current in Standby mode (backup registers retained), RTC enabled	RTC clocked by LSE bypassed at 32768Hz	1.8 V	308	504	1483	3793	9883	-	-	-	-	-	nA
			2.4 V	400	633	1763	4457	11483	-	-	-	-	-	
			3 V	508	779	2119	5325	13730	-	-	-	-	-	
			3.6 V	661	1009	2625	6427	16140	-	-	-	-	-	
		RTC clocked by LSE quartz (3) in low drive mode	1.8 V	426	624	1679	4244	10884	-	-	-	-	-	
			2.4 V	521	751	1985	4952	12619	-	-	-	-	-	
			3 V	643	914	2371	5931	15121	-	-	-	-	-	
			3.6 V	819	1162	2914	7019	17551	-	-	-	-	-	
I_{DD_ALL} (SRAM2)(4)	Supply current to be added in Standby mode when SRAM2 is retained	-	1.8 V	371	1111	4297	10153	22747	-	-	-	-	-	nA
			2.4 V	372	1112	4328	10154	22888	-	-	-	-	-	
			3 V	374	1116	4403	10429	23711	-	-	-	-	-	
			3.6 V	378	1149	4545	10702	24361	-	-	-	-	-	
I_{DD_ALL} (wakeup from Standby)	Supply current during wakeup from Standby mode	Wakeup clock is MSI = 4 MHz. See (5).	3 V	1.4	-	-	-	-	-	-	-	-	-	mA

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. The supply current in Standby with SRAM2 mode is: I_{DD_ALL}(Standby) + I_{DD_ALL}(SRAM2). The supply current in Standby with RTC with SRAM2 mode is: II_{DD_ALL}(Standby + RTC) + I_{DD_ALL}(SRAM2).
5. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 51: Low-power mode wakeup timings*.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 23. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 57*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 57. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

Figure 25. HSI16 frequency versus temperature

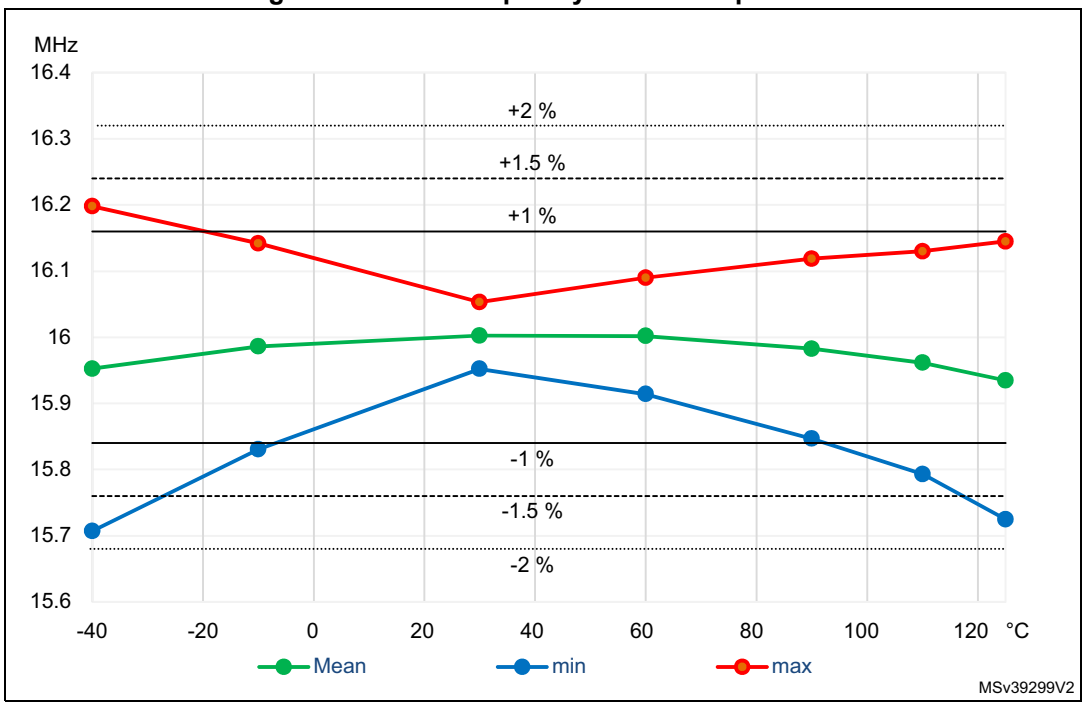
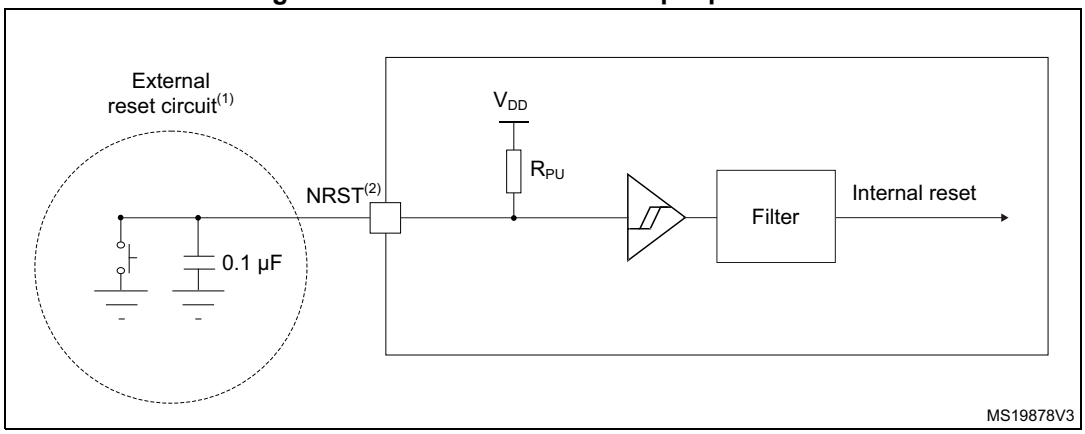


Figure 30. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 73: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

6.3.16 Analog switches booster

Table 74. Analog switches booster characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.62	-	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	240	µs
$I_{DD(BOOST)}$	Booster consumption for 1.62 V ≤ V_{DD} ≤ 2.0 V	-	-	250	µA
	Booster consumption for 2.0 V ≤ V_{DD} ≤ 2.7 V	-	-	500	
	Booster consumption for 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	900	

1. Guaranteed by design.

Table 85. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{LOAD}	Drive current	Normal mode	$V_{DDA} \geq 2$ V	-	-	500	µA
		Low-power mode		-	-	100	
I_{LOAD_PGA}	Drive current in PGA mode	Normal mode	$V_{DDA} \geq 2$ V	-	-	450	
		Low-power mode		-	-	50	
R_{LOAD}	Resistive load (connected to VSSA or to VDDA)	Normal mode	$V_{DDA} < 2$ V	4	-	-	kΩ
		Low-power mode		20	-	-	
R_{LOAD_PGA}	Resistive load in PGA mode (connected to VSSA or to V_{DDA})	Normal mode	$V_{DDA} < 2$ V	4.5	-	-	
		Low-power mode		40	-	-	
C_{LOAD}	Capacitive load	-		-	-	50	pF
CMRR	Common mode rejection ratio	Normal mode		-	-85	-	dB
		Low-power mode		-	-90	-	
PSRR	Power supply rejection ratio	Normal mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 4$ kΩ DC	70	85	-	dB
		Low-power mode	$C_{LOAD} \leq 50$ pf, $R_{LOAD} \geq 20$ kΩ DC	72	90	-	
GBW	Gain Bandwidth Product	Normal mode	$V_{DDA} \geq 2.4$ V (OPA_RANGE = 1)	550	1600	2200	kHz
		Low-power mode		100	420	600	
		Normal mode	$V_{DDA} < 2.4$ V (OPA_RANGE = 0)	250	700	950	
		Low-power mode		40	180	280	
SR(2)	Slew rate (from 10 and 90% of output voltage)	Normal mode	$V_{DDA} \geq 2.4$ V	-	700	-	V/ms
		Low-power mode		-	180	-	
		Normal mode	$V_{DDA} < 2.4$ V	-	300	-	
		Low-power mode		-	80	-	
AO	Open loop gain	Normal mode		55	110	-	dB
		Low-power mode		45	110	-	
V_{OHSAT}(2)	High saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at V_{DDA}.	V_{DDA} - 100	-	-	mV
		Low-power mode		V_{DDA} - 50	-	-	
V_{OLSAT}(2)	Low saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at 0.	-	-	100	
		Low-power mode		-	-	50	
φ_m	Phase margin	Normal mode		-	74	-	°
		Low-power mode		-	66	-	

6.3.22 Temperature sensor characteristics

Table 86. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope(2)	Average slope	2.3	2.5	2.7	mV/°C
V_{30}	Voltage at 30°C (±5 °C)(3)	0.742	0.76	0.785	V
t_{START} (TS_BUF)(1)	Sensor Buffer Start-up time in continuous mode(4)	-	8	15	µs
t_{START}(1)	Start-up time when entering in continuous mode(4)	-	70	120	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	5	-	-	µs
I_{DD}(TS)(1)	Temperature sensor consumption from V_{DD}, when selected by ADC	-	4.7	7	µA

1. Guaranteed by design.
2. Guaranteed by characterization results.
3. Measured at V_{DDA} = 3.0 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 8: Temperature sensor calibration values*.
4. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

6.3.23 V_{BAT} monitoring characteristics

Table 87. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er(1)	Error on Q	-10	-	10	%
t_{S_vbat}(1)	ADC sampling time when reading the VBAT	12	-	-	µs

1. Guaranteed by design.

Table 88. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

Table 91. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 80 MHz	12.5	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 80 MHz	0	40	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2 and TIM5)	-	16	bit
		TIM2 and TIM5	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 80 MHz	0.0125	819.2	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 80 MHz	-	53.68	s

1. TIMx is used as a general term in which x stands for 1,2,3,4,5,6,7,8,15,16 or 17.

Table 92. IWDG min/max timeout period at 32 kHz (LSI)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

1. The exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 93. WWDG min/max timeout value at 80 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0512	3.2768	ms
2	1	0.1024	6.5536	
4	2	0.2048	13.1072	
8	3	0.4096	26.2144	

Table 95. SPI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 V < V_{DD} < 3.6 V Voltage Range 1	-	13	15.5	ns
		Slave mode 1.71 V < V_{DD} < 3.6 V Voltage Range 1	-	13	26.5	
		Slave mode 1.71 V < V_{DD} < 3.6 V Voltage Range 2	-	13	30	
-		Slave mode 1.08 V < V_{DDIO2} < 1.32 V(3)	-	26	60	
$t_{v(MO)}$		Master mode	-	4.5	6	
th(SO)	Data output hold time	Slave mode 1.71 V < V_{DD} < 3.6 V	7	-	-	
th(MO)		Master mode	0	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50 %.
3. SPI mapped on Port G.

Figure 34. SPI timing diagram - slave mode and CPHA = 0

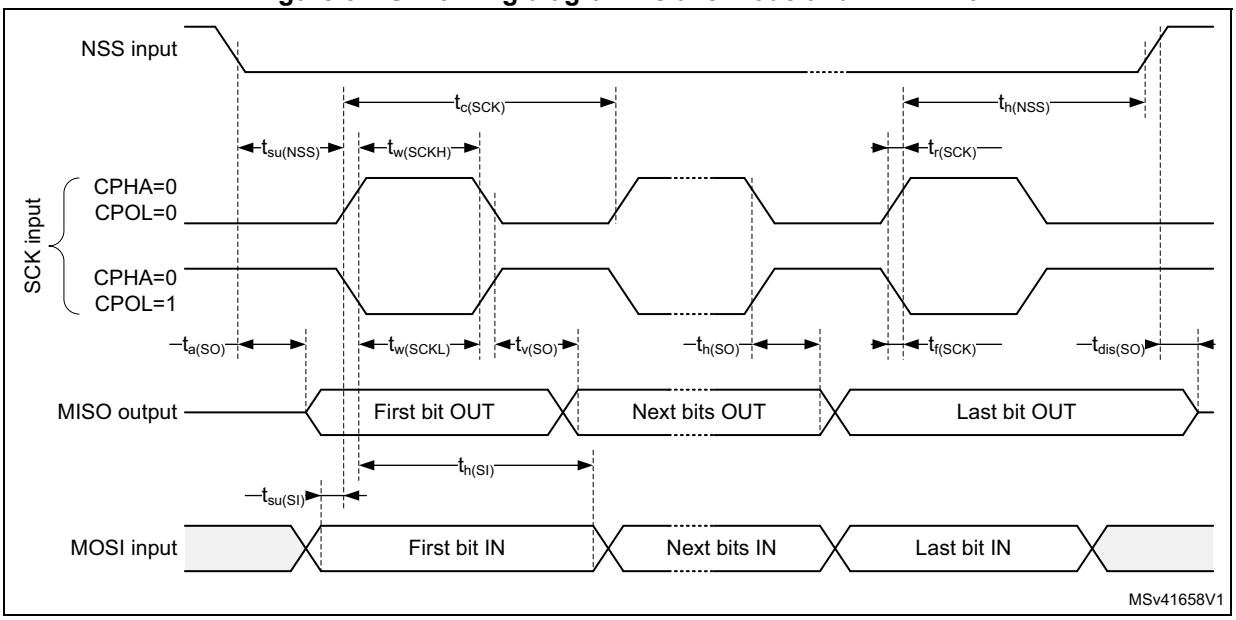


Table 113. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{HCLK}$-0.5	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	T_{HCLK}+0.5	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	4	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	0	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	T_{HCLK}+1	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	3	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	1.5	-	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	T_{HCLK}+0.5	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	3.5	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

NAND controller waveforms and timings

Figure 51 through *Figure 54* represent synchronous waveforms, and *Table 114* and *Table 115* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01
- COM.FMC_WaitSetupTime = 0x03
- COM.FMC_HoldSetupTime = 0x02
- COM.FMC_HiZSetupTime = 0x01
- ATT.FMC_SetupTime = 0x01
- ATT.FMC_WaitSetupTime = 0x03
- ATT.FMC_HoldSetupTime = 0x02
- ATT.FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0

In all timing tables, the T_{HCLK} is the HCLK clock period.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in *Table 129* T_{Jmax} is calculated as follows:

– For LQFP100, 42 °C/W

T_{Jmax} = 82 °C + (42 °C/W × 447 mW) = 82 °C + 18.774 °C = 100.774 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C) see *Section 8: Part numbering*.

In this case, parts must be ordered at least with the temperature range suffix 6 (see Part numbering).

Note: With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6: T_{Amax} = T_{Jmax} - (42°C/W × 447 mW) = 105-18.774 = 86.226 °C

Suffix 7: T_{Amax} = T_{Jmax} - (42°C/W × 447 mW) = 125-18.774 = 106.226 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 129* T_{Jmax} is calculated as follows:

– For LQFP100, 42 °C/W

T_{Jmax} = 100 °C + (42 °C/W × 134 mW) = 100 °C + 5.628 °C = 105.628 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).