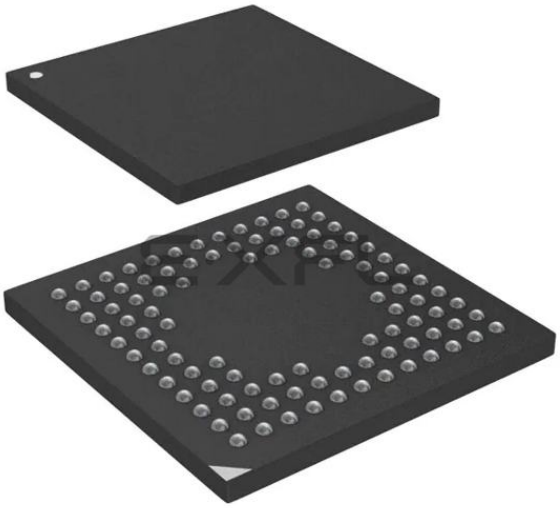

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	83
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA, WLCSP
Supplier Device Package	100-WLCSP (4.62x4.14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l496vgy6ptr

3.4 Embedded Flash memory

STM32L496xx devices feature up to 1 Mbyte of embedded Flash memory available for storing programs and data. The Flash memory is divided into two banks allowing read-while-write operations. This feature allows to perform a read operation from one bank while an erase or program operation is performed to the other bank. The dual bank boot is also supported. Each bank contains 256 pages of 2 Kbyte.

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP) to protect the whole memory. Three levels are available:
  - Level 0: no readout protection
  - Level 1: memory readout protection: the Flash memory cannot be read from or written to if either debug features are connected, boot in RAM or bootloader is selected
  - Level 2: chip readout protection: debug features (Cortex-M4 JTAG and serial wire), boot in RAM and bootloader selection are disabled (JTAG fuse). This selection is irreversible.

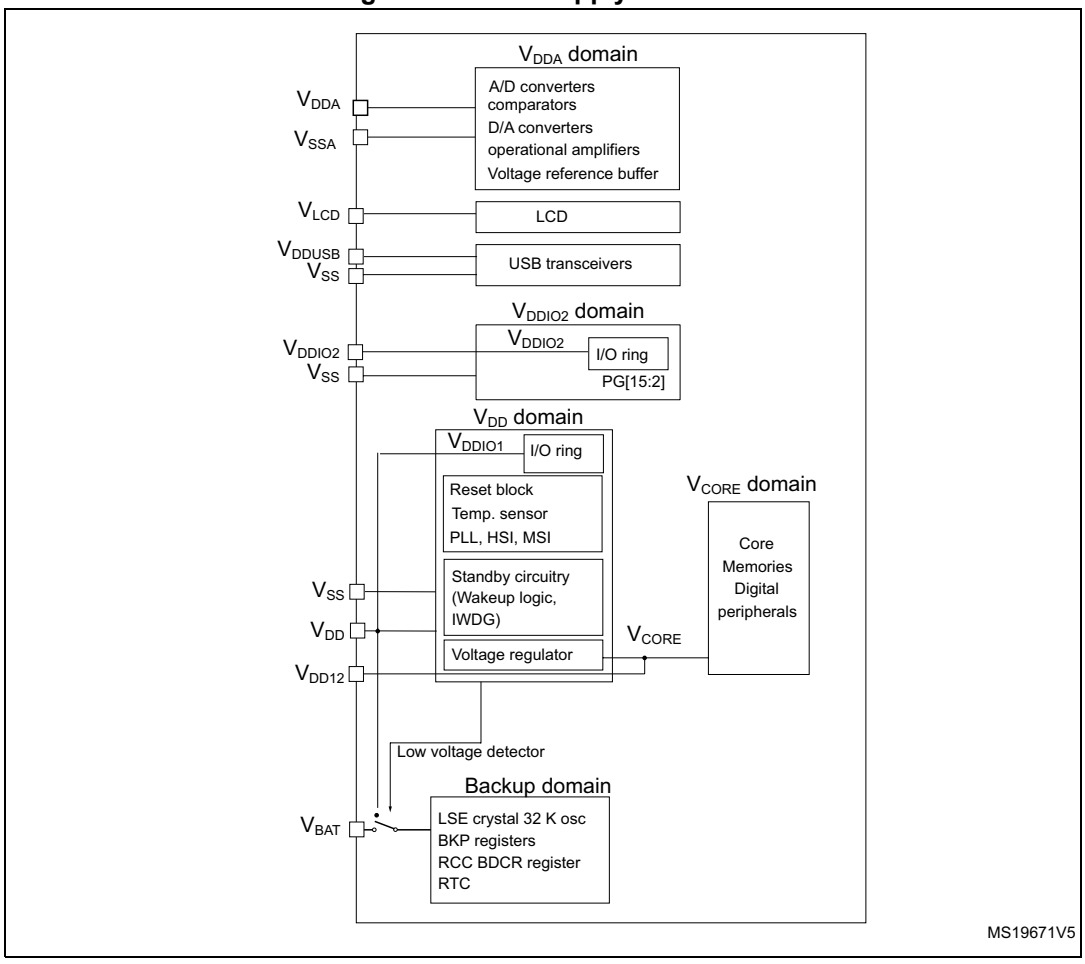
Table 3. Access status versus readout protection level and execution modes

Area	Protection level	User execution			Debug, boot from RAM or boot from system memory (loader)		
		Read	Write	Erase	Read	Write	Erase
Main memory	1	Yes	Yes	Yes	No	No	No
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes	1	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	No	No	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A(1)	No	No	N/A(1)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	Yes(1)	No	No	No(1)
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. Erased when RDP change from Level 1 to Level 0.

- Write protection (WRP): the protected area is protected against erasing and programming. Two areas per bank can be selected, with 2-Kbyte granularity.
- Proprietary code readout protection (PCROP): a part of the flash memory can be protected against read and write from third parties. The protected area is execute-only: it can only be reached by the STM32 CPU, as an instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited. One area per bank can be selected, with 64-bit granularity. An additional option bit (PCROP_RDP) allows to select if the PCROP area is erased or not when the RDP protection is changed from Level 1 to Level 0.

Figure 3. Power supply overview



3.10.2 Power supply supervisor

The device has an integrated ultra-low-power brown-out reset (BOR) active in all modes except Shutdown and ensuring proper operation after power-on and during power down. The device remains in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71V at power on, and other higher thresholds can be selected through option bytes.The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold. An interrupt can be generated when V_{DD} drops below the VPVD threshold and/or when V_{DD} is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the device embeds a Peripheral Voltage Monitor which compares the independent supply voltages V_{DDA}, V_{DDUSB}, V_{DDIO2} with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

3.10.3 Voltage regulator

Two embedded linear voltage regulators supply most of the digital circuitries: the main regulator (MR) and the low-power regulator (LPR).

- The MR is used in the Run and Sleep modes and in the Stop 0 mode.
- The LPR is used in Low-Power Run, Low-Power Sleep, Stop 1 and Stop 2 modes. It is also used to supply the 64 Kbyte SRAM2 in Standby with RAM2 retention.
- Both regulators are in power-down in Standby and Shutdown modes: the regulator output is in high impedance, and the kernel circuitry is powered down thus inducing zero consumption.

The ultralow-power STM32L496xx supports dynamic voltage scaling to optimize its power consumption in run mode. The voltage from the Main Regulator that supplies the logic (VCORE) can be adjusted according to the system's maximum operating frequency.

There are two power consumption ranges:

- Range 1 with the CPU running at up to 80 MHz.
- Range 2 with a maximum CPU frequency of 26 MHz. All peripheral clocks are also limited to 26 MHz.

The VCORE can be supplied by the low-power regulator, the main regulator being switched off. The system is then in Low-power run mode.

- Low-power run mode with the CPU running at up to 2 MHz. Peripherals with independent clock can be clocked by HSI16.

When the MR is in use, the STM32L496xx with the external SMPS option allows to force an external VCORE supply on the VDD12 supply pins.

When VDD12 is forced by an external source and is higher than the output of the internal LDO, the current is taken from this external supply and the overall power efficiency is significantly improved if using an external step down DC/DC converter.

3.10.4 Low-power modes

The ultra-low-power STM32L496xx supports seven low-power modes to achieve the best compromise between low-power consumption, short startup time, available peripherals and available wakeup sources:

3.13 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.14 Direct memory access controller (DMA)

The device embeds 2 DMAs. Refer to *Table 7: DMA implementation* for the features implementation.

Direct memory access (DMA) is used in order to provide high-speed data transfer between peripherals and memory as well as memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps CPU resources free for other operations.

The two DMA controllers have 14 channels in total, each dedicated to managing memory access requests from one or more peripherals. Each has an arbiter for handling the priority between DMA requests.

The DMA supports:

- 14 independently configurable channels (requests)
- Each channel is connected to dedicated hardware DMA requests, software trigger is also supported on each channel. This configuration is done by software.
- Priorities between requests from channels of one DMA are software programmable (4 levels consisting of very high, high, medium, low) or hardware in case of equality (request 1 has priority over request 2, etc.)
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size.
- Support for circular buffer management
- 3 event flags (DMA Half Transfer, DMA Transfer complete and DMA Transfer Error) logically ORed together in a single interrupt request for each channel
- Memory-to-memory transfer
- Peripheral-to-memory and memory-to-peripheral, and peripheral-to-peripheral transfers
- Access to Flash, SRAM, APB and AHB peripherals as source and destination
- Programmable number of data to be transferred: up to 65536.

Table 7. DMA implementation

DMA features	DMA1	DMA2
Number of regular channels	7	7

Table 13. SAI implementation

SAI features(1)	SAI1	SAI2
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	X	X
Mute mode	X	X
Stereo/Mono audio frame capability.	X	X
16 slots	X	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit	X	X
FIFO Size	X (8 Word)	X (8 Word)
SPDIF	X	X

1. X: supported

3.34 Single wire protocol master interface (SWPMI)

The Single wire protocol master interface (SWPMI) is the master interface corresponding to the Contactless Frontend (CLF) defined in the ETSI TS 102 613 technical specification. The main features are:

- full-duplex communication mode
- automatic SWP bus state management (active, suspend, resume)
- configurable bitrate up to 2 Mbit/s
- automatic SOF, EOF and CRC handling

SWPMI can be served by the DMA controller.

3.35 Controller area network (CAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bit rate up to 1Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). 256 bytes of SRAM are allocated for each CAN.

The synchronization for this oscillator can also be taken from the USB data stream itself (SOF signalization) which allows crystal less operation.

The major features are:

- Combined Rx and Tx FIFO size of 1.25 KB with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 1 bidirectional control endpoint + 5 IN endpoints + 5 OUT endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- Software configurable to OTG 1.3 and OTG 2.0 modes of operation
- OTG 2.0 Supports ADP (Attach detection Protocol)
- USB 2.0 LPM (Link Power Management) support
- Battery Charging Specification Revision 1.2 support
- Internal FS OTG PHY support

For OTG/Host modes, a power switch is needed in case bus-powered devices are connected.

3.38 Clock recovery system (CRS)

The STM32L496xx devices embed a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.39 Flexible static memory controller (FSMC)

The Flexible static memory controller (FSMC) includes two memory controllers:

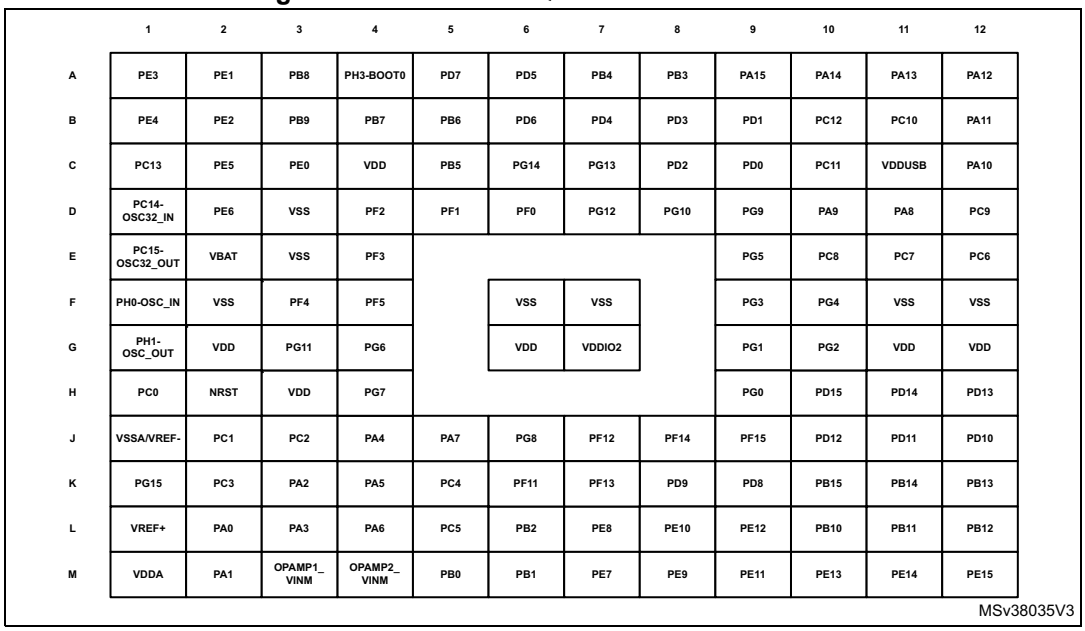
- The NOR/PSRAM memory controller
- The NAND/memory controller

This memory controller is also named Flexible memory controller (FMC).

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM (4 memory banks)
  - NAND Flash memory with ECC hardware to check up to 8 Kbyte of data
- 8-,16- bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- The Maximum FMC_CLK frequency for synchronous accesses is HCLK/2.

Figure 10. STM32L496Qx UFBGA132 ballout(1)



1. The above figure shows the package top view.

Table 15. STM32L496xx pin definitions (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP100	WLCSP100_SMPS	LQFP100	UFBGA132	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
-	H5	H5	41	L8	63	63	H7	H7	PE10	I/O	FT	-	TIM1_CH2N, DFSDM1_DATIN4, TSC_G5_IO1, QUADSPI_CLK, FMC_D7, SAI1_MCLK_B, EVENTOUT	-
-	K4	K4	42	M9	64	64	N8	N8	PE11	I/O	FT	-	TIM1_CH2, DFSDM1_CKIN4, TSC_G5_IO2, QUADSPI_BK1_NCS, FMC_D8, EVENTOUT	-
-	G5	J4	43	L9	65	65	M8	M8	PE12	I/O	FT	-	TIM1_CH3N, SPI1_NSS, DFSDM1_DATIN5, TSC_G5_IO3, QUADSPI_BK1_IO0, FMC_D9, EVENTOUT	-
-	G4	G5	44	M10	66	66	L8	L8	PE13	I/O	FT	-	TIM1_CH3, SPI1_SCK, DFSDM1_CKIN5, TSC_G5_IO4, QUADSPI_BK1_IO1, FMC_D10, EVENTOUT	-
-	J4	G4	45	M11	67	67	K8	K8	PE14	I/O	FT	-	TIM1_CH4, TIM1_BKIN2, TIM1_BKIN2_COMP2, SPI1_MISO, QUADSPI_BK1_IO2, FMC_D11, EVENTOUT	-
-	H4	H4	46	M12	68	68	J8	J8	PE15	I/O	FT	-	TIM1_BKIN, TIM1_BKIN_COMP1, SPI1_MOSI, QUADSPI_BK1_IO3, FMC_D12, EVENTOUT	-
29	K3	K3	47	L10	69	69	N9	N9	PB10	I/O	FT_fl	-	TIM2_CH3, I2C4_SCL, I2C2_SCL, SPI2_SCK, DFSDM1_DATIN7, USART3_TX, LPUART1_RX, TSC_SYNC, QUADSPI_CLK, LCD_SEG10, COMP1_OUT, SAI1_SCK_A, EVENTOUT	-
30	J3	J3	48	L11	70	-	H8	H8	PB11	I/O	FT_fl	-	TIM2_CH4, I2C4_SDA, I2C2_SDA, DFSDM1_CKIN7, USART3_RX, LPUART1_TX, QUADSPI_BK1_NCS, LCD_SEG11, COMP2_OUT, EVENTOUT	-
-	-	K1	-	-	-	70	-	M10	VDD12	S	-	-	-	-

Table 15. STM32L496xx pin definitions (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP100	WLCSP100_SMPS	LQFP100	UFBGA132	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
45	C1	C1	71	A12	104	104	D13	D13	PA12	I/O	FT_u	-	TIM1_ETR, SPI1_MOSI, USART1_RTS_DE, CAN1_TX, OTG_FS_DP, EVENTOUT	-
46	C2	C2	72	A11	105	105	A11	A11	PA13 (JTMS/SWDIO)	I/O	FT	-	JTMS/SWDIO, IR_OUT, OTG_FS_NOE, SWPMI1_TX, SAI1_SD_B, EVENTOUT	-
47	B1	B1	-	-	-	-	-	-	VSS	S	-	-	-	-
48	A1	A1	73	C11	106	106	E12	E12	VDDUSB	S	-	-	-	-
-	-	-	74	F11	107	107	C12	C12	VSS	S	-	-	-	-
-	-	-	75	G11	108	108	C13	C13	VDD	S	-	-	-	-
-	-	-	-	-	-	-	E11	E11	PH6	I/O	FT	-	I2C2_SMBA, DCMI_D8, EVENTOUT	-
-	-	-	-	-	-	-	D12	D12	PH7	I/O	FT_f	-	I2C3_SCL, DCMI_D9, EVENTOUT	-
-	-	-	-	-	-	-	D11	D11	PH9	I/O	FT	-	I2C3_SMBA, DCMI_D0, EVENTOUT	-
-	-	-	-	-	-	-	B13	B13	PH12	I/O	FT	-	TIM5_CH3, DCMI_D3, EVENTOUT	-
-	-	-	-	-	-	-	A13	A13	PH14	I/O	FT	-	TIM8_CH2N, DCMI_D4, EVENTOUT	-
-	-	-	-	-	-	-	B12	B12	PH15	I/O	FT	-	TIM8_CH3N, DCMI_D11, EVENTOUT	-
-	-	-	-	-	-	-	A12	A12	PI0	I/O	FT	-	TIM5_CH4, SPI2_NSS, DCMI_D13, EVENTOUT	-

Table 17. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 16*) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		UART4/5/ LPUART1/ CAN2	CAN1/TSC	CAN2/ OTG_FS/DCMI/ QUADSPI	LCD	SDMMC/ COMP1/2/FMC/SWPMI1	SAI1/2	TIM2/15/16/17/ LPTIM2	EVENOUT
Port I	PI0	-	-	DCMI_D13	-	-	-	-	EVENTOUT
	PI1	-	-	DCMI_D8	-	-	-	-	EVENTOUT
	PI2	-	-	DCMI_D9	-	-	-	-	EVENTOUT
	PI3	-	-	DCMI_D10	-	-	-	-	EVENTOUT
	PI4	-	-	DCMI_D5	-	-	-	-	EVENTOUT
	PI5	-	-	DCMI_VSYNC	-	-	-	-	EVENTOUT
	PI6	-	-	DCMI_D6	-	-	-	-	EVENTOUT
	PI7	-	-	DCMI_D7	-	-	-	-	EVENTOUT
	PI8	-	-	DCMI_D12	-	-	-	-	EVENTOUT
	PI9	-	CAN1_RX	-	-	-	-	-	EVENTOUT
	PI10	-	-	-	-	-	-	-	EVENTOUT
	PI11	-	-	-	-	-	-	-	EVENTOUT

3. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
4. Positive injection (when $V_{IN} > V_{DDIOx}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 19: Voltage characteristics* for the minimum allowed input voltage values.
6. When several inputs are submitted to a current injection, the maximum $\sum|I_{INJ(PIN)}|$ is the absolute sum of the negative injected currents (instantaneous values).

Table 21. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 22. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	80	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	80	
f_{PCLK2}	Internal APB2 clock frequency	-	0	80	
V_{DD}	Standard operating voltage	-	1.71 (1)	3.6	V
VDD12	Standard operating voltage	full frequency range	1.08	1.32	
		up to 26MHz	1.05		
V_{DDIO2}	PG[15:2] I/Os supply voltage	At least one I/O in PG[15:2] used	1.08	3.6	V
		PG[15:2] not used	0	3.6	
V_{DDA}	Analog supply voltage	ADC or COMP used	1.62	3.6	V
		DAC or OPAMP used	1.8		
		VREFBUF used	2.4		
		ADC, DAC, OPAMP, COMP, VREFBUF not used	0		

Table 24. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
V_{PVD2}	PVD threshold 2	Rising edge	2.41	2.46	2.51	V
		Falling edge	2.31	2.36	2.41	
V_{PVD3}	PVD threshold 3	Rising edge	2.56	2.61	2.66	V
		Falling edge	2.47	2.52	2.57	
V_{PVD4}	PVD threshold 4	Rising edge	2.69	2.74	2.79	V
		Falling edge	2.59	2.64	2.69	
V_{PVD5}	PVD threshold 5	Rising edge	2.85	2.91	2.96	V
		Falling edge	2.75	2.81	2.86	
V_{PVD6}	PVD threshold 6	Rising edge	2.92	2.98	3.04	V
		Falling edge	2.84	2.90	2.96	
V_{hyst_BORH0}	Hysteresis voltage of BORH0	Hysteresis in continuous mode	-	20	-	mV
		Hysteresis in other mode	-	30	-	
$V_{hyst\_BOR\_PVD}$	Hysteresis voltage of BORH (except BORH0) and PVD	-	-	100	-	mV
I_{DD} (BOR_PVD)[2]	BOR[3] (except BOR0) and PVD consumption from V_{DD}	-	-	1.1	1.6	µA
V_{PVM3}	V_{DDA} peripheral voltage monitoring	Rising edge	1.61	1.65	1.69	V
		Falling edge	1.6	1.64	1.68	
V_{PVM4}	V_{DDA} peripheral voltage monitoring	Rising edge	1.78	1.82	1.86	V
		Falling edge	1.77	1.81	1.85	
V_{hyst_PVM3}	PVM3 hysteresis	-	-	10	-	mV
V_{hyst_PVM4}	PVM4 hysteresis	-	-	10	-	mV
I_{DD} (PVM1/PVM2) (2)	PVM1 and PVM2 consumption from V_{DD}	-	-	0.2	-	µA
I_{DD} (PVM3/PVM4) (2)	PVM3 and PVM4 consumption from V_{DD}	-	-	2	-	µA

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.
2. Guaranteed by design.
3. BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.

Figure 20. V_{REFINT} versus temperature

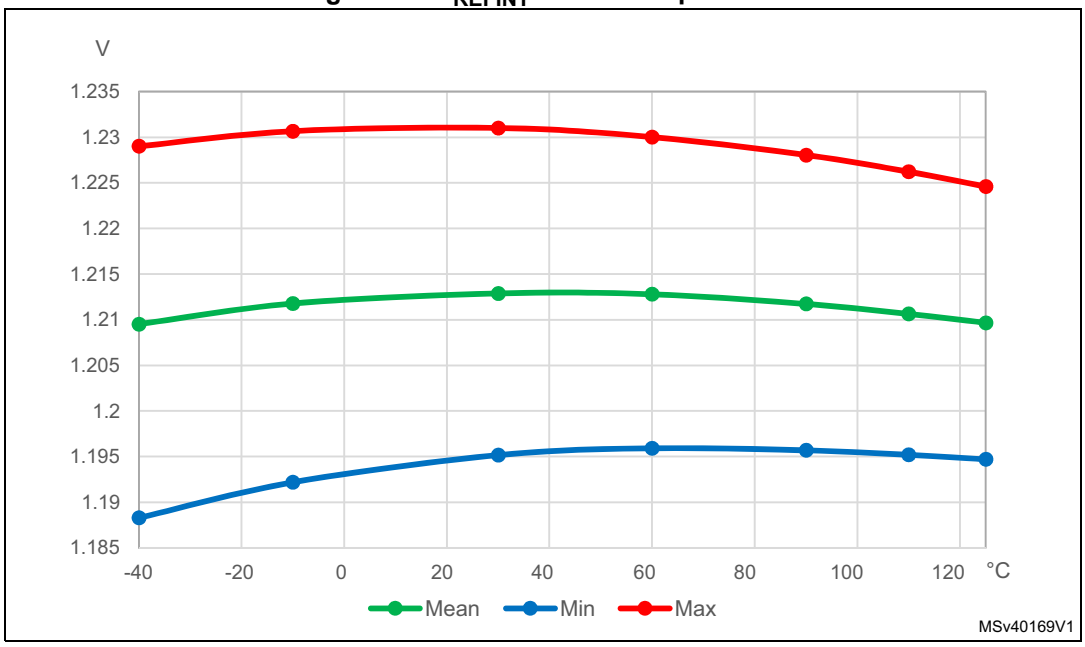


Table 36. Typical current consumption in Run modes, with different codesrunning from Flash, ART disable and power supplied by external SMPS (VDD12 = 1.10 V)

Symbol	Parameter	Conditions(1)			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	f_{HCLK} = 26 MHz	Reduced code(2)	1.34	mA	51	µA/MHz
				Coremark	1.23		47	
				Dhrystone 2.1	1.23		47	
				Fibonacci	1.13		44	
				While(1)	1.04		40	
			f_{HCLK} = 80 MHz	Reduced code(1)	3.59		45	
				Coremark	3.35		42	
				Dhrystone 2.1	3.38		42	
				Fibonacci	3.11		39	
				While(1)	3.10		39	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, VDD12 = 1.10 V
2. Reduced code used for characterization results provided in *Table 26*, *Table 28*, *Table 30*.

Table 37. Typical current consumption in Run modes, with different codesrunning from Flash, ART disable and power supplied by external SMPS (VDD12 = 1.05 V)

Symbol	Parameter	Conditions(1)			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD_ALL} (Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals	f_{HCLK} = 26 MHz	Reduced code(2)	1.22	mA	47	µA/MHz
				Coremark	1.12		43	
				Dhrystone 2.1	1.12		43	
				Fibonacci	1.03		40	
				While(1)	0.95		37	

1. All values are obtained by calculation based on measurements done without SMPS and using following parameters: SMPS input = 3.3 V, SMPS efficiency = 85%, VDD12 = 1.05 V
2. Reduced code used for characterization results provided in *Table 26*, *Table 28*, *Table 30*.

Table 41. Current consumption in Sleep and Low-power sleep modes, Flash ON

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Sleep)	Supply current in sleep mode,	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode pll ON above 48 MHz all peripherals disable	Range 2	26 MHz	0.79	0.82	0.95	1.17	1.63	0.9	1.0	1.2	1.7	2.7	mA
				16 MHz	0.54	0.57	0.7	0.92	1.38	0.6	0.7	1.0	1.4	2.4	
				8 MHz	0.33	0.37	0.49	0.71	1.17	0.4	0.5	0.7	1.2	2.2	
				4 MHz	0.23	0.26	0.39	0.61	1.06	0.3	0.4	0.6	1.1	2.1	
				2 MHz	0.18	0.21	0.34	0.56	1.01	0.2	0.3	0.5	1.0	1.0	
				1 MHz	0.16	0.19	0.31	0.53	0.99	0.2	0.3	0.5	1.0	1.0	
				100 kHz	0.13	0.17	0.29	0.51	0.96	0.1	0.3	0.5	1.0	1.9	
			Range 1	80 MHz	2.57	2.62	2.76	3.01	3.53	2.8	2.9	3.2	3.8	4.9	
				72 MHz	2.34	2.38	2.53	2.78	3.29	2.6	2.7	3.0	3.5	4.6	
				64 MHz	2.1	2.15	2.29	2.54	3.05	2.3	2.4	2.7	3.3	4.4	
				48 MHz	1.58	1.63	1.78	2.03	2.54	1.8	1.9	2.2	2.7	3.8	
				32 MHz	1.11	1.15	1.3	1.54	2.05	1.2	1.4	1.7	2.2	3.3	
				24 MHz	0.87	0.91	1.06	1.3	1.81	1.0	1.1	1.4	1.9	3.0	
				16 MHz	0.63	0.67	0.82	1.06	1.56	0.7	0.8	1.1	1.6	2.7	
I_{DD_ALL} (LPSleep)	Supply current in low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	103	140	270	506	985	130	247	500	990	2025	µA
				1 MHz	74.2	111	245	476	955	100	215	467	963	1999	
				400 kHz	60	89.8	224	457	937	79	194	444	941	1975	
				100 kHz	53.7	84.1	216	448	928	70	185	434	933	1967	

1. Guaranteed by characterization results, unless otherwise specified.

Table 43. Current consumption in Low-power sleep modes, Flash in power-down

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (LPSleep)	Supply current in low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	92.7	124	258	487	968	105	224	474	969	2006	µA
				1 MHz	63.5	97.5	223	460	951	75	193	446	942	1975	
				400 kHz	42.6	75.6	207	443	947	54	171	426	923	1955	
				100 kHz	31.2	67.6	199	437	905	44	162	420	916	1947	

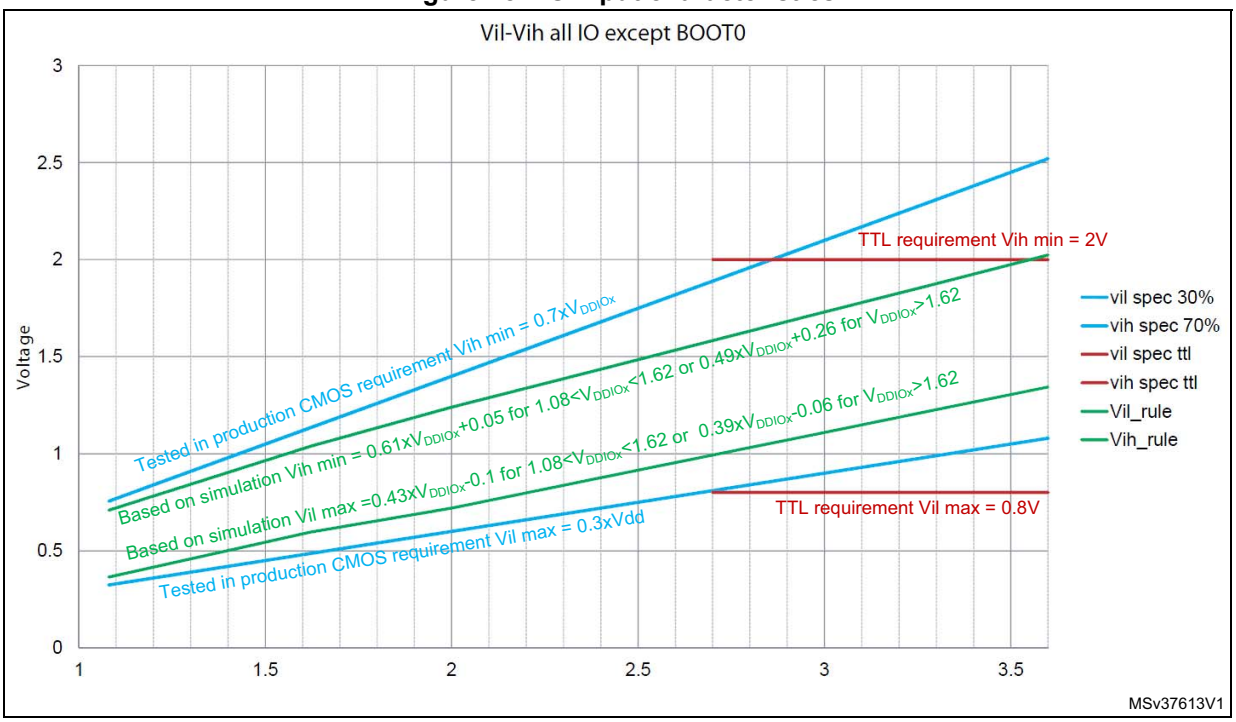
1. Guaranteed by characterization results, unless otherwise specified.

Table 44. Current consumption in Stop 2 mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Stop 2)	Supply current in Stop 2 mode, RTC disabled	LCD disabled	1.8 V	2.57	6.86	25.2	60.1	135	5.3	16.4	64	154.6	353	µA
			2.4 V	2.62	6.91	25.5	60.6	137	5.3	16.6	64.9	156.7	359	
			3 V	2.69	6.93	25.7	61.5	140	5.4	16.9	66.3	159.7	366	
			3.6 V	2.7	7.08	26.3	62.9	143	5.4	17.4	67.8	163.8	375	
		LCD enabled(2) clocked by LSI	1.8 V	2.92	7.19	25.3	59.5	135	5.3	16.6	64.8	155.6	355	
			2.4 V	2.99	7.3	25.6	60.3	136	5.5	16.8	65.9	157.9	360	
			3 V	3.04	7.41	26.1	61.7	140	5.9	17.3	67.1	160.8	367	
			3.6 V	3.31	7.7	26.8	63.2	143	6.2	17.9	69.1	165.0	376	

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 28* for standard I/Os, and in *Figure 28* for 5 V tolerant I/Os.

Figure 28. I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on V_{DDIOx}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 19: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 19: Voltage characteristics*).

Table 75. ADC characteristics(1) (2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3.0	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t_s	Sampling time	f_{ADC} = 80 MHz	0.03125	-	8.00625	µs
		-	2.5	-	640.5	$1/f_{ADC}$
$t_{ADCVREG\_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 80 MHz Resolution = 12 bits	0.1875	-	8.1625	µs
		Resolution = 12 bits	ts + 12.5 cycles for successive approximation = 15 to 653			$1/f_{ADC}$
I_{DDA}(ADC)	ADC consumption from the V_{DDA} supply	fs = 5 Msps	-	730	830	µA
		fs = 1 Msps	-	160	220	
		fs = 10 ksps	-	16	50	
I_{DDV_S}(ADC)	ADC consumption from the V_{REF+} single ended mode	fs = 5 Msps	-	130	160	µA
		fs = 1 Msps	-	30	40	
		fs = 10 ksps	-	0.6	2	
I_{DDV_D}(ADC)	ADC consumption from the V_{REF+} differential mode	fs = 5 Msps	-	260	310	µA
		fs = 1 Msps	-	60	70	
		fs = 10 ksps	-	1.3	3	

1. Guaranteed by design
2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 4: Pinouts and pin description* for further details.

Table 91. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 80 MHz	12.5	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 80 MHz	0	40	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2 and TIM5)	-	16	bit
		TIM2 and TIM5	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 80 MHz	0.0125	819.2	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 80 MHz	-	53.68	s

1. TIMx is used as a general term in which x stands for 1,2,3,4,5,6,7,8,15,16 or 17.

Table 92. IWDG min/max timeout period at 32 kHz (LSI)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

1. The exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 93. WWDG min/max timeout value at 80 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0512	3.2768	ms
2	1	0.1024	6.5536	
4	2	0.2048	13.1072	
8	3	0.4096	26.2144	