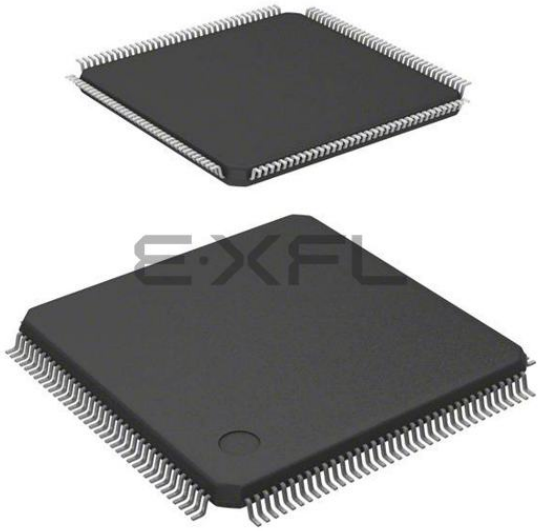


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	115
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	320K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l496zgt6

The STM32L496xx family offers six packages from 64-pin to 169-pin packages.

Table 2. STM32L496xx family device features and peripheral counts

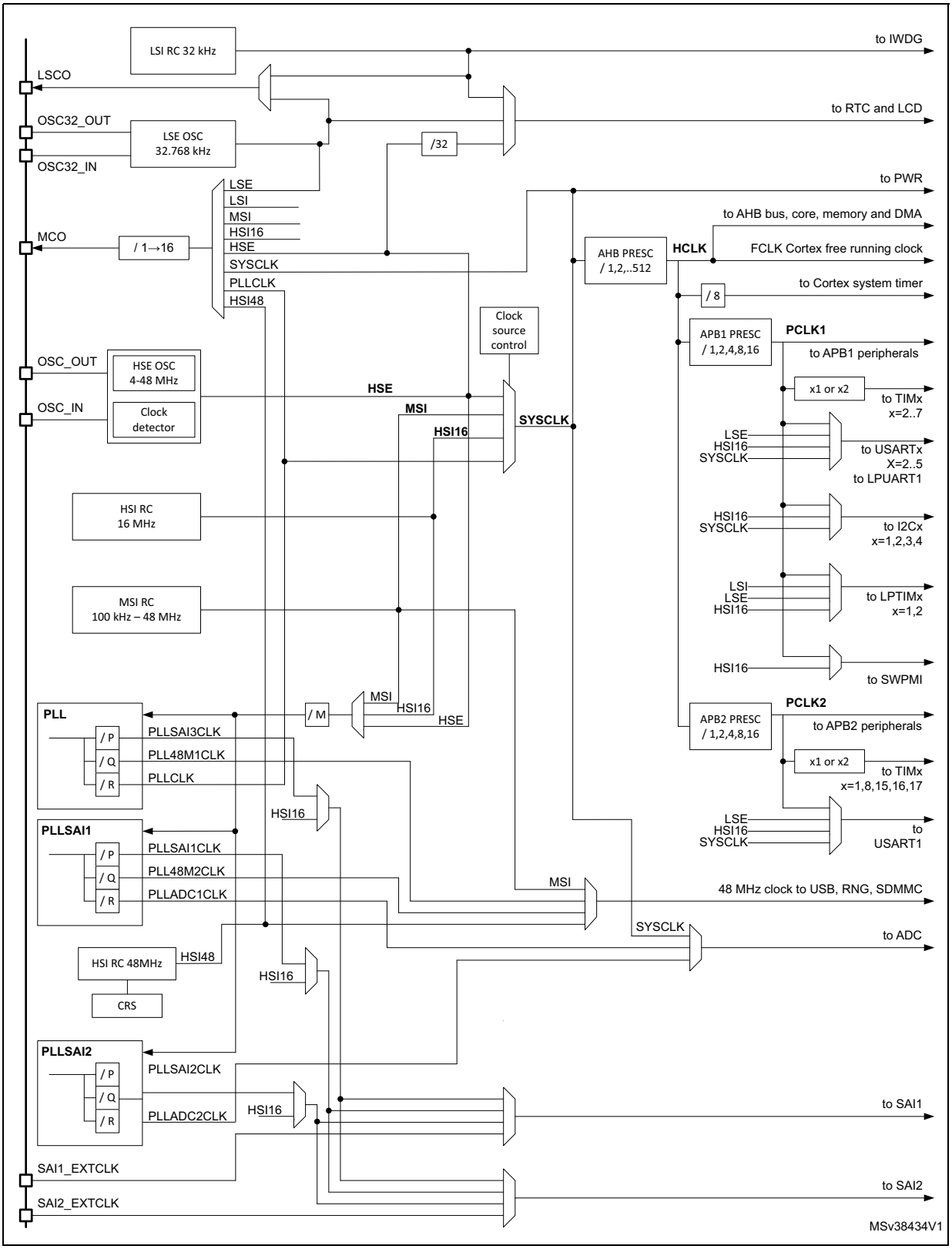
Peripheral		STM32L496Ax		STM32L496Zx		STM32L496Qx		STM32L496Vx		STM32L496Rx	
Flash memory		512KB	1MB	512KB	1MB	512KB	1MB	512KB	1MB	512KB	1MB
SRAM		320 KB									
External memory controller for static memories		Yes		Yes		Yes		Yes(1)		No	
Quad SPI		Yes									
Timers	Advanced control	2 (16-bit)									
	General purpose	5 (16-bit) 2 (32-bit)									
	Basic	2 (16-bit)									
	Low power	2 (16-bit)									
	SysTick timer	1									
	Watchdog timers (independen, window)	2									
Comm. interfaces	SPI	3									
	I^2C	4									
	USART UART LPUART	3 2 1									
	SAI	2									
	CAN	2									
	USB OTG FS	Yes									
	SDMMC	Yes									
	SWPMI	Yes									
Digital filters for sigma-delta modulators		Yes (4 filters)									
Number of channels		8									
RTC		Yes									
Tamper pins		3									
Camera interface		Yes								Yes(2)	
Chrom-ART Accelerator™		Yes									

Table 2. STM32L496xx family device features and peripheral counts (continued)

Peripheral	STM32L496Ax	STM32L496Zx	STM32L496Qx	STM32L496Vx	STM32L496Rx
LCD COM x SEG	Yes 8x40 or 4x44				
Random generator	Yes				
GPIOs(3) Wakeup pins Nb of I/Os down to 1.08 V	136 5 14	115 5 14	110 5 14	83 5 0	52 4 0
Capacitive sensing Number of channels	24	24	24	21	21
12-bit ADCs Number of channels	3 24	3 24	3 19	3 16	3 16
12-bit DAC channels	2				
Internal voltage reference buffer	Yes				
Analog comparator	2				
Operational amplifiers	2				
Max. CPU frequency	80 MHz				
Operating voltage (VDD)	1.71 to 3.6 V				
Operating voltage (VDD12)	1.05 to 1.32 V				
Operating temperature	Ambient operating temperature: -40 to 85 °C / -40 to 105 °C / -40 to 125 °C Junction temperature: -40 to 105 °C / -40 to 125 °C / -40 to 130 °C				
Packages	UFBGA169	LQFP144	UFBGA132	LQFP100 WLCSP100	LQFP64

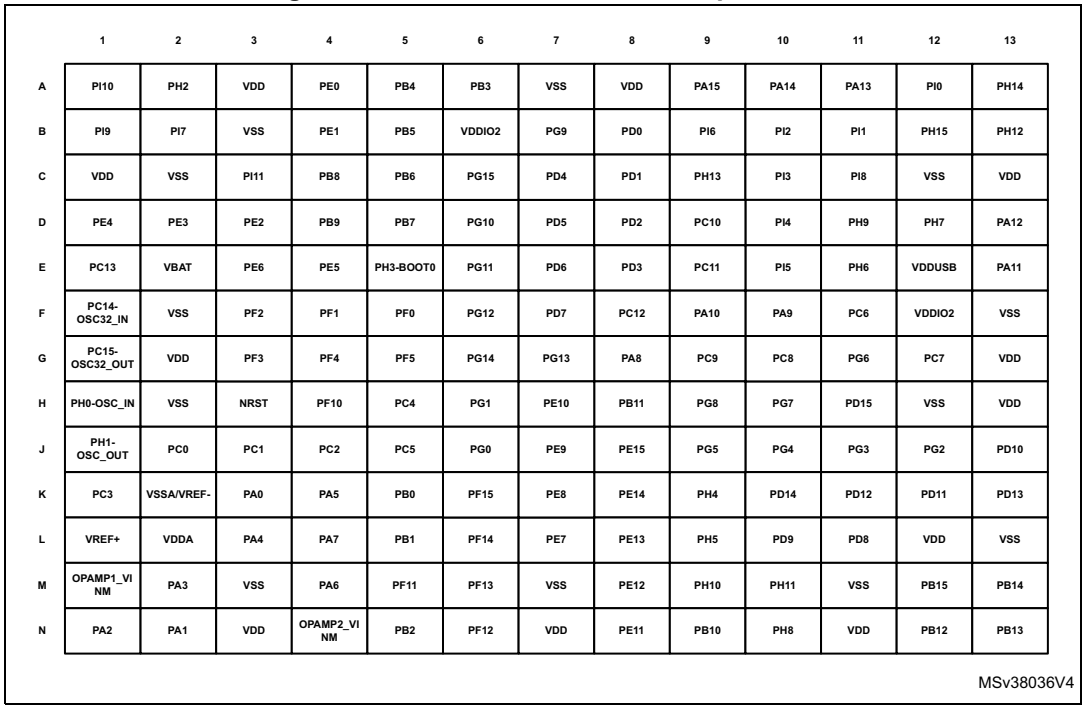
1. For the LQFP100 and WLCSP100 packages, only FMC Bank1 is available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select.
2. Only up to 13 data bits.
3. In case external SMPS package type is used, 2 GPIO's are replaced by VDD12 pins to connect the SMPS power supplies hence reducing the number of available GPIO's by 2.

Figure 4. Clock tree



4 Pinouts and pin description

Figure 6. STM32L496Ax UFBGA169 pinout(1)

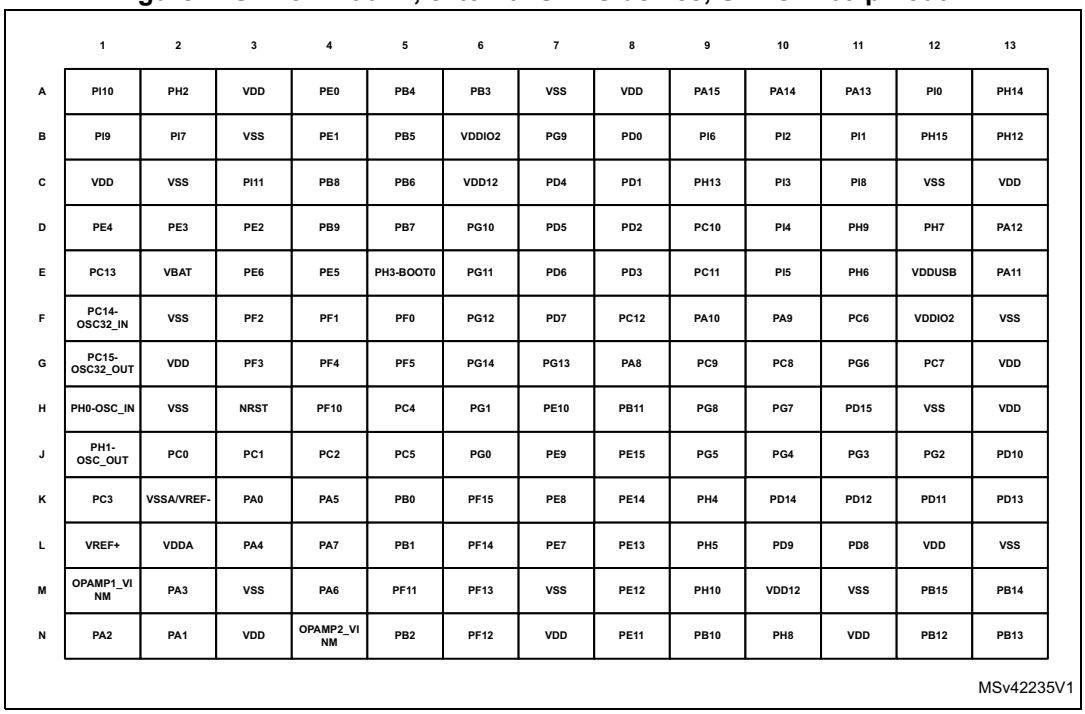


	1	2	3	4	5	6	7	8	9	10	11	12	13
A	PI10	PH2	VDD	PE0	PB4	PB3	VSS	VDD	PA15	PA14	PA13	PI0	PH14
B	PI9	PI7	VSS	PE1	PB5	VDDIO2	PG9	PD0	PI6	PI2	PI1	PH15	PH12
C	VDD	VSS	PI11	PB8	PB6	PG15	PD4	PD1	PH13	PI3	PI8	VSS	VDD
D	PE4	PE3	PE2	PB9	PB7	PG10	PD5	PD2	PC10	PI4	PH9	PH7	PA12
E	PC13	VBAT	PE6	PE5	PH3-BOOT0	PG11	PD6	PD3	PC11	PI5	PH6	VDDUSB	PA11
F	PC14-OSC32_IN	VSS	PF2	PF1	PF0	PG12	PD7	PC12	PA10	PA9	PC6	VDDIO2	VSS
G	PC15-OSC32_OUT	VDD	PF3	PF4	PF5	PG14	PG13	PA8	PC9	PC8	PG6	PC7	VDD
H	PH0-OSC_IN	VSS	NRST	PF10	PC4	PG1	PE10	PB11	PG8	PG7	PD15	VSS	VDD
J	PH1-OSC_OUT	PC0	PC1	PC2	PC5	PG0	PE9	PE15	PG5	PG4	PG3	PG2	PD10
K	PC3	VSSA/VREF-	PA0	PA5	PB0	PF15	PE8	PE14	PH4	PD14	PD12	PD11	PD13
L	VREF+	VDDA	PA4	PA7	PB1	PF14	PE7	PE13	PH5	PD9	PD8	VDD	VSS
M	OPAMP1_VINM	PA3	VSS	PA6	PF11	PF13	VSS	PE12	PH10	PH11	VSS	PB15	PB14
N	PA2	PA1	VDD	OPAMP2_VINM	PB2	PF12	VDD	PE11	PB10	PH8	VDD	PB12	PB13

MSv38036V4

1. The above figure shows the package top view.

Figure 7. STM32L496Ax, external SMPS device, UFBGA169 pinout(1)

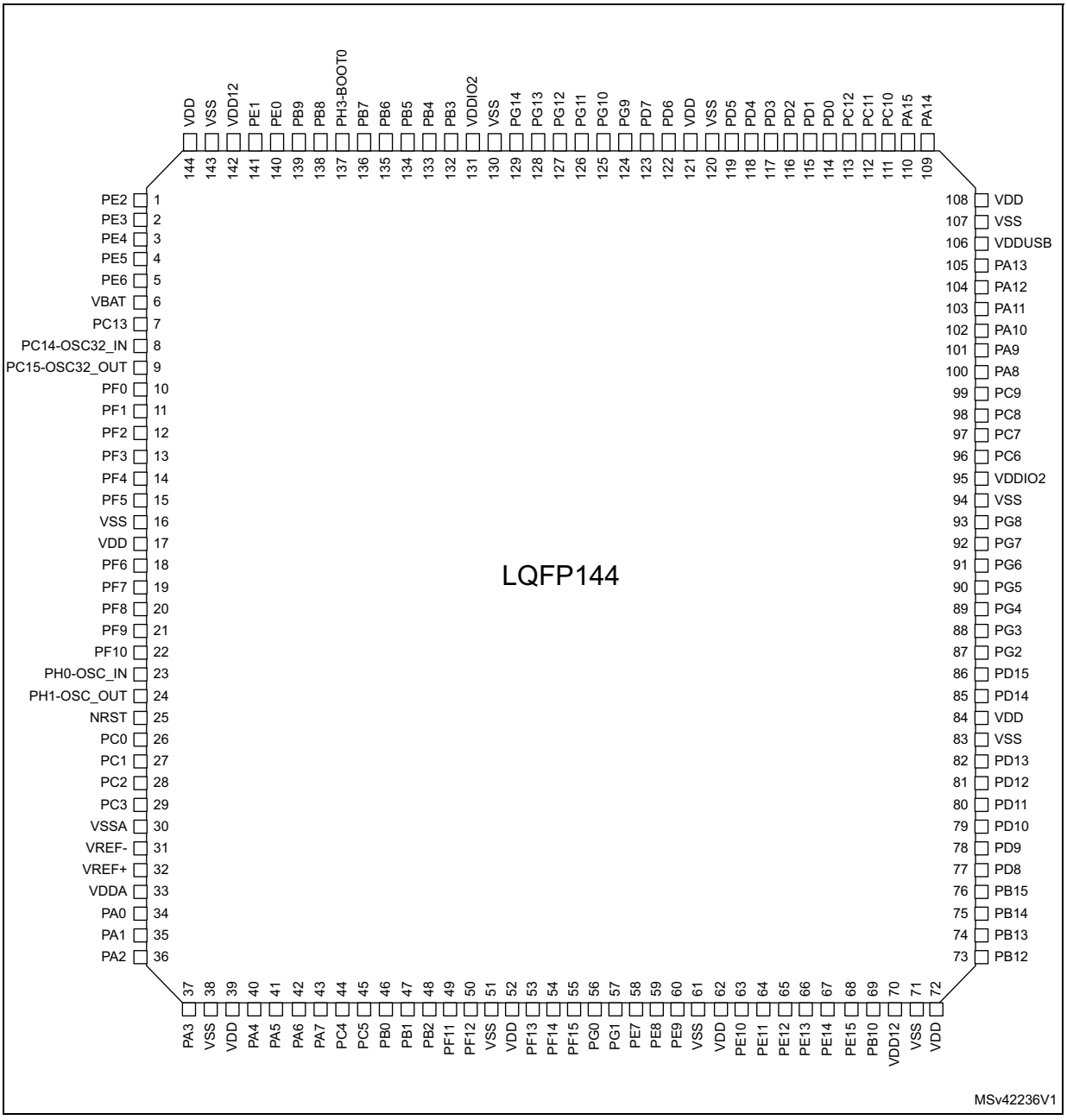


	1	2	3	4	5	6	7	8	9	10	11	12	13
A	PI10	PH2	VDD	PE0	PB4	PB3	VSS	VDD	PA15	PA14	PA13	PI0	PH14
B	PI9	PI7	VSS	PE1	PB5	VDDIO2	PG9	PD0	PI6	PI2	PI1	PH15	PH12
C	VDD	VSS	PI11	PB8	PB6	VDD12	PD4	PD1	PH13	PI3	PI8	VSS	VDD
D	PE4	PE3	PE2	PB9	PB7	PG10	PD5	PD2	PC10	PI4	PH9	PH7	PA12
E	PC13	VBAT	PE6	PE5	PH3-BOOT0	PG11	PD6	PD3	PC11	PI5	PH6	VDDUSB	PA11
F	PC14-OSC32_IN	VSS	PF2	PF1	PF0	PG12	PD7	PC12	PA10	PA9	PC6	VDDIO2	VSS
G	PC15-OSC32_OUT	VDD	PF3	PF4	PF5	PG14	PG13	PA8	PC9	PC8	PG6	PC7	VDD
H	PH0-OSC_IN	VSS	NRST	PF10	PC4	PG1	PE10	PB11	PG8	PG7	PD15	VSS	VDD
J	PH1-OSC_OUT	PC0	PC1	PC2	PC5	PG0	PE9	PE15	PG5	PG4	PG3	PG2	PD10
K	PC3	VSSA/VREF-	PA0	PA5	PB0	PF15	PE8	PE14	PH4	PD14	PD12	PD11	PD13
L	VREF+	VDDA	PA4	PA7	PB1	PF14	PE7	PE13	PH5	PD9	PD8	VDD	VSS
M	OPAMP1_VINM	PA3	VSS	PA6	PF11	PF13	VSS	PE12	PH10	VDD12	VSS	PB15	PB14
N	PA2	PA1	VDD	OPAMP2_VINM	PB2	PF12	VDD	PE11	PB10	PH8	VDD	PB12	PB13

MSv42235V1

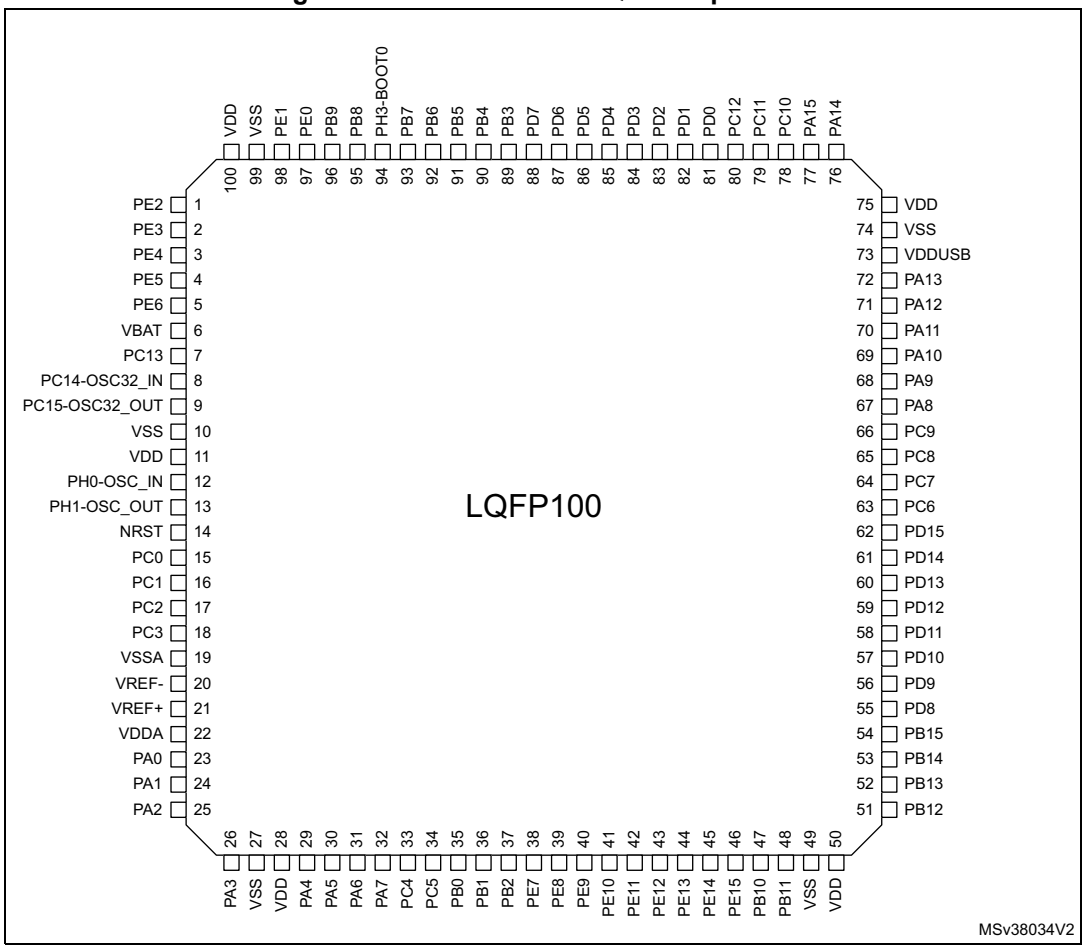
1. The above figure shows the package top view.

Figure 9. STM32L496Zx, external SMPS device, LQFP144 pinout(1)



1. The above figure shows the package top view.

Figure 11. STM32L496Vx LQFP100 pinout(1)



1. The above figure shows the package top view.

Table 15. STM32L496xx pin definitions (continued)

Pin Number									Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	WLCSP100	WLCSP100_SMPS	LQFP100	UFBGA132	LQFP144	LQFP144_SMPS	UFBGA169	UFBGA169_SMPS					Alternate functions	Additional functions
22	K9	K9	31	L4	42	42	M4	M4	PA6	I/O	FT_la	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, DCMI_PIXCLK, SPI1_MISO, USART3_CTS, LPUART1_CTS, QUADSPI_BK1_IO3, LCD_SEG3, TIM1_BKIN_COMP2, TIM8_BKIN_COMP2, TIM16_CH1, EVENTOUT	OPAMP2_VINP, ADC12_IN11
-	-	-	-	M4	-	-	N4	N4	OPAMP2_VINM	I	TT	-	-	-
23	J7	G6	32	J5	43	43	L4	L4	PA7	I/O	FT_fla	(1)	TIM1_CH1N, TIM3_CH2, TIM8_CH1N, I2C3_SCL, SPI1_MOSI, QUADSPI_BK1_IO2, LCD_SEG4, TIM17_CH1, EVENTOUT	OPAMP2_VINM, ADC12_IN12
24	H6	K8	33	K5	44	44	H5	H5	PC4	I/O	FT_la	-	USART3_TX, QUADSPI_BK2_IO3, LCD_SEG22, EVENTOUT	COMP1_INM, ADC12_IN13
25	K8	-	34	L5	45	45	J5	J5	PC5	I/O	FT_la	-	USART3_RX, LCD_SEG23, EVENTOUT	COMP1_INP, ADC12_IN14, WKUP5
26	J6	H6	35	M5	46	46	K5	K5	PB0	I/O	TT_la	-	TIM1_CH2N, TIM3_CH3, TIM8_CH2N, SPI1_NSS, USART3_CK, QUADSPI_BK1_IO1, LCD_SEG5, COMP1_OUT, SAI1_EXTCLK, EVENTOUT	OPAMP2_VOUT, ADC12_IN15
27	K7	K7	36	M6	47	47	L5	L5	PB1	I/O	FT_la	-	TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN0, USART3_RTS_DE, LPUART1_RTS_DE, QUADSPI_BK1_IO0, LCD_SEG6, LPTIM2_IN1, EVENTOUT	COMP1_INM, ADC12_IN16
28	F5	J6	37	L6	48	48	N5	N5	PB2	I/O	FT_la	-	RTC_OUT, LPTIM1_OUT, I2C3_SMBA, DFSDM1_CKIN0, LCD_VLCD, EVENTOUT	COMP1_INP
-	-	-	-	K6	49	49	M5	M5	PF11	I/O	FT	-	DCMI_D12, EVENTOUT	-

Table 18. STM32L496xx memory map and peripheral register boundary addresses(1) (continued)

Bus	Boundary address	Size (bytes)	Peripheral
APB1	0x4000 9800 - 0x4000 FFFF	26 KB	Reserved
	0x4000 9400 - 0x4000 97FF	1 KB	LPTIM2
	0x4000 8C00 - 0x4000 93FF	2 KB	Reserved
	0x4000 8800 - 0x4000 8BFF	1 KB	SWPMI1
	0x4000 8400 - 0x4000 87FF	1 KB	I2C4
	0x4000 8000 - 0x4000 83FF	1 KB	LPUART1
	0x4000 7C00 - 0x4000 7FFF	1 KB	LPTIM1
	0x4000 7800 - 0x4000 7BFF	1 KB	OPAMP
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6800 - 0x4000 6FFF	1 KB	Reserved
	0x4000 6800 - 0x4000 6BFF	1 KB	CAN2
	0x4000 6400 - 0x4000 67FF	1 KB	CAN1
	0x4000 6000 - 0x4000 63FF	1 KB	CRS
	0x4000 5C00- 0x4000 5FFF	1 KB	I2C3
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 5000 - 0x4000 53FF	1 KB	UART5
	0x4000 4C00 - 0x4000 4FFF	1 KB	UART4

Figure 20. V_{REFINT} versus temperature

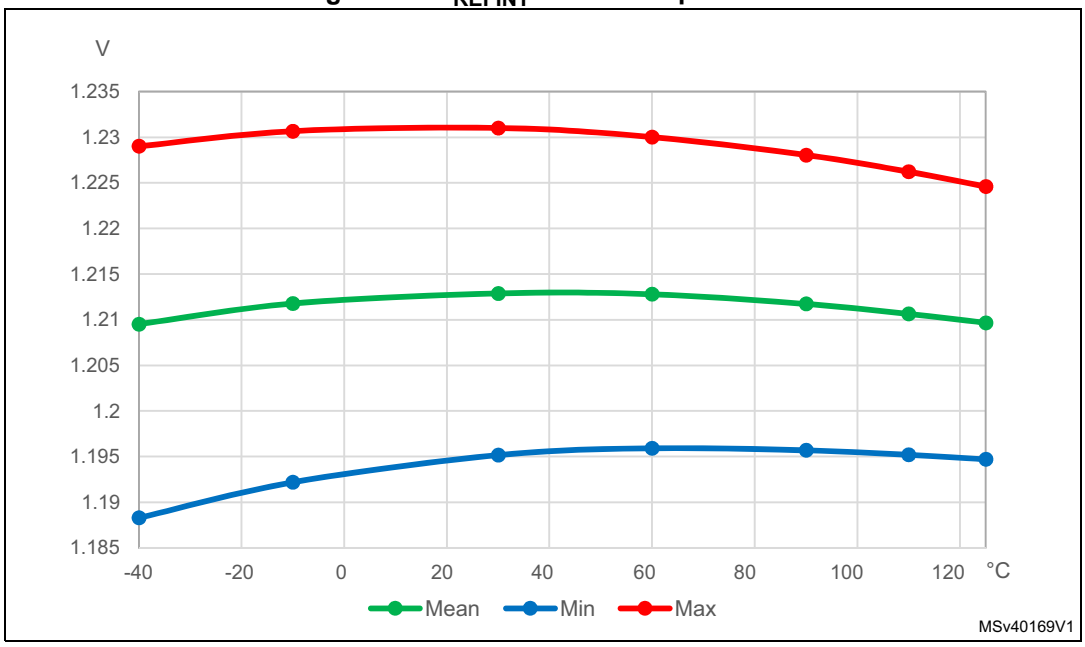


Table 45. Current consumption in Stop 1 mode (continued)

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (wakeup from Stop1)	Supply current during wakeup from Stop 1	Wakeup clock MSI = 48 MHz, voltage Range 1. See (4).		3 V	0.99	-	-	-	-	-	-	-	-	-	mA
		Wakeup clock MSI = 4 MHz, voltage Range 2. See (4).		3 V	1.1	-	-	-	-	-	-	-	-	-	
		Wakeup clock HSI16 = 16 MHz, voltage Range 1. See (4).		3 V	0.95	-	-	-	-	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. LCD enabled with external voltage source. Consumption from VLCD excluded. Refer to LCD controller characteristics for I_{VLCD}.
3. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
4. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 51: Low-power mode wakeup timings*.

Table 46. Current consumption in Stop 0 mode

Symbol	Parameter	Conditions	TYP					MAX(1)					Unit
		V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD_ALL} (Stop 0)	Supply current in Stop 0 mode, RTC disabled	1.8 V	127	153	244	404	734	148	218	471	905	1795	µA
		2.4 V	129	155	247	407	737	151	221	474	910	1803	
		3 V	131	156	249	409	741	154	224	478	915	1813	
		3.6 V	133	158	251	412	744	157	228	482	921	1822(2)	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.

6.3.8 Internal clock source characteristics

The parameters given in *Table 58* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*. The provided curves are characterization results, not tested in production.

High-speed internal (HSI16) RC oscillator

Table 58. HSI16 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	HSI16 Frequency	V_{DD}=3.0 V, T_A=30 °C	15.88	-	16.08	MHz
TRIM	HSI16 user trimming step	Trimming code is not a multiple of 64	0.2	0.3	0.4	%
		Trimming code is a multiple of 64	-4	-6	-8	
DuCy(HSI16)(2)	Duty Cycle	-	45	-	55	%
Δ_{Temp}(HSI16)	HSI16 oscillator frequency drift over temperature	T_A= 0 to 85 °C	-1	-	1	%
		T_A= -40 to 125 °C	-2	-	1.5	%
Δ_{VDD}(HSI16)	HSI16 oscillator frequency drift over V_{DD}	V_{DD}=1.62 V to 3.6 V	-0.1	-	0.05	%
t_{su}(HSI16)(2)	HSI16 oscillator start-up time	-	-	0.8	1.2	µs
t_{stab}(HSI16)(2)	HSI16 oscillator stabilization time	-	-	3	5	µs
I_{DD}(HSI16)(2)	HSI16 oscillator power consumption	-	-	155	190	µA

1. Guaranteed by characterization results.
2. Guaranteed by design.

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

Table 71. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx}-0.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	TTL port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	
V_{OH}(3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	1.3	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}-1.3	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 4 mA $V_{DDIOx} \geq 1.62$ V	-	0.45	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}-0.45	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 2 mA 1.62 V ≥ V_{DDIOx} ≥ 1.08 V	-	$0.35_x V_{DDIOx}$	
V_{OH}(3)	Output high level voltage for an I/O pin		$0.65_x V_{DDIOx}$	-	
V_{OLFM+}(3)	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with "f" option)	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	
		$\|I_{IO}\|$ = 10 mA $V_{DDIOx} \geq 1.62$ V	-	0.4	
		$\|I_{IO}\|$ = 2 mA 1.62 V ≥ V_{DDIOx} ≥ 1.08 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 19: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 29* and *Table 72*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

Table 72. I/O AC characteristics(1)(2) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
10	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	25	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	5	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	100(3)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37.5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5.8	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	11	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	28	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	2.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	12	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	120(3)	MHz
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	50	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	10	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	180(3)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	75	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	10	
	Tr/Tf	Output rise and fall time	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	3.3	ns
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	6	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	16	
Fm+	Fmax	Maximum frequency	C=50 pF, 1.6 V≤V_{DDIOx}≤3.6 V	-	1	MHz
	Tf	Output fall time(4)		-	5	ns

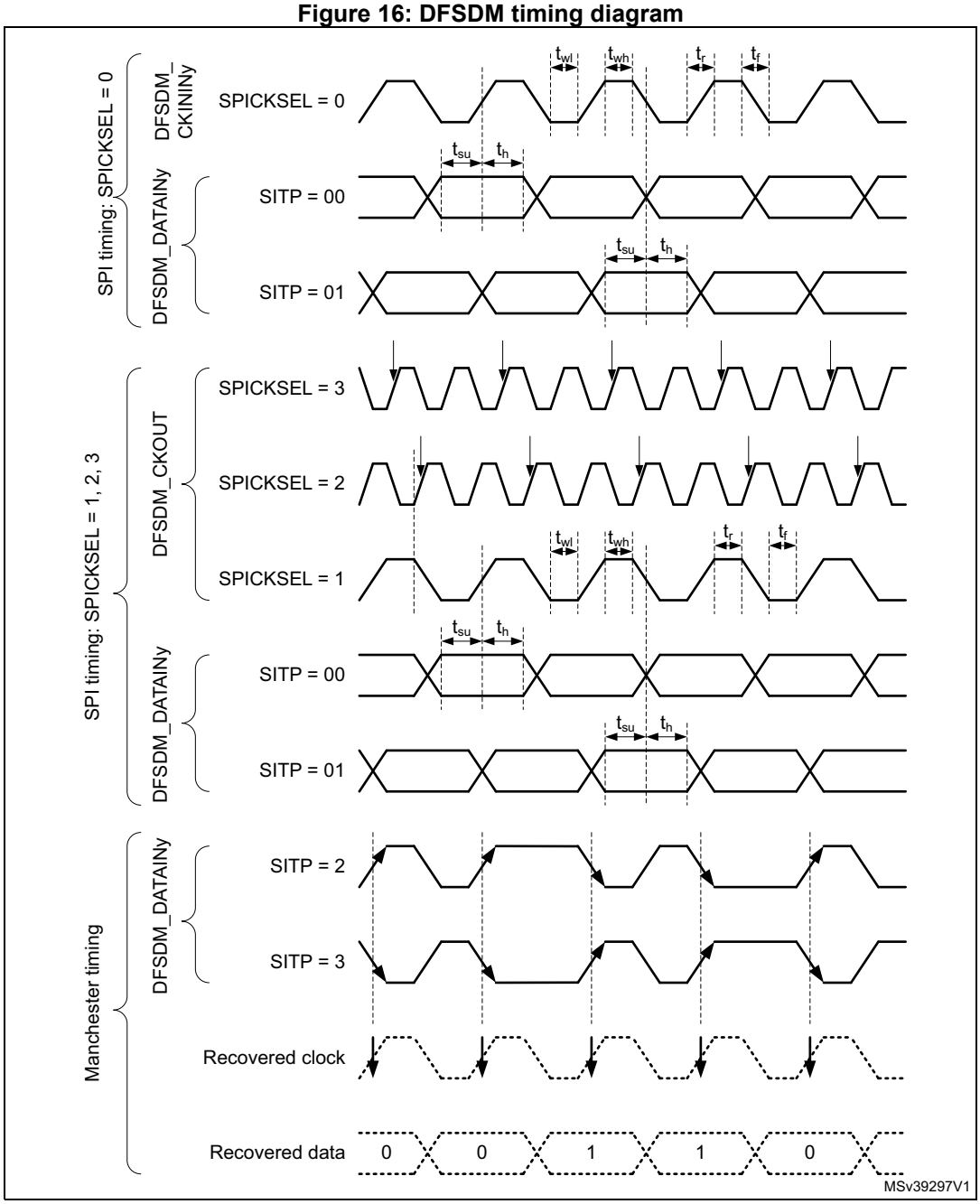
1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the RM0351 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. This value represents the I/O capability but the maximum system frequency is limited to 80 MHz.
4. The fall time is defined between 70% and 30% of the output waveform accordingly to I^2C specification.

Table 75. ADC characteristics(1) (2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{LATRINJ}$	Trigger conversion latency Injected channels aborting a regular conversion	CKMODE = 00	2.5	3	3.5	$1/f_{ADC}$
		CKMODE = 01	-	-	3.0	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t_s	Sampling time	f_{ADC} = 80 MHz	0.03125	-	8.00625	µs
		-	2.5	-	640.5	$1/f_{ADC}$
$t_{ADCVREG\_STUP}$	ADC voltage regulator start-up time	-	-	-	20	µs
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 80 MHz Resolution = 12 bits	0.1875	-	8.1625	µs
		Resolution = 12 bits	ts + 12.5 cycles for successive approximation = 15 to 653			$1/f_{ADC}$
I_{DDA}(ADC)	ADC consumption from the V_{DDA} supply	fs = 5 Msps	-	730	830	µA
		fs = 1 Msps	-	160	220	
		fs = 10 ksps	-	16	50	
I_{DDV_S}(ADC)	ADC consumption from the V_{REF+} single ended mode	fs = 5 Msps	-	130	160	µA
		fs = 1 Msps	-	30	40	
		fs = 10 ksps	-	0.6	2	
I_{DDV_D}(ADC)	ADC consumption from the V_{REF+} differential mode	fs = 5 Msps	-	260	310	µA
		fs = 1 Msps	-	60	70	
		fs = 10 ksps	-	1.3	3	

1. Guaranteed by design
2. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4V). It is disable when V_{DDA} ≥ 2.4 V.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 4: Pinouts and pin description* for further details.

Figure 16: DFSDM timing diagram



6.3.26 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 99. SD / MMC dynamic characteristics, V_{DD}=2.7 V to 3.6 V(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	f_{PP} = 25 MHz	-	3	5	ns
t_{OHD}	Output hold default time SD	f_{PP} = 25 MHz	0	-	-	ns

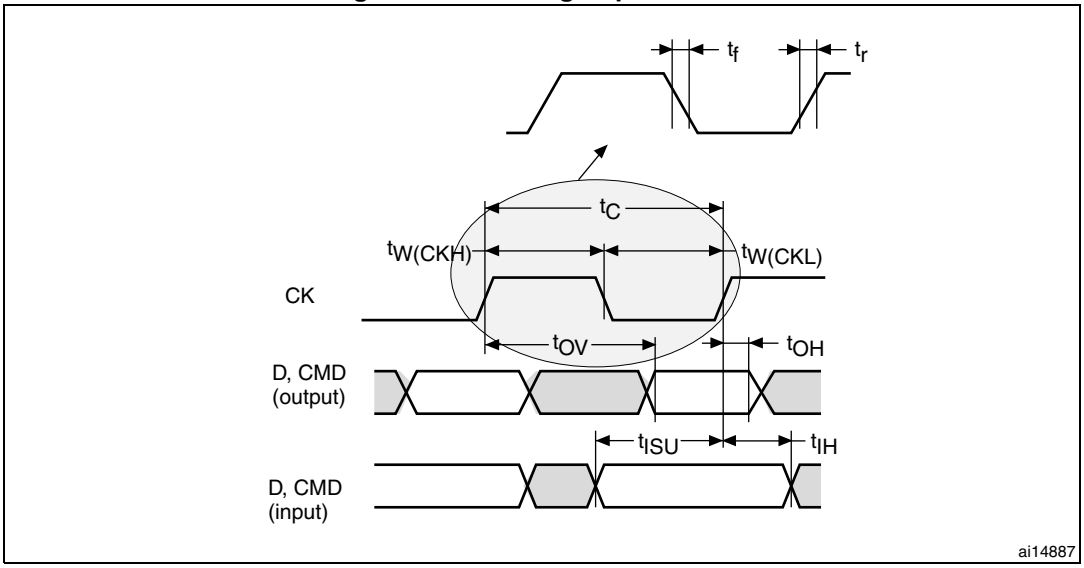
1. Guaranteed by characterization results.

Table 100. eMMC dynamic characteristics, V_{DD} = 1.71 V to 1.9 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/f_{PCLK2} frequency ratio	-	-	-	4/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 50 MHz	8	10	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 50 MHz	8	10	-	ns
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	f_{PP} = 50 MHz	2.5	-	-	ns
t_{IH}	Input hold time HS	f_{PP} = 50 MHz	2.5	-	-	ns
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	f_{PP} = 50 MHz	-	13.5	16.5	ns
t_{OH}	Output hold time HS	f_{PP} = 50 MHz	9	-	-	ns

1. Guaranteed by characterization results.
2. C_{LOAD} = 20pF.

Figure 41. SDIO high-speed mode



1. CL = 30 pF.
2. Guaranteed by characterization results.

Table 109. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{HCLK}$- 1	$9T_{HCLK}$+ 1	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{HCLK}$- 0.5	$7T_{HCLK}$+ 0.5	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$6T_{HCLK}$+ 2	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{HCLK}$- 1	-	

1. CL = 30 pF.
2. Guaranteed by characterization results.

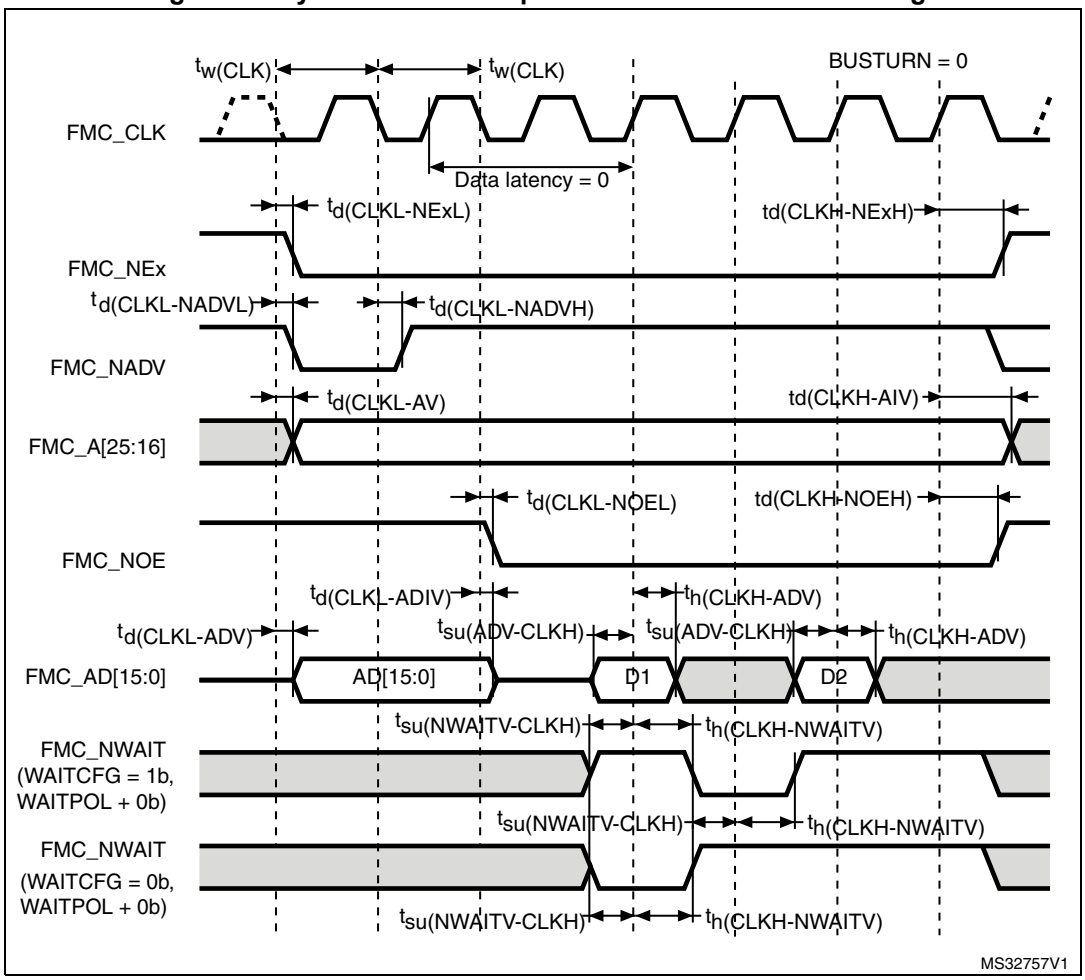
Synchronous waveforms and timings

Figure 47 through *Figure 50* represent synchronous waveforms and *Table 110* through *Table 113* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

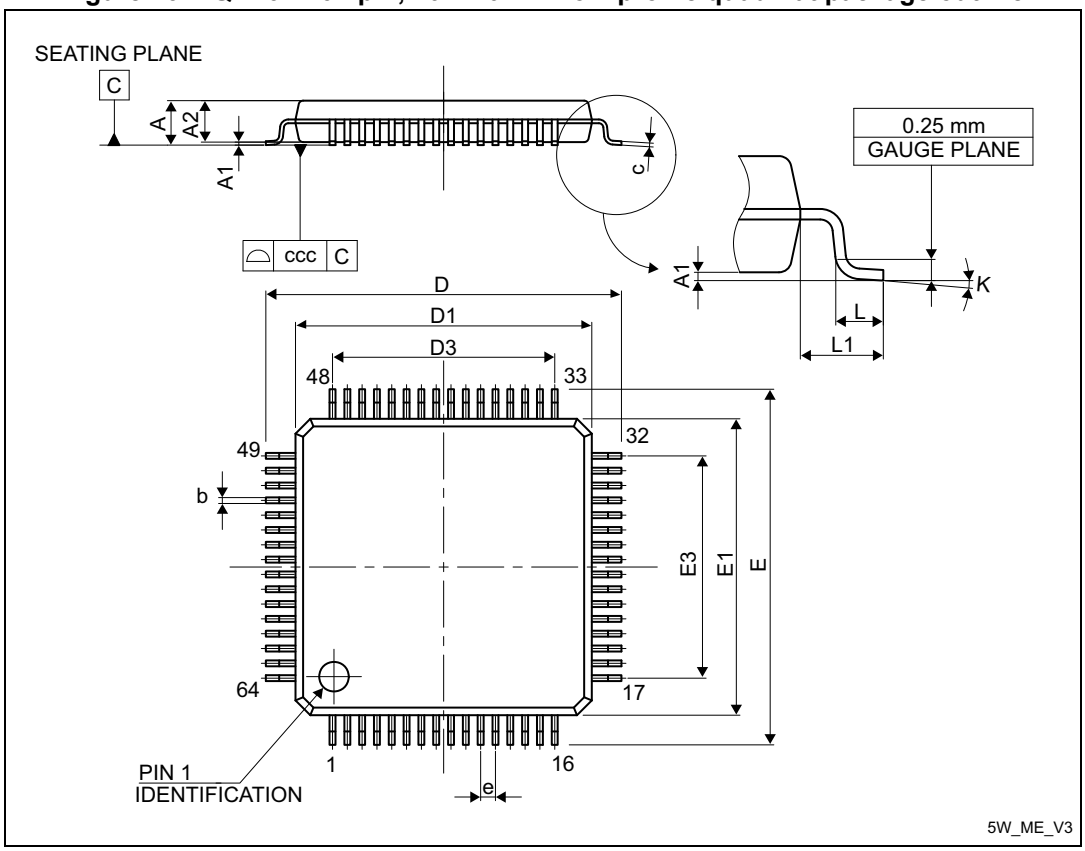
In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 47. Synchronous multiplexed NOR/PSRAM read timings



7.6 LQFP64 package information

Figure 76. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 128. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-