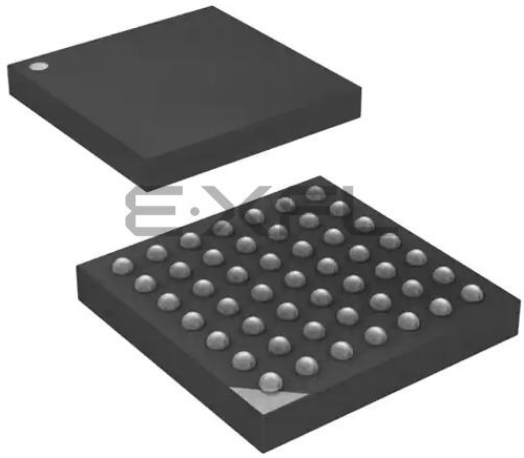


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	49-VFBGA
Supplier Device Package	49-VFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega16a4u-cnr

7. Memories

7.1 Features

- Flash program memory
  - One linear address space
  - In-system programmable
  - Self-programming and boot loader support
  - Application section for application code
  - Application table section for application code or data storage
  - Boot section for application code or boot loader code
  - Separate read/write protection lock bits for all sections
  - Built in fast CRC check of a selectable flash program memory section
- Data memory
  - One linear address space
  - Single-cycle access from CPU
  - SRAM
  - EEPROM
    - Byte and page accessible
    - Optional memory mapping for direct load and store
  - I/O memory
    - Configuration and status registers for all peripherals and modules
    - 16 bit-accessible general purpose registers for global variables or flags
  - Bus arbitration
    - Deterministic priority handling between CPU, DMA controller, and other bus masters
  - Separate buses for SRAM, EEPROM and I/O memory
    - Simultaneous bus access for CPU and DMA controller
- Production signature row memory for factory programmed data
  - ID for each microcontroller device type
  - Serial number for each device
  - Calibration bytes for factory calibrated peripherals
- User signature row
  - One flash page in size
  - Can be read and written from software
  - Content is kept after chip erase

7.2 Overview

The Atmel AVR architecture has two main memory spaces, the program memory and the data memory. Executable code can reside only in the program memory, while data can be stored in the program memory and the data memory. The data memory includes the internal SRAM, and EEPROM for nonvolatile data storage. All memory spaces are linear and require no memory bank switching. Nonvolatile memory (NVM) spaces can be locked for further write and read/write operations. This prevents unrestricted access to the application software.

A separate memory section contains the fuse bytes. These are used for configuring important system functions, and can only be written by an external programmer.

The available memory size configurations are shown in “Ordering Information” on page 2. In addition, each device has a Flash memory signature row for calibration data, device identification, serial number etc.

Table 32-3. Port C - alternate functions.

PORT C	PIN #	INTERRUPT	TCC0 (1)(2)	AWEXC	TCC1	USART C0(3)	USART C1	SPIC(4)	TWIC	TWIC w/ext driver	CLOCKOUT (5)	EVENTOUT (6)
GND	8											
VCC	9											
PC0	10	SYNC	OC0A	$\overline{\text{OC0ALS}}$					SDA	SDAIN		
PC1	11	SYNC	OC0B	OC0AHS		XCK0			SCL	SCLIN		
PC2	12	SYNC/ ASYNC	OC0C	$\overline{\text{OC0BLS}}$		RXD0				SDAOUT		
PC3	13	SYNC	OC0D	OC0BHS		TXD0				SCLOUT		
PC4	14	SYNC		$\overline{\text{OC0CLS}}$	OC1A			$\overline{\text{SS}}$				
PC5	15	SYNC		OC0CHS	OC1B		XCK1	MOSI				
PC6	16	SYNC		$\overline{\text{OC0DLS}}$			RXD1	MISO			clk_{RTC}	
PC7	17	SYNC		OC0DHS			TXD1	SCK			clk_{PER}	EVOUT

Notes:
1. Pin mapping of all TC0 can optionally be moved to high nibble of port
2. If TC0 is configured as TC2 all eight pins can be used for PWM output.
3. Pin mapping of all USART0 can optionally be moved to high nibble of port.
4. Pins MOSI and SCK for all SPI can optionally be swapped.
5. CLKOUT can optionally be moved between port C, D and E and between pin 4 and 7.
6. EVOUT can optionally be moved between port C, D and E and between pin 4 and 7.

Table 32-4. Port D - alternate functions.

PORT D	PIN #	INTERRUPT	TCD0	TCD1	USB	USARTD0	USARTD1	SPID	CLOCKOUT	EVENTOUT
GND	18									
VCC	19									
PD0	20	SYNC	OC0A							
PD1	21	SYNC	OC0B			XCK0				
PD2	22	SYNC/ASYNC	OC0C			RXD0				
PD3	23	SYNC	OC0D			TXD0				
PD4	24	SYNC		OC1A				$\overline{\text{SS}}$		
PD5	25	SYNC		OC1B			XCK1	MOSI		
PD6	26	SYNC			D-		RXD1	MISO		
PD7	27	SYNC			D+		TXD1	SCK	clk_{PER}	EVOUT

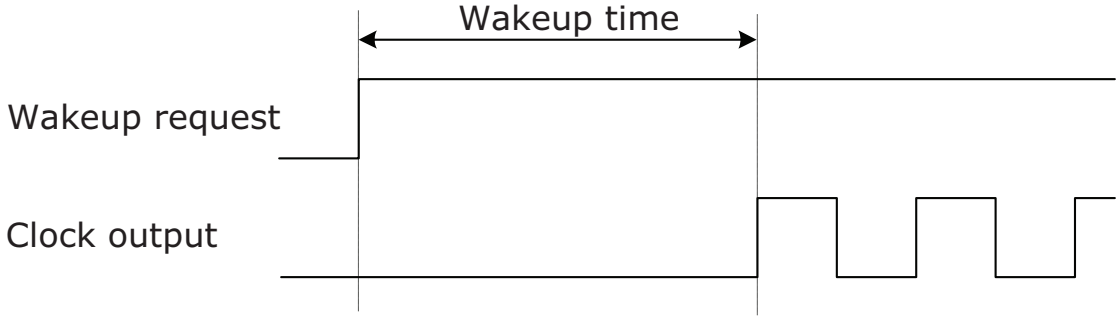
36.2.4 Wake-up time from sleep modes

Table 36-38. Device wake-up time from sleep modes with various system clock sources.

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
t_{wakeup}	Wake-up time from idle, standby, and extended standby mode	External 2MHz clock		2.0		µs
		32.768kHz internal oscillator		120		
		2MHz internal oscillator		2.0		
		32MHz internal oscillator		0.2		
	Wake-up time from power-save and power-down mode	External 2MHz clock		4.5		µs
		32.768kHz internal oscillator		320		
		2MHz internal oscillator		9.0		
		32MHz internal oscillator		5.0		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 36-9. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 36-9. Wake-up time definition.



36.2.14 Clock and Oscillator Characteristics

36.2.14.1 Calibrated 32.768kHz Internal Oscillator characteristics

Table 36-54. 32.768kHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	%

36.2.14.2 Calibrated 2MHz RC Internal Oscillator characteristics

Table 36-55. 2MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8		2.2	MHz
	Factory calibrated frequency			2.0		MHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	%
	DFLL calibration stepsize			0.21		%

36.2.14.3 Calibrated and tunable 32MHz internal oscillator characteristics

Table 36-56. 32MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30		55	MHz
	Factory calibrated frequency			32		MHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	%
	DFLL calibration step size			0.22		%

36.2.14.4 32kHz Internal ULP Oscillator characteristics

Table 36-57. 32kHz internal ULP oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Output frequency			32		kHz
	Accuracy		-30		30	%

Table 36-69. Current consumption for modules and peripherals.

Symbol	Parameter	Condition [1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				1.0		µA
	32.768kHz int. oscillator				29		µA
	2MHz int. oscillator				85		µA
		DFLL enabled with 32.768kHz int. osc. as reference			120		
	32MHz int. oscillator				300		µA
		DFLL enabled with 32.768kHz int. osc. as reference			465		
	PLL	20x multiplication factor, 32MHz int. osc. DIV4 as reference			320		µA
	Watchdog timer				1.0		µA
	BOD	Continuous mode			138		µA
		Sampled mode, includes ULP oscillator			1.0		
	Internal 1.0V reference				103		µA
	Temperature sensor				100		µA
	ADC	250ksps V_{REF} = Ext ref			3.0		mA
			CURRLIMIT = LOW		2.6		
			CURRLIMIT = MEDIUM		2.1		
			CURRLIMIT = HIGH		1.6		
	DAC	250ksps V_{REF} = Ext ref No load	Normal mode		1.9		mA
			Low power mode		1.1		
	AC	High speed mode			330		µA
		Low pPower mode			130		
	DMA	615KBps between I/O registers and SRAM			108		µA
	Timer/counter				16		µA
	USART	Rx and Tx enabled, 9600 BAUD			2.5		µA
	Flash memory and EEPROM programming				8.0		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

36.3.6 ADC characteristics

Table 36-72. Power supply, reference and input range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	V
V_{REF}	Reference voltage		1.0		AV_{CC}- 0.6	V
R_{in}	Input resistance	Switched		4.0		kΩ
C_{sample}	Input capacitance	Switched		4.4		pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7.0		pF
V_{IN}	Input range		-0.1		AV_{CC}+0.1	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	V
	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF}-ΔV	V
ΔV	Fixed offset voltage			190		lsb

Table 36-73. Clock and timing.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC clock frequency	Maximum is 1/4 of peripheral clock frequency	100		2000	kHz
		Measuring internal signals	100		125	
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off	100		2000	ksps
		CURRLIMIT = LOW	100		1500	
		CURRLIMIT = MEDIUM	100		1000	
		CURRLIMIT = HIGH	100		500	
	Sampling time	1/2 Clk_{ADC} cycle	0.25		5	µs
	Conversion time (latency)	(RES+2)/2+(GAIN !=0) RES (Resolution) = 8 or 12	5		8	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	Clk_{ADC} cycles
	ADC settling time	After changing reference or input mode		7	7	Clk_{ADC} cycles
		After ADC flush		1	1	

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	ESR	SF = Safety factor			$\min(R_Q)/SF$	kΩ
C_{XTAL1}	Parasitic capacitance XTAL1 pin			5.60		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin			7.62		pF
C_{LOAD}	Parasitic capacitance load			3.23		pF

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization

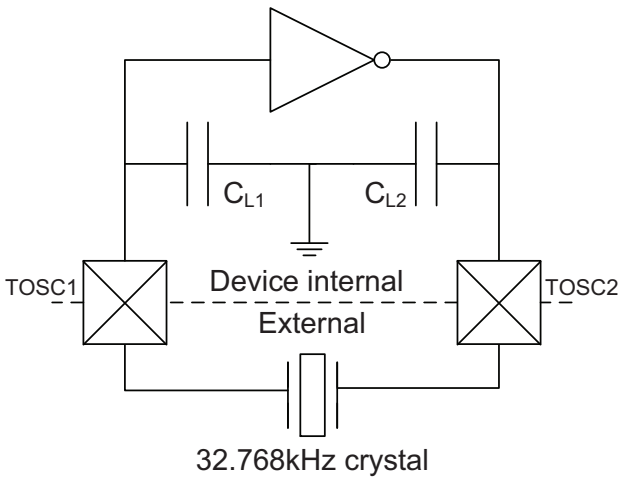
36.3.14.8 External 32.768kHz crystal oscillator and TOSC characteristics

Table 36-94. External 32.768kHz crystal oscillator and TOSC characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
C_{TOSC1}	Parasitic capacitance TOSC1 pin			5.4		pF
		Alternate TOSC location		4.0		
C_{TOSC2}	Parasitic capacitance TOSC2 pin			7.1		pF
		Alternate TOSC location		4.0		
	Recommended safety factor	capacitance load matched to crystal specification	3			

Note: 1. See Figure 36-18 for definition.

Figure 36-18. TOSC input capacitance.



The parasitic capacitance between the TOSC pins is C_{L1} + C_{L2} in series as seen from the crystal when oscillating without external capacitors.

36.3.16 Two-Wire Interface Characteristics

Table 36-96 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 36-21.

Figure 36-21.Two-wire interface bus timing.

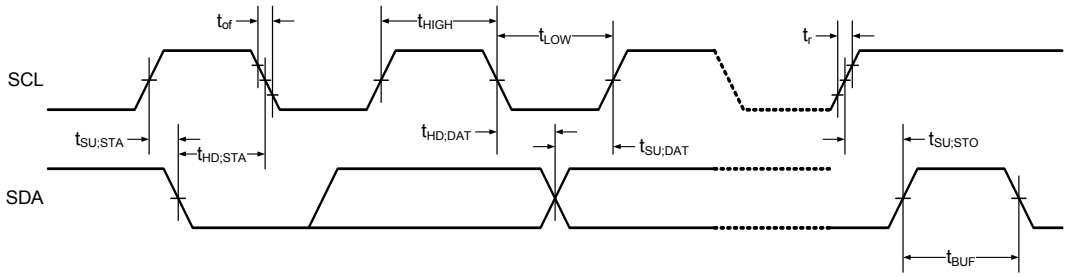


Table 36-96. Two-wire interface characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		$0.7*V_{CC}$		$V_{CC}+0.5$	V
V_{IL}	Input low voltage		-0.5		$0.3*V_{CC}$	V
V_{hys}	Hysteresis of Schmitt trigger inputs		$0.05*V_{CC}$ (1)		0	V
V_{OL}	Output low voltage	3mA, sink current	0		0.4	V
t_r	Rise time for both SDA and SCL		$20+0.1C_b$ (1)(2)		0	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF$ (2)	$20+0.1C_b$ (1)(2)		300	ns
t_{SP}	Spikes suppressed by input filter		0		50	ns
I_I	Input current for each I/O pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	µA
C_I	Capacitance for each I/O pin		0		10	pF
f_{SCL}	SCL clock frequency	f_{PER} (3)>max($10f_{SCL}$, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq 100kHz$	$\frac{V_{CC}-0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		$f_{SCL} > 100kHz$			$\frac{300ns}{C_b}$	
$t_{HD;STA}$	Hold time (repeated) START condition	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
t_{LOW}	Low period of SCL clock	$f_{SCL} \leq 100kHz$	4.7			µs
		$f_{SCL} > 100kHz$	1.3			
t_{HIGH}	High period of SCL clock	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq 100kHz$	4.7			µs
		$f_{SCL} > 100kHz$	0.6			

Table 36-106. Accuracy characteristics.

Symbol	Parameter	Condition [2]		Min.	Typ.	Max.	Units
RES	Resolution	Programmable to 8 or 12 bit		8	12	12	Bits
INL [1]	Integral non-linearity	500ksps	V_{CC}-1.0V < V_{REF}< V_{CC}-0.6V		±1.2	±2	lsb
			All V_{REF}		±1.5	±3	
		2000ksps	V_{CC}-1.0V < V_{REF}< V_{CC}-0.6V		±1.0	±2	
			All V_{REF}		±1.5	±3	
DNL [1]	Differential non-linearity	guaranteed monotonic			<±0.8	<±1	lsb
	Offset error				-1.0		mV
		Temperature drift			<0.01		mV/K
		Operating voltage drift			<0.6		mV/V
	Gain error	Differential mode	External reference		-1		mV
			AV_{CC}/1.6		10		
			AV_{CC}/2.0		8.0		
			Bandgap		±5		
		Temperature drift			<0.02		mV/K
		Operating voltage drift			<0.5		mV/V
	Noise	Differential mode, shorted input 2msps, V_{CC} = 3.6V, Clk_{PER} = 16MHz			0.4		mV rms

Notes:
1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external V_{REF} is used.

Table 36-107. Gain stage characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_{in}	Input resistance	Switched in normal mode			4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode			4.4		pF
	Signal range	Gain stage output		0		V_{CC}- 0.6	V
	Propagation delay	ADC conversion rate			1.0		Clk_{ADC} cycles
	Sample rate	Same as ADC		100		1000	kHz
INL [1]	Integral Non-Linearity	500ksps	All gain settings		±1.5	±4.0	lsb
	Gain error	1x gain, normal mode			-0.8		%
		8x gain, normal mode			-2.5		
		64x gain, normal mode			-3.5		

Figure 37-34. I/O pin input threshold voltage vs. V_{CC}.

V_{IL} I/O pin read as "0".

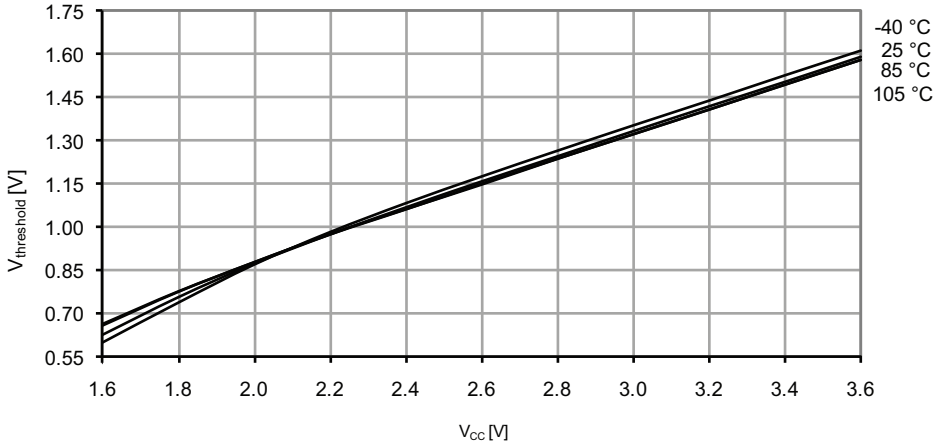


Figure 37-35. I/O pin input hysteresis vs. V_{CC}.

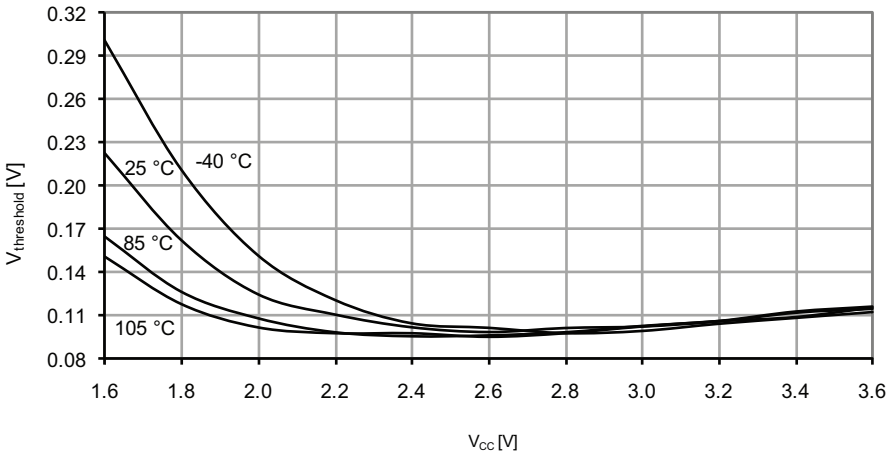
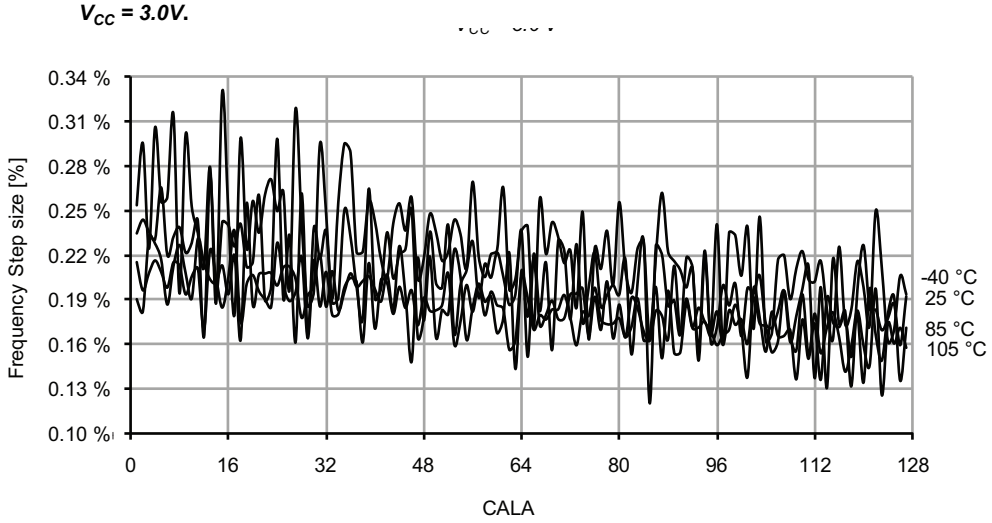


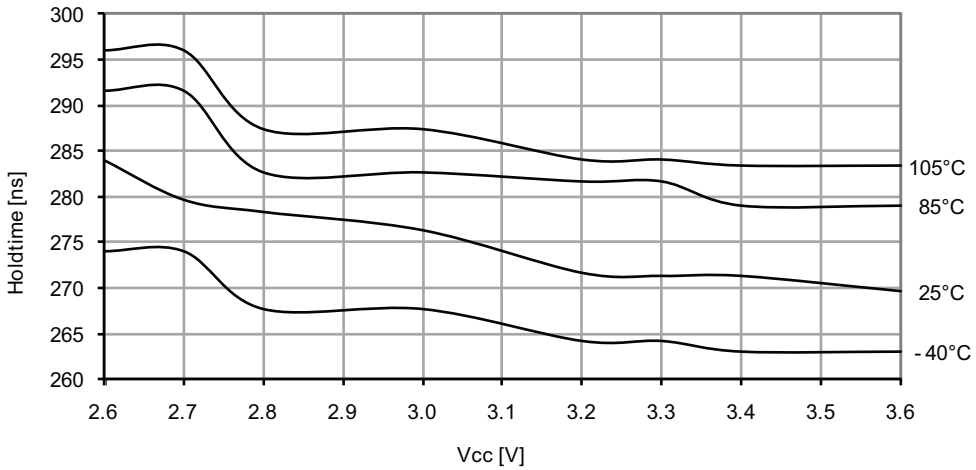
Figure 37-82. 48MHz internal oscillator CALA calibration step size.

V_{CC} = 3.0V.



37.1.11 Two-Wire Interface characteristics

Figure 37-83. SDA hold time vs. supply voltage.



37.1.12 PDI characteristics

Figure 37-84. Maximum PDI frequency vs. V_{CC}.

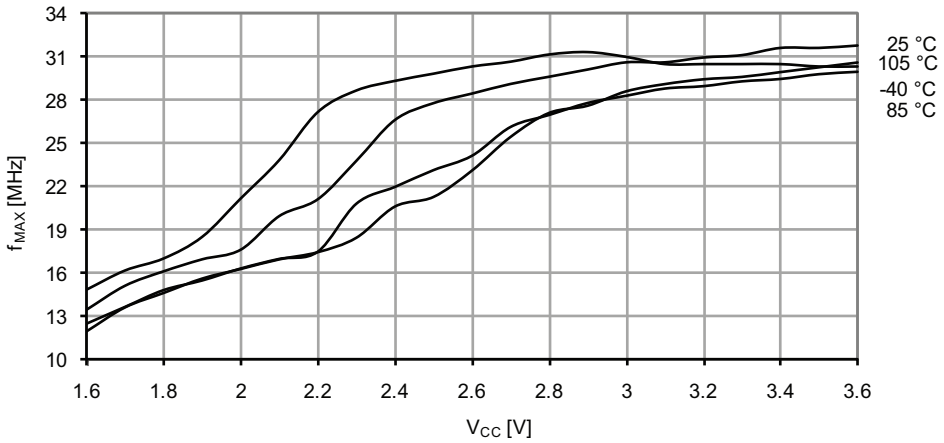
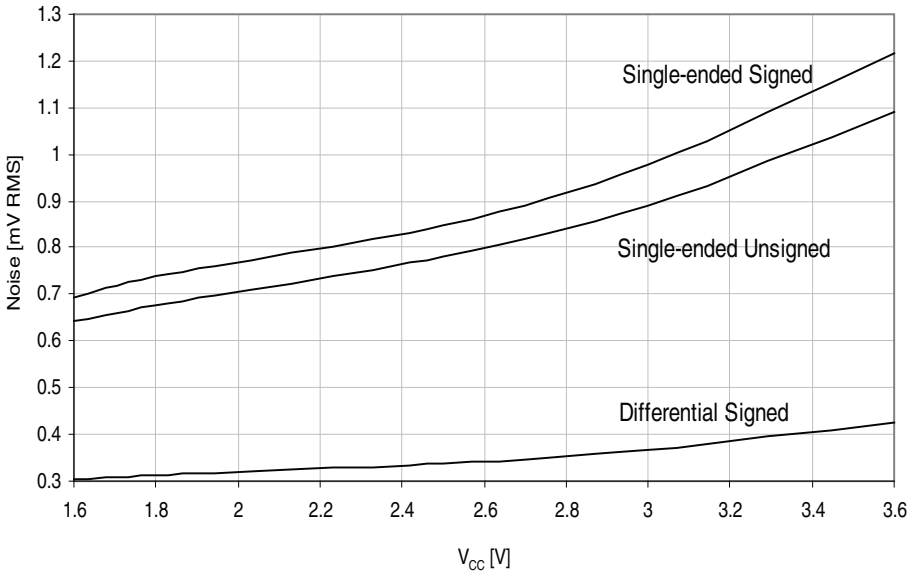


Figure 37-132. Noise vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.



37.2.4 DAC Characteristics

Figure 37-133. DAC INL error vs. V_{REF}.

V_{CC} = 3.6V.

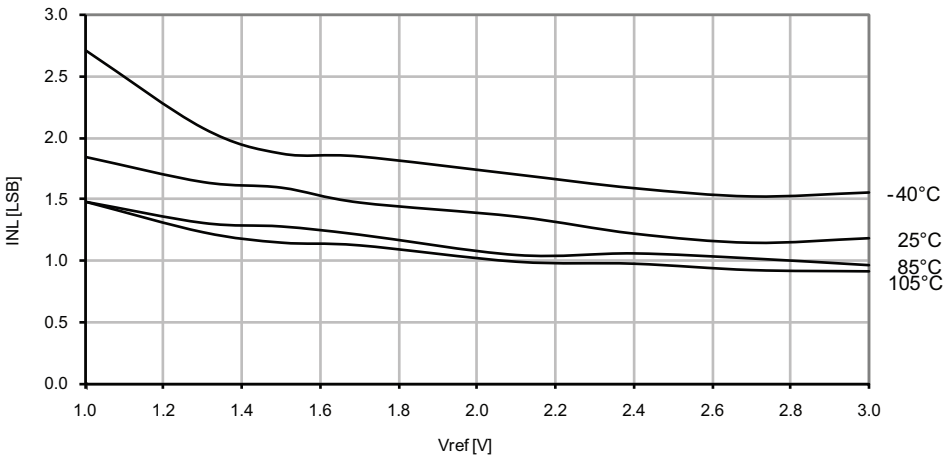


Figure 37-134. DNL error vs. V_{REF}.

V_{CC} = 3.6V.

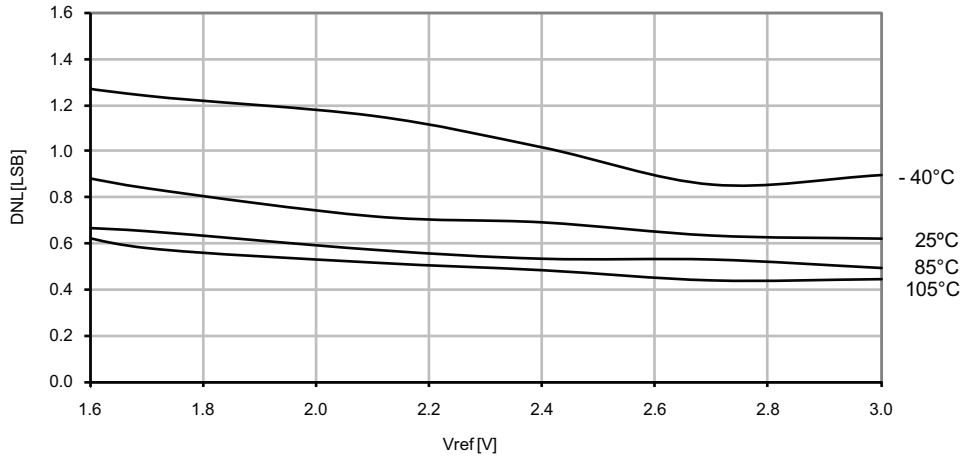
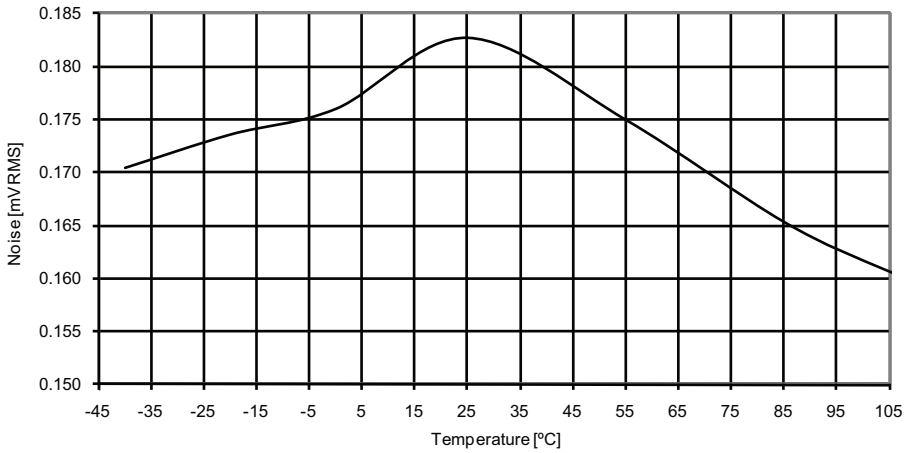


Figure 37-135. DAC noise vs. temperature.

V_{CC} = 3.0V, V_{REF} = 2.4V .



37.2.9 Power-on Reset Characteristics

Figure 37-152. Power-on reset current consumption vs. V_{CC}.

BOD level = 3.0V, enabled in continuous mode.

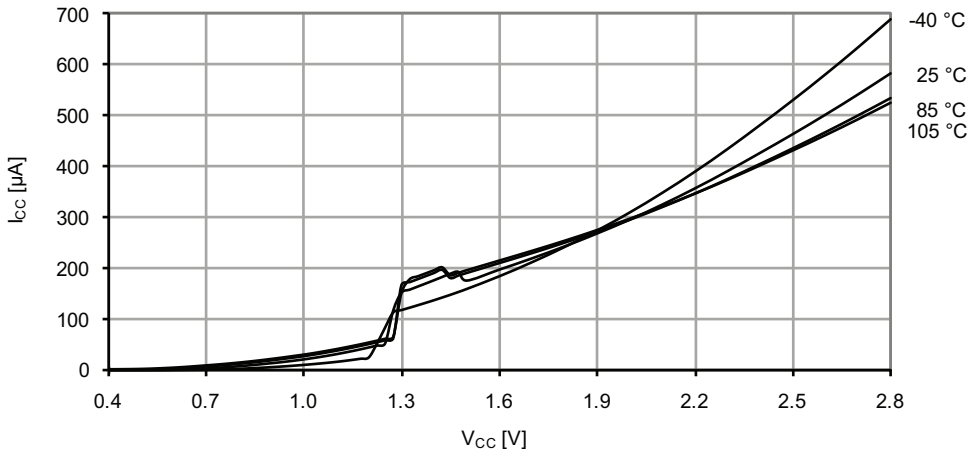
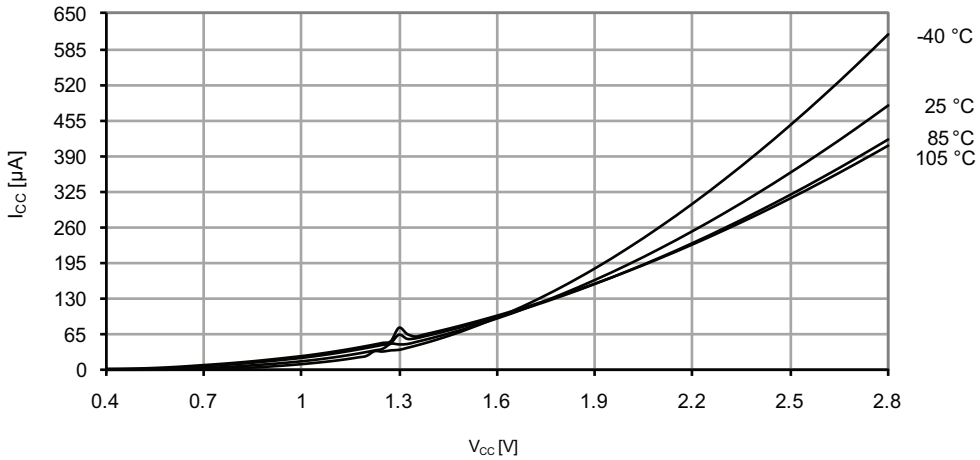


Figure 37-153. Power-on reset current consumption vs. V_{CC}.

BOD level = 3.0V, enabled in sampled mode.



37.2.12 PDI characteristics

Figure 37-168. Maximum PDI frequency vs. V_{CC}.

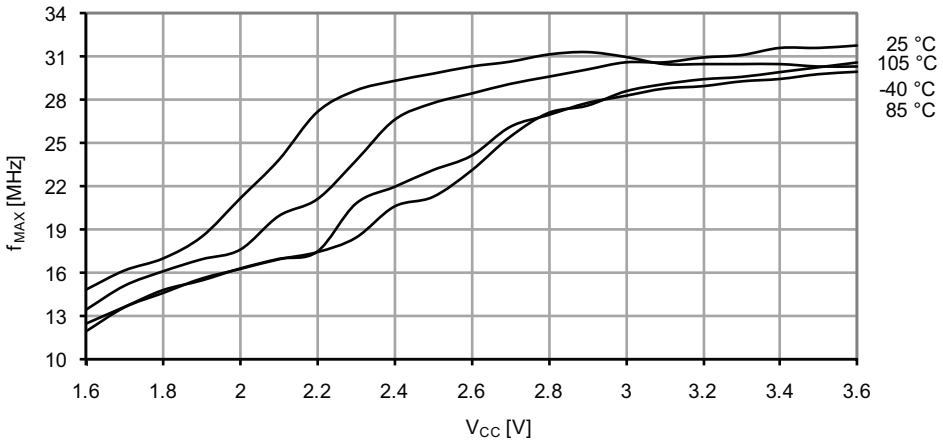
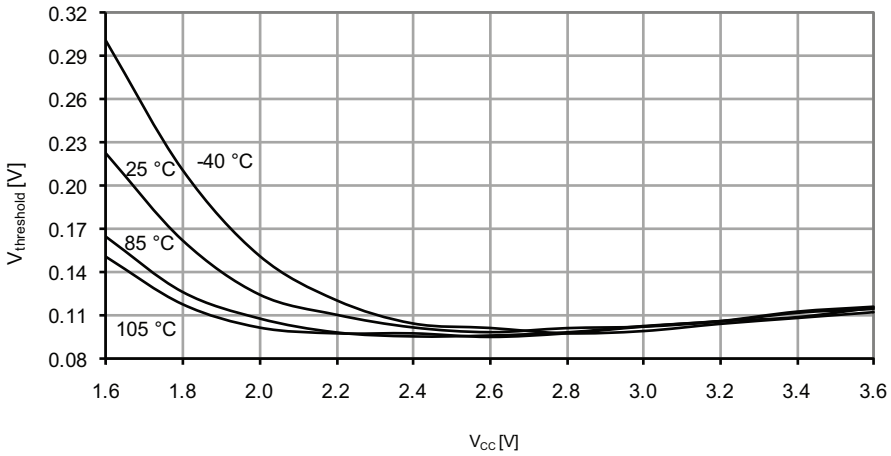


Figure 37-203. I/O pin input hysteresis vs. V_{CC}.



37.3.3 ADC Characteristics

Figure 37-204. INL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

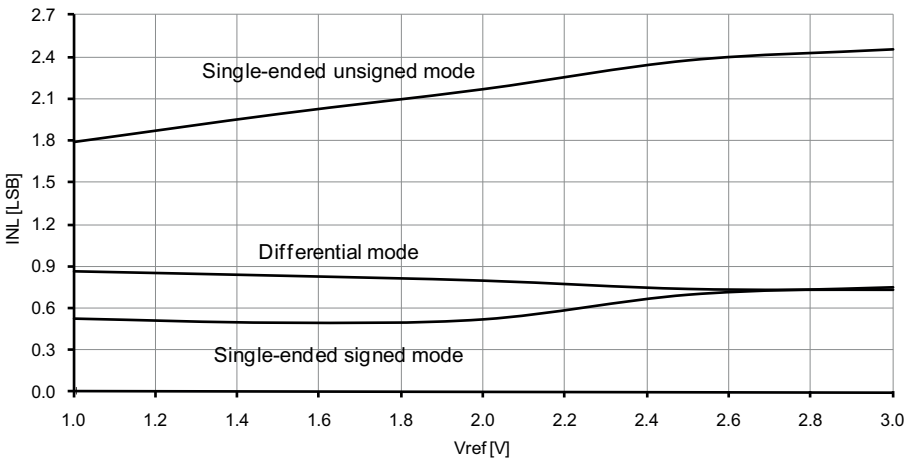


Figure 37-207. DNL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

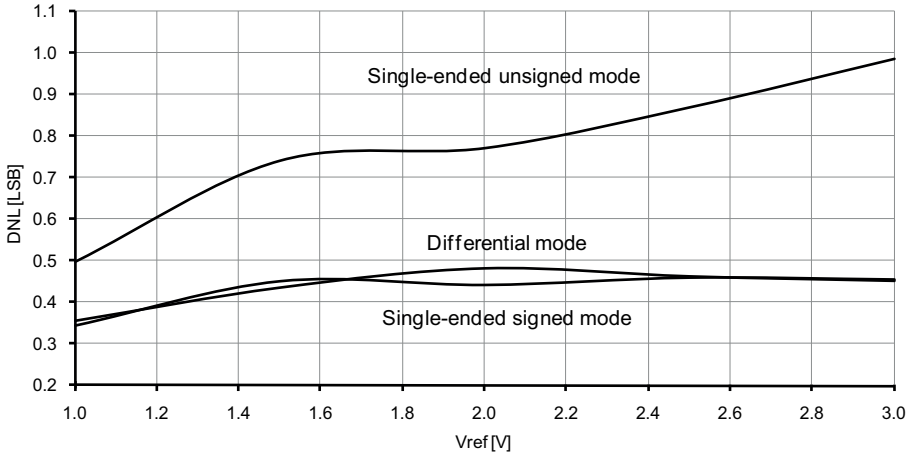


Figure 37-208. DNL error vs. sample rate.

T = 25°C, V_{CC} = 2.7V, V_{REF} = 1.0V external.

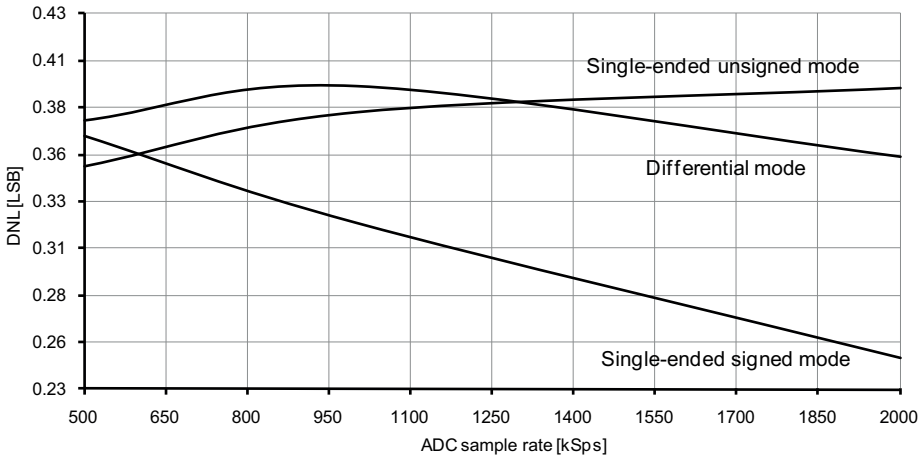


Figure 37-211. Gain error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.

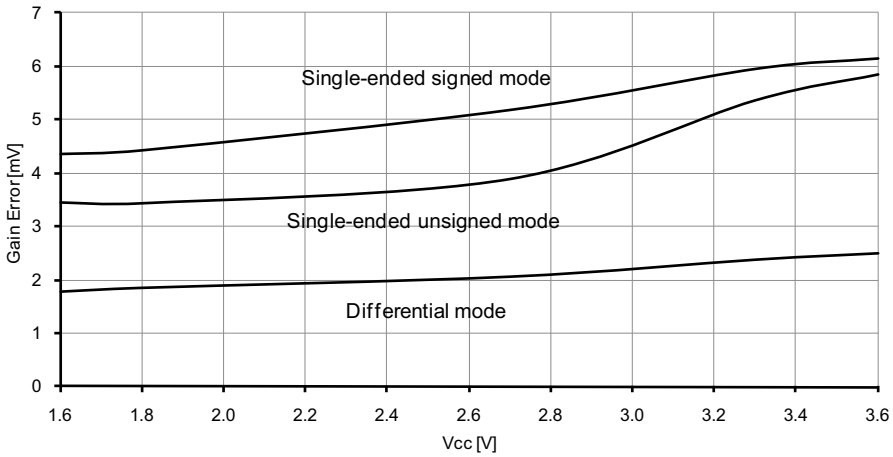
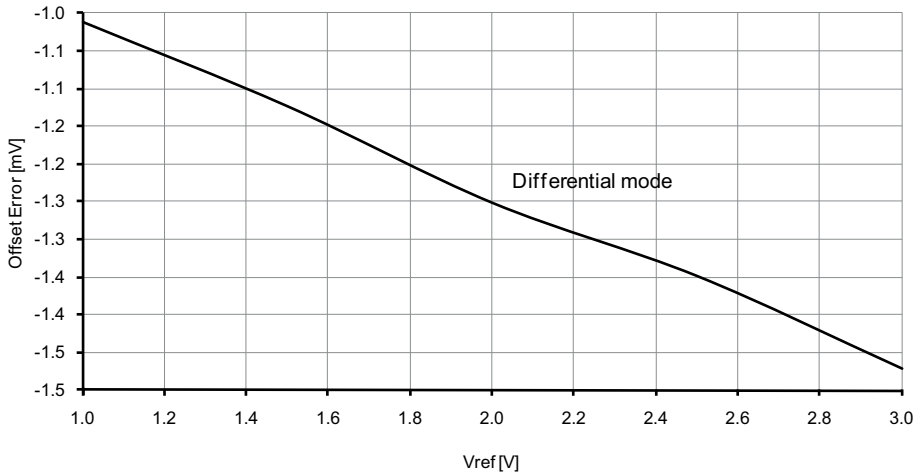


Figure 37-212. Offset error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps.



39. Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

39.1 8387H –09/2014

1.	Updated “Ordering Information” on page 2. Added ordering information for ATxmega16A4U/32A4U/64A4U/128A4U @ 105°C
2.	Updated the Application Table Section from 4K/4K/4K/4K to 8K/4K/4K/4K in the Figure 7-1 on page 14
3.	Updated Table 36-4 on page 74, Table 36-36 on page 95, Table 36-68 on page 117 and Table 36-100 on page 139. Added Icc Power-down power consumption for T=105°C for all functions disabled and for WDT and sampled BOD enabled
4.	Updated Table 36-20 on page 84, Table 36-52 on page 105, Table 36-84 on page 127 and Table 36-116 on page 149. Updated all tables to include values for T=85°C and T=105°C. Removed T=55°C
5.	Added 105°C Typical Characterization plots for: ATxmega16A4U ATxmega32A4U ATxmega64A4U ATxmega128A4U
6.	Changed Vcc to AVcc in Figure 28-1 on page 50 and in the text in Section 28. “ADC – 12-bit Analog to Digital Converter” on page 49 andSection 30. “AC – Analog Comparator” on page 53.
7.	Changed values for 128A4U in Table 7-3 on page 17. Page size = 128, FWORD = Z(6:0)
8.	Changed unit notation for parameter $t_{SU;DAT}$ to ns in Table 36-32 on page 92, Table 36-64 on page 113, and Table 36-128 on page 157.

39.2 8387G – 03/2014

1.	Removed “Preliminary” from the datasheet
2.	Updated “Errata” on page 327: added ERRATA “Rev. D” and “Rev. C” for “ATxmega64A4U” on page 329

39.3 8387F – 01/2014

1.	Removed JTAG references from the datasheet
2.	Updated Figure 30-1 on page 54. The positive Mux has two “Input” while the negative Mux has four “Input”

39.4 8387E – 11/2013

1.	Updated Flash size column in “Ordering Information” on page 2 for: ATxmega128A4U-AU, ATxmega128A4U-AUR, ATxmega128A4U-MH and ATxmega128A4U-MHR