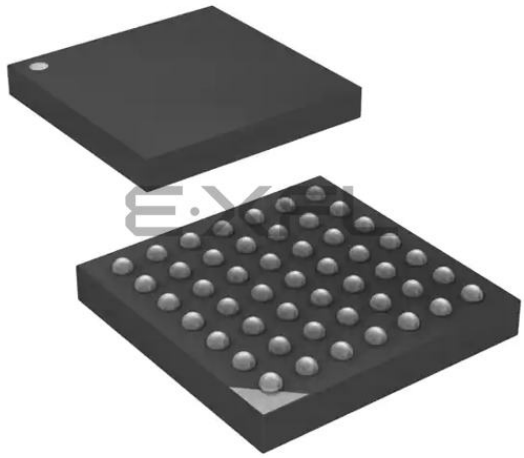

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	49-VFBGA
Supplier Device Package	49-VFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega16a4u-cur

4. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

4.1 Recommended reading

- Atmel AVR XMEGA AU manual
- XMEGA application notes

This device data sheet only contains part specific information with a short description of each peripheral and module. The XMEGA AU manual describes the modules and peripherals in depth. The XMEGA application notes contain example code and show applied use of the modules and peripherals.

All documentation are available from www.atmel.com/avr.

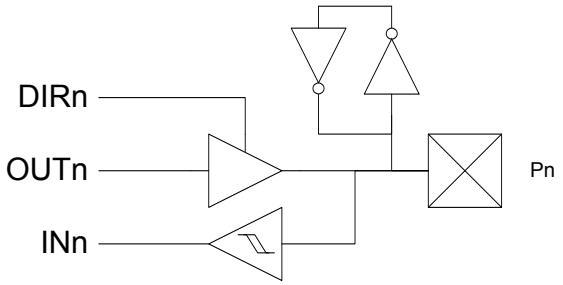
5. Capacitive touch sensing

The Atmel QTouch library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The QTouch library includes support for the QTouch and QMatrix acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch library for the AVR microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

The QTouch library is FREE and downloadable from the Atmel website at the following location: www.atmel.com/qtouchlibrary. For implementation details and other information, refer to the QTouch library user guide - also available for download from the Atmel website.

Figure 15-4. I/O configuration - Totem-pole with bus-keeper.



15.3.5 Others

Figure 15-5. Output configuration - Wired-OR with optional pull-down.

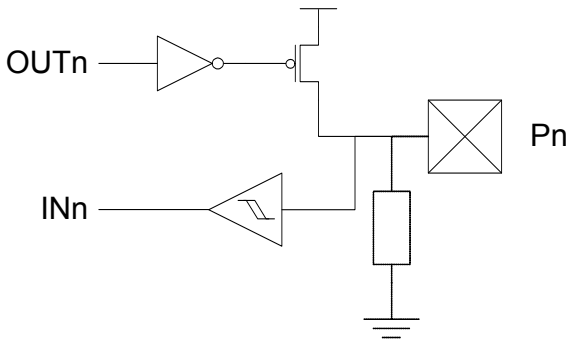
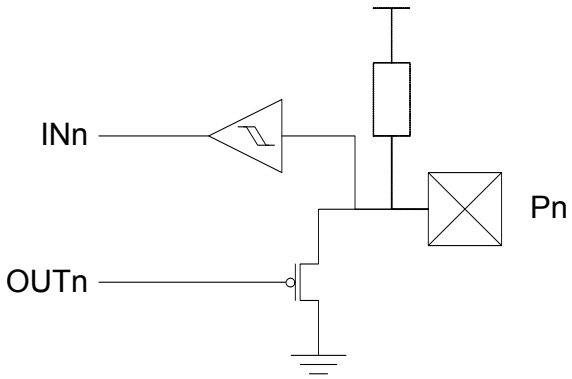


Figure 15-6. I/O configuration - Wired-AND with optional pull-up.



34. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
Arithmetic and Logic Instructions					
ADD	Rd, Rr	Add without Carry	Rd ← Rd + Rr	Z,C,N,V,S,H	1
ADC	Rd, Rr	Add with Carry	Rd ← Rd + Rr + C	Z,C,N,V,S,H	1
ADIW	Rd, K	Add Immediate to Word	Rd ← Rd + 1:Rd + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract without Carry	Rd ← Rd - Rr	Z,C,N,V,S,H	1
SUBI	Rd, K	Subtract Immediate	Rd ← Rd - K	Z,C,N,V,S,H	1
SBC	Rd, Rr	Subtract with Carry	Rd ← Rd - Rr - C	Z,C,N,V,S,H	1
SBCI	Rd, K	Subtract Immediate with Carry	Rd ← Rd - K - C	Z,C,N,V,S,H	1
SBIW	Rd, K	Subtract Immediate from Word	Rd + 1:Rd ← Rd + 1:Rd - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND	Rd ← Rd • Rr	Z,N,V,S	1
ANDI	Rd, K	Logical AND with Immediate	Rd ← Rd • K	Z,N,V,S	1
OR	Rd, Rr	Logical OR	Rd ← Rd v Rr	Z,N,V,S	1
ORI	Rd, K	Logical OR with Immediate	Rd ← Rd v K	Z,N,V,S	1
EOR	Rd, Rr	Exclusive OR	Rd ← Rd ⊕ Rr	Z,N,V,S	1
COM	Rd	One's Complement	Rd ← $FF - Rd	Z,C,N,V,S	1
NEG	Rd	Two's Complement	Rd ← $00 - Rd	Z,C,N,V,S,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V,S	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • ($FFh - K)	Z,N,V,S	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V,S	1
DEC	Rd	Decrement	Rd ← Rd - 1	Z,N,V,S	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V,S	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V,S	1
SER	Rd	Set Register	Rd ← $FF	None	1
MUL	Rd,Rr	Multiply Unsigned	R1:R0 ← Rd x Rr (UU)	Z,C	2
MULS	Rd,Rr	Multiply Signed	R1:R0 ← Rd x Rr (SS)	Z,C	2
MULSU	Rd,Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr (SU)	Z,C	2
FMUL	Rd,Rr	Fractional Multiply Unsigned	R1:R0 ← Rd x Rr<<1 (UU)	Z,C	2
FMULS	Rd,Rr	Fractional Multiply Signed	R1:R0 ← Rd x Rr<<1 (SS)	Z,C	2
FMULSU	Rd,Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← Rd x Rr<<1 (SU)	Z,C	2
DES	K	Data Encryption	if (H = 0) then R15:R0 ← Encrypt(R15:R0, K) else if (H = 1) then R15:R0 ← Decrypt(R15:R0, K)		1/2
Branch instructions					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2
EIJMP		Extended Indirect Jump to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	2
JMP	k	Jump	PC ← k	None	3

Table 36-5. Current consumption for modules and peripherals.

Symbol	Parameter	Condition [1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				1.0		µA
	32.768kHz int. oscillator				27		µA
	2MHz int. oscillator				85		µA
		DFLL enabled with 32.768kHz int. osc. as reference			115		
	32MHz int. oscillator				270		µA
		DFLL enabled with 32.768kHz int. osc. as reference			460		
	PLL	20x multiplication factor, 32MHz int. osc. DIV4 as reference			220		µA
	Watchdog timer				1.0		µA
	BOD	Continuous mode			138		µA
		Sampled mode, includes ULP oscillator			1.2		
	Internal 1.0V reference				100		µA
	Temperature sensor				95		µA
	ADC	250ksps V_{REF} = Ext ref			3.0		mA
			CURRLIMIT = LOW		2.6		
			CURRLIMIT = MEDIUM		2.1		
			CURRLIMIT = HIGH		1.6		
	DAC	250ksps V_{REF} = Ext ref No load	Normal mode		1.9		mA
			Low Power mode		1.1		
	AC	High speed mode			330		µA
		Low power mode			130		
	DMA	615kbps between I/O registers and SRAM			108		µA
	Timer/counter				16		µA
	USART	Rx and Tx enabled, 9600 BAUD			2.5		µA
	Flash memory and EEPROM programming				4.0	8.0	mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

36.1.14.5 Internal Phase Locked Loop (PLL) characteristics

Table 36-26. Internal PLL characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency (1)	V_{CC}= 1.6 - 1.8V	20		48	MHz
		V_{CC}= 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		µs

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

36.1.14.6 External clock characteristics

Figure 36-3. External clock drive waveform

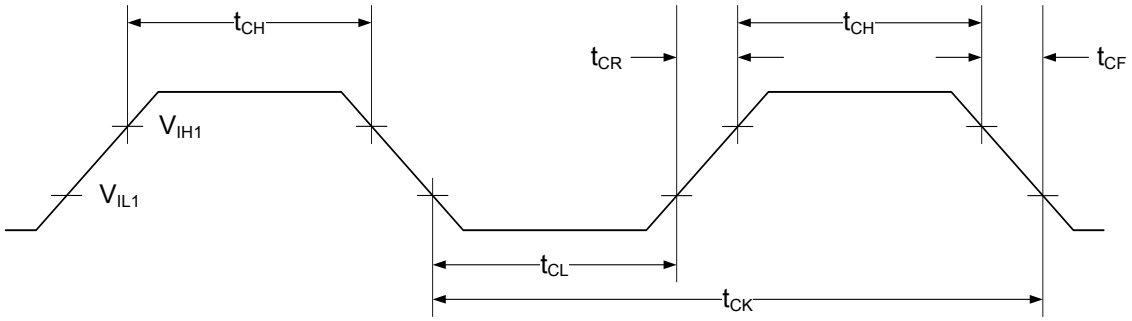


Table 36-27. External clock used as system clock without prescaling.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (1)	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

Table 36-60. External clock with prescaler [1] for system clock.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency [2]	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

36.2.14.7 External 16MHz crystal oscillator and XOSC characteristic

Table 36-61. External 16MHz crystal oscillator and XOSC characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0		<10		ns
			FRQRANGE=1, 2, or 3		<1		
		XOSCPWR=1			<1		
	Long term jitter	XOSCPWR=0	FRQRANGE=0		<6		ns
			FRQRANGE=1, 2, or 3		<0.5		
		XOSCPWR=1			<0.5		
	Frequency error	XOSCPWR=0	FRQRANGE=0		<0.1		%
			FRQRANGE=1		<0.05		
			FRQRANGE=2 or 3		<0.005		
		XOSCPWR=1			<0.005		
	Duty cycle	XOSCPWR=0	FRQRANGE=0		40		%
			FRQRANGE=1		42		
			FRQRANGE=2 or 3		45		
		XOSCPWR=1			48		

36.2.15 SPI Characteristics

Figure 36-12. SPI timing requirements in master mode.

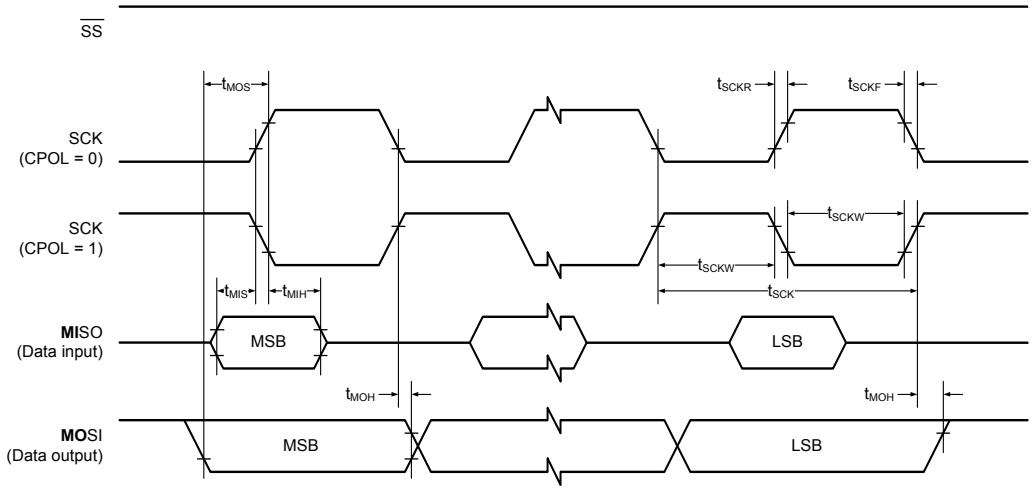
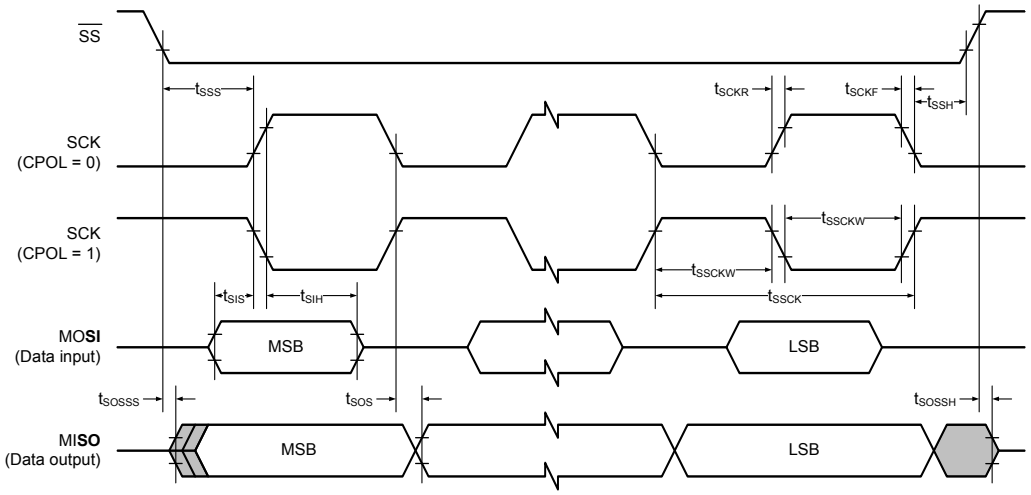


Figure 36-13. SPI timing requirements in slave mode.



Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$t_{HD;DAT}$	Data hold time	$f_{SCL} \leq 100kHz$	0		3.45	µs
		$f_{SCL} > 100kHz$	0		0.9	
$t_{SU;DAT}$	Data setup time	$f_{SCL} \leq 100kHz$	250			ns
		$f_{SCL} > 100kHz$	100			
$t_{SU;STO}$	Setup time for STOP condition	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
t_{BUF}	Bus free time between a STOP and START condition	$f_{SCL} \leq 100kHz$	4.7			µs
		$f_{SCL} > 100kHz$	1.3			

Notes:
1. Required only for $f_{SCL} > 100kHz$.
2. C_b = Capacitance of one bus line in pF.
3. f_{PER} = Peripheral clock frequency.

Table 36-101.Current consumption for modules and peripherals.

Symbol	Parameter	Condition [1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				1.0		µA
	32.768kHz int. oscillator				29		µA
	2MHz int. oscillator				85		µA
		DFLL enabled with 32.768kHz int. osc. as reference			115		
	32MHz int. oscillator				270		µA
		DFLL enabled with 32.768kHz int. osc. as reference			440		
	PLL	20x multiplication factor, 32MHz int. osc. DIV4 as reference			320		µA
	Watchdog timer				1.0		µA
	BOD	Continuous mode			138		µA
		Sampled mode, includes ULP oscillator			1.2		
	Internal 1.0V reference				260		µA
	Temperature sensor				250		µA
	ADC	250ksps V_{REF} = Ext ref			3.0		mA
			CURRLIMIT = LOW		2.6		
			CURRLIMIT = MEDIUM		2.1		
			CURRLIMIT = HIGH		1.6		
	DAC	250ksps V_{REF} = Ext ref No load	Normal mode		1.9		mA
			Low power mode		1.1		
	AC	High speed mode			330		µA
		Low power mode			130		
	DMA	615kbps between I/O registers and SRAM			108		µA
	Timer/counter				16		µA
	USART	Rx and Tx enabled, 9600 BAUD			2.5		µA
	Flash memory and EEPROM programming				4.0	8.0	mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

36.4.16 Two-Wire Interface Characteristics

Table 36-128 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 36-28.

Figure 36-28. Two-wire interface bus timing.

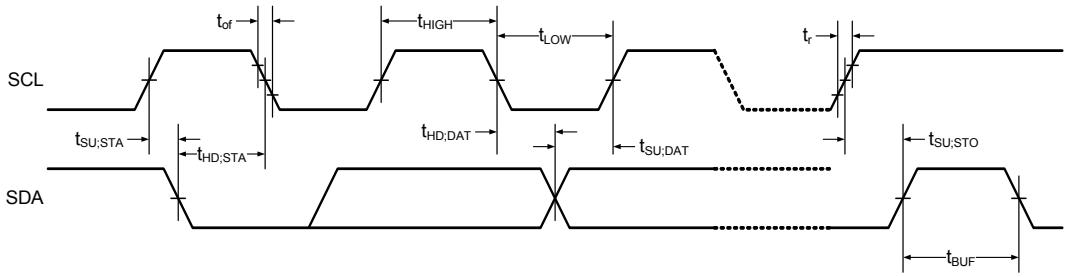


Table 36-128. Two-wire interface characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		$0.7V_{CC}$		V_{CC}+0.5	V
V_{IL}	Input Low Voltage		0.5		$0.3\times V_{CC}$	V
V_{hys}	Hysteresis of Schmitt Trigger Inputs		$0.05V_{CC}$ (1)			V
V_{OL}	Output Low Voltage	3mA, sink current	0		0.4	V
t_r	Rise Time for both SDA and SCL		$20+0.1C_b$ (1)(2)		300	ns
t_{of}	Output Fall Time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF$ (2)	$20+0.1C_b$ (1)(2)		250	ns
t_{SP}	Spikes Suppressed by Input Filter		0		50	ns
I_I	Input Current for each I/O Pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	µA
C_I	Capacitance for each I/O Pin				10	pF
f_{SCL}	SCL Clock Frequency	f_{PER} (3)>max($10f_{SCL}$, 250kHz)	0		400	kHz
R_P	Value of Pull-up resistor	$f_{SCL} \le 100kHz$	$\frac{V_{CC}-0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		$f_{SCL} > 100kHz$			$\frac{300ns}{C_b}$	
$t_{HD;STA}$	Hold Time (repeated) START condition	$f_{SCL} \le 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
t_{LOW}	Low Period of SCL Clock	$f_{SCL} \le 100kHz$	4.7			µs
		$f_{SCL} > 100kHz$	1.3			
t_{HIGH}	High Period of SCL Clock	$f_{SCL} \le 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \le 100kHz$	4.7			µs
		$f_{SCL} > 100kHz$	0.6			

37.1.1.5 Standby mode supply current

Figure 37-19. Standby supply current vs. V_{CC}.

Standby, f_{SYS} = 1MHz.

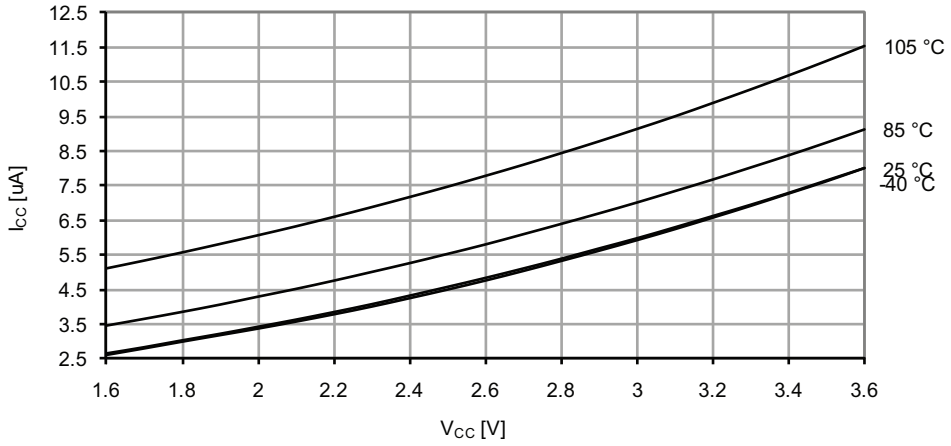
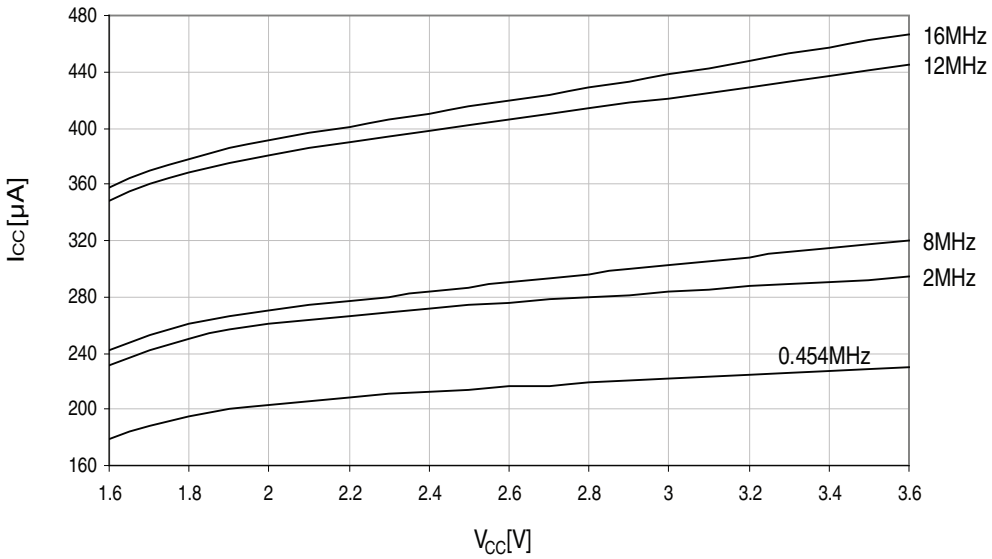


Figure 37-20. Standby supply current vs. V_{CC}.

25°C, running from different crystal oscillators.



37.1.2.3 Thresholds and Hysteresis

Figure 37-32. I/O pin input threshold voltage vs. V_{CC}.
T = 25°C.

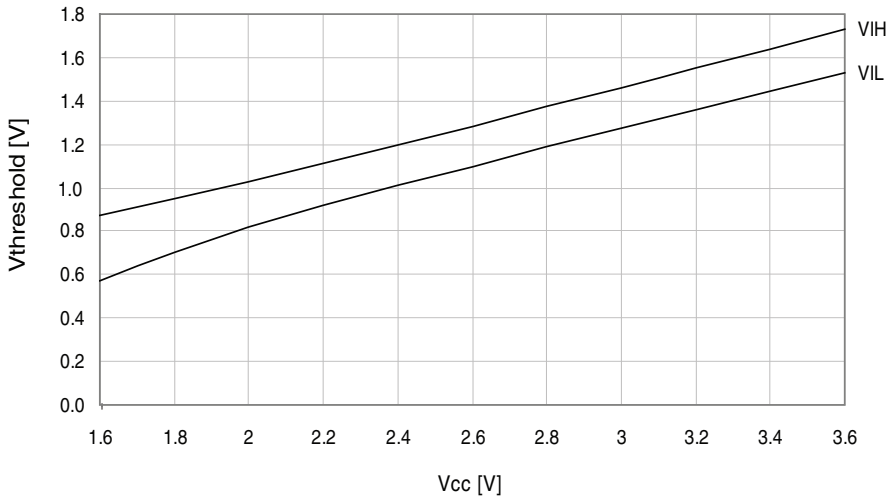


Figure 37-33. I/O pin input threshold voltage vs. V_{CC}.
V_{IH} I/O pin read as "1".

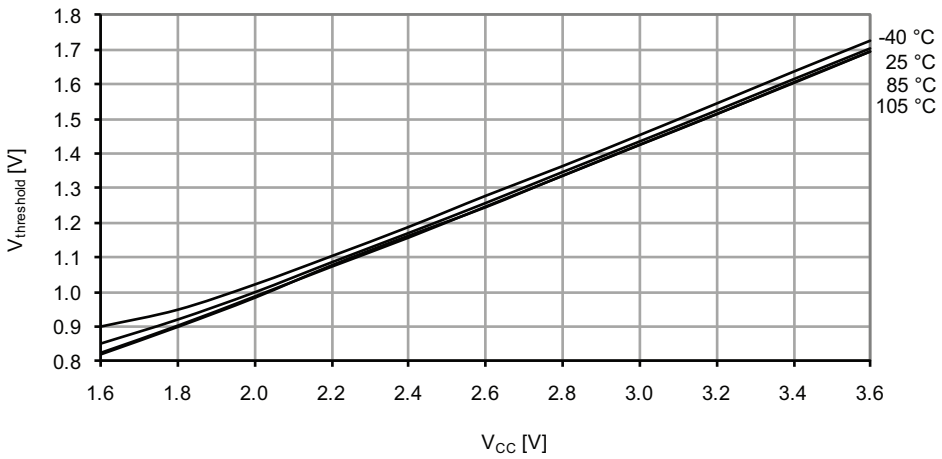
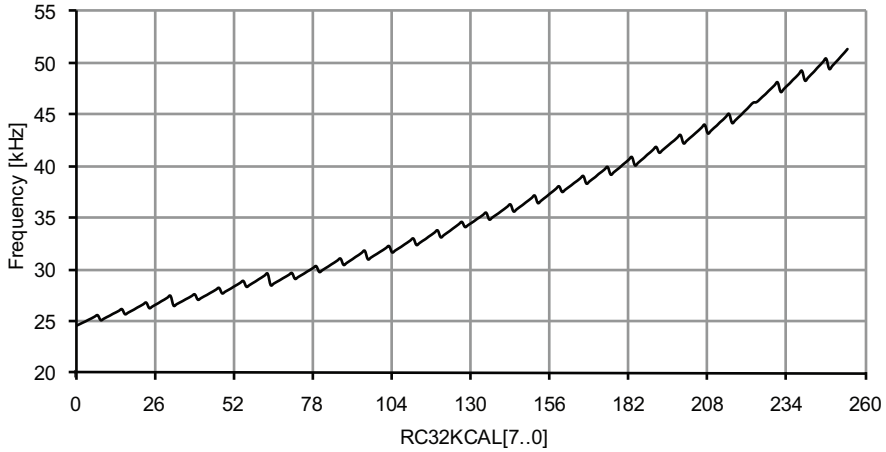


Figure 37-72. 32.768kHz internal oscillator frequency vs. calibration value.

V_{CC} = 3.0V, T = 25°C.



37.1.10.3 2MHz Internal Oscillator

Figure 37-73. 2MHz internal oscillator frequency vs. temperature.

DFLL disabled.

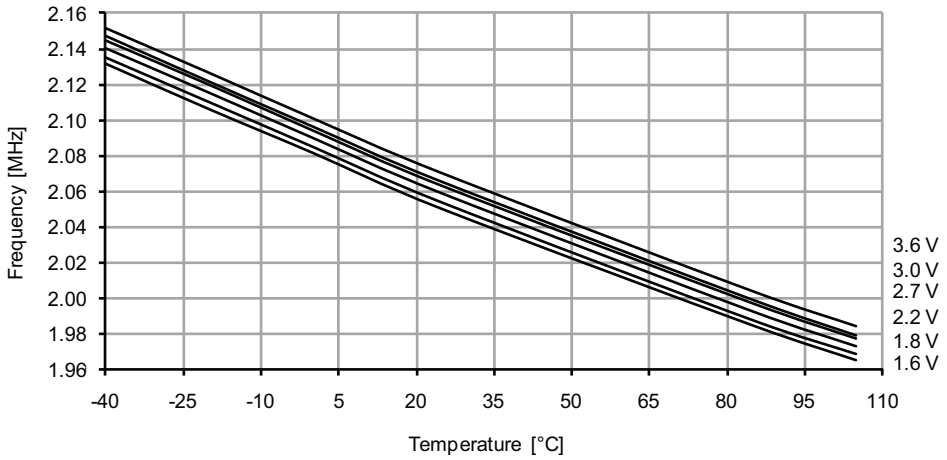


Figure 37-87.Active mode supply current vs. V_{CC}.

f_{SYS} = 32.768kHz internal oscillator.

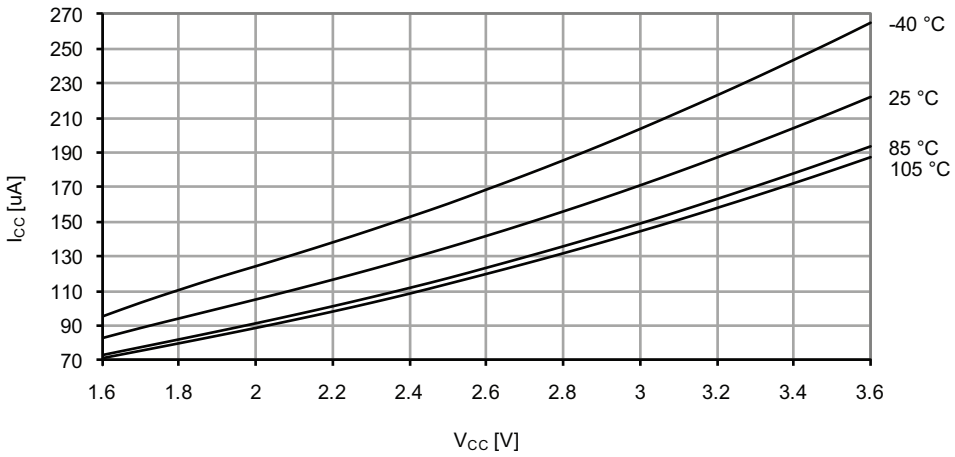


Figure 37-88.Active mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

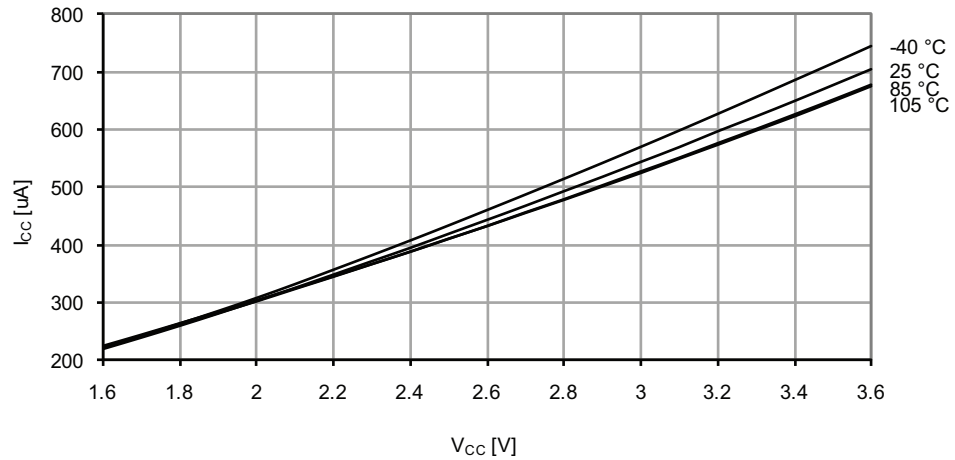


Figure 37-122. INL error vs. input code

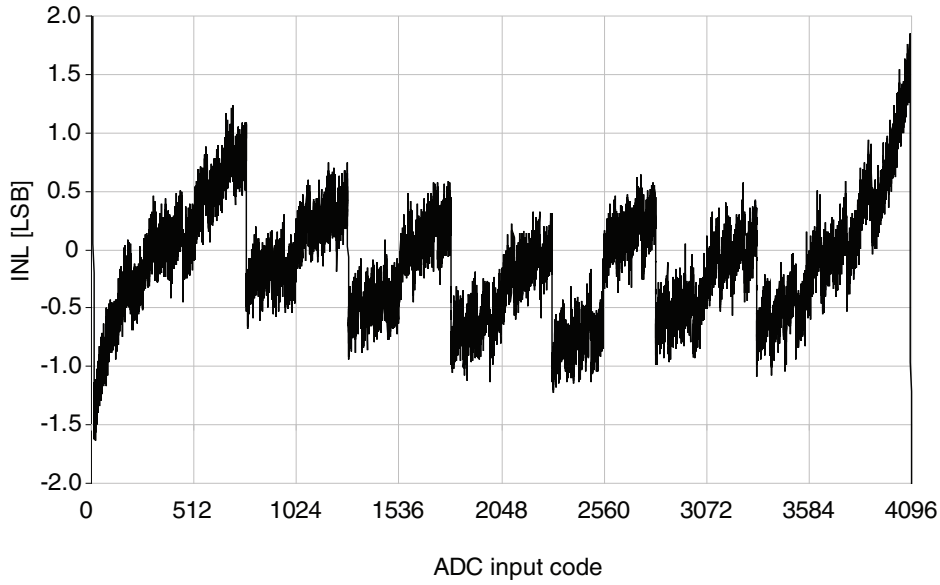


Figure 37-123. DNL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

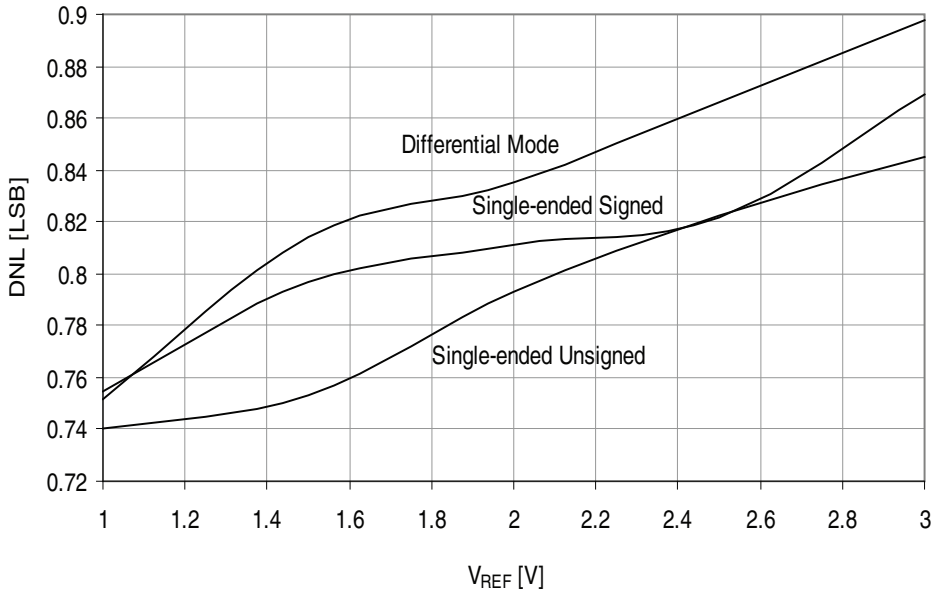


Figure 37-134. DNL error vs. V_{REF}.

V_{CC} = 3.6V.

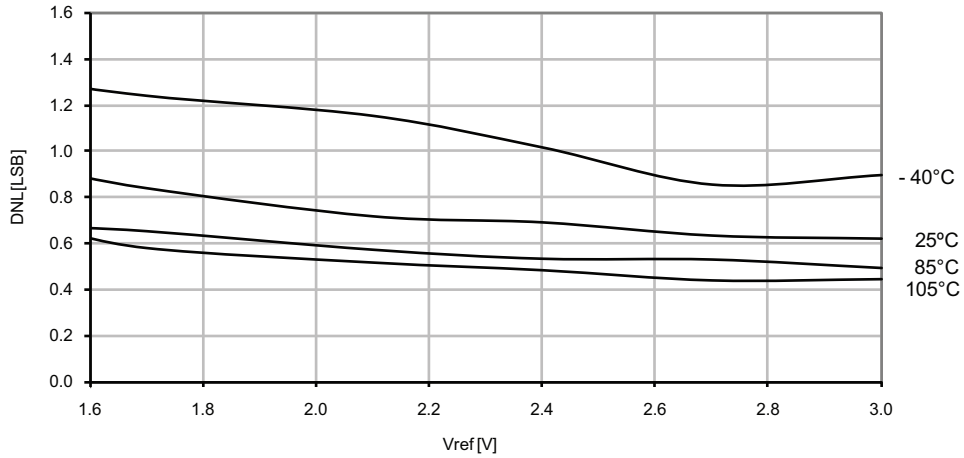


Figure 37-135. DAC noise vs. temperature.

V_{CC} = 3.0V, V_{REF} = 2.4V .

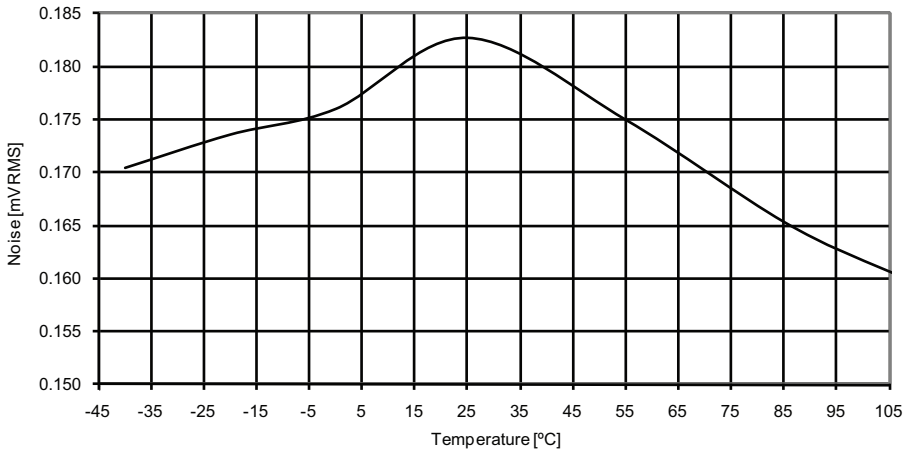
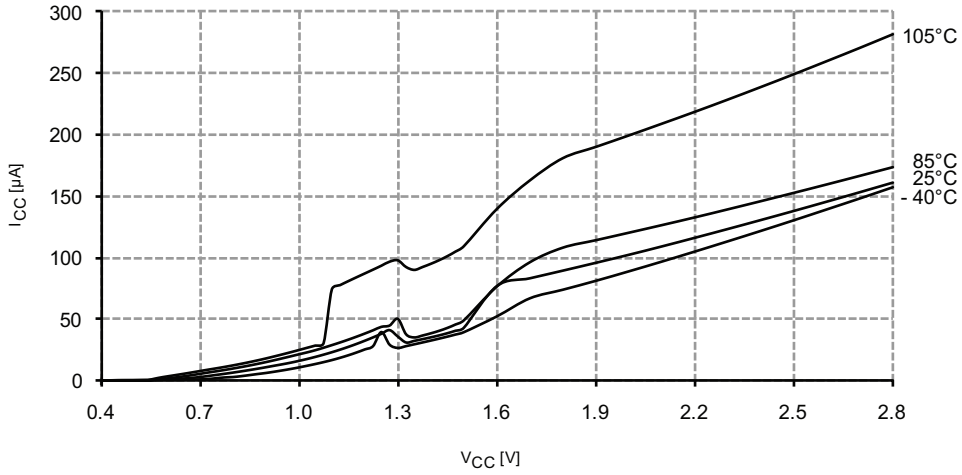


Figure 37-237. Power-on reset current consumption vs. V_{CC}.

BOD level = 3.0V, enabled in sampled mode.



37.3.10 Oscillator Characteristics

37.3.10.1 Ultra Low-Power internal oscillator

Figure 37-238. Ultra Low-Power internal oscillator frequency vs. temperature.

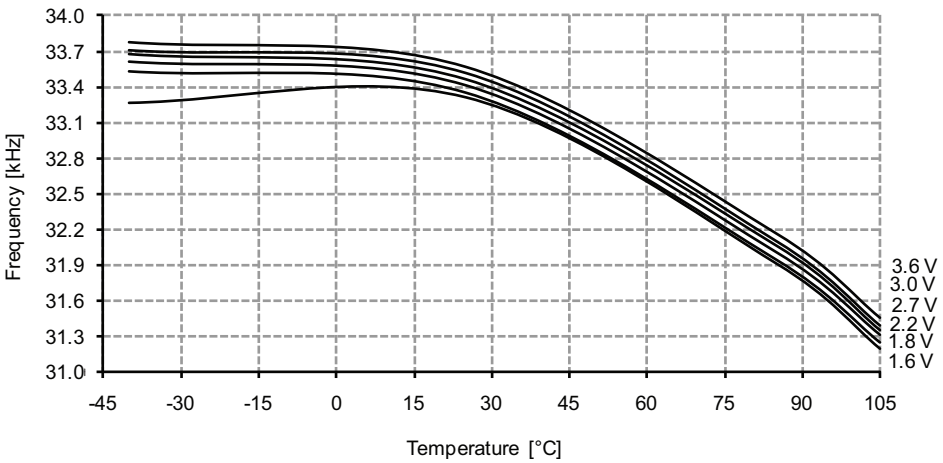


Figure 37-263. Idle mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock

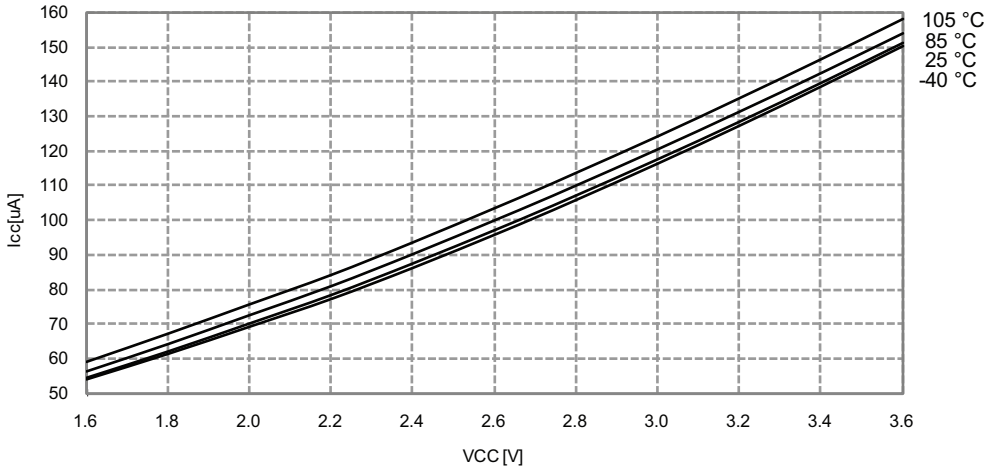
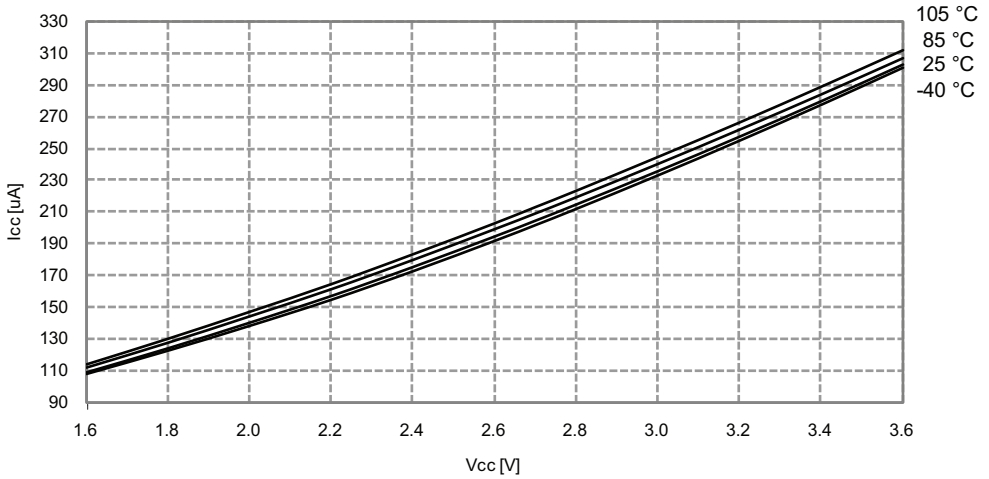


Figure 37-264. Idle mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator



37.4.2 I/O Pin Characteristics

37.4.2.1 Pull-up

Figure 37-273. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 1.8V

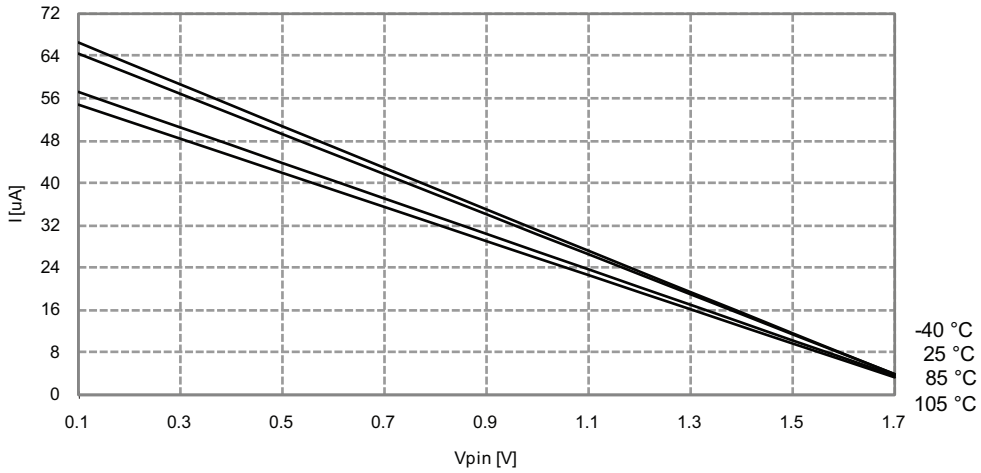


Figure 37-274. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 3.0V

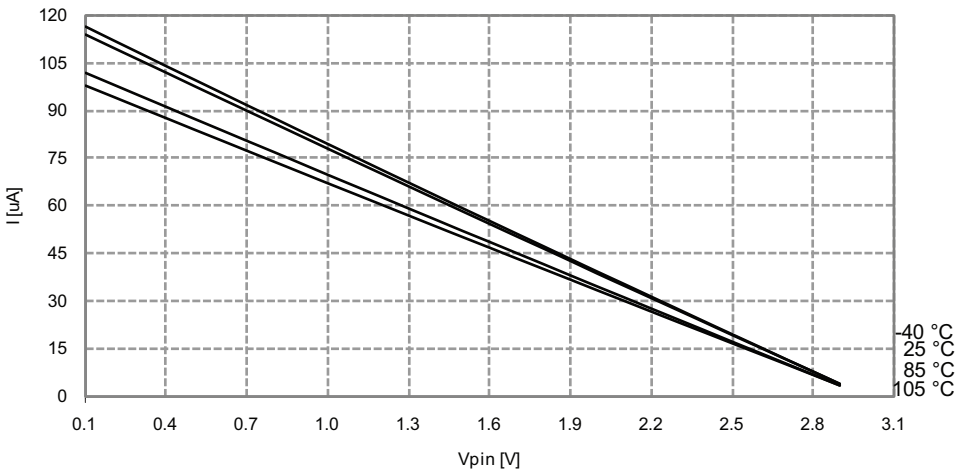


Figure 37-309. Analog comparator current source vs. calibration value.

V_{CC} = 3.0V.

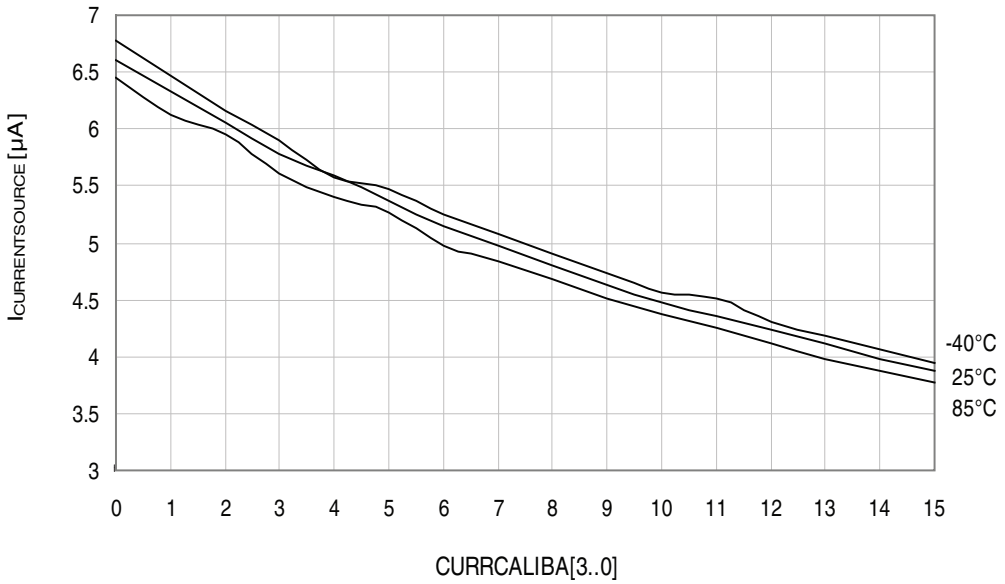


Figure 37-310. Voltage scaler INL vs. SCALEFAC.

T = 25°C, V_{CC} = 3.0V.