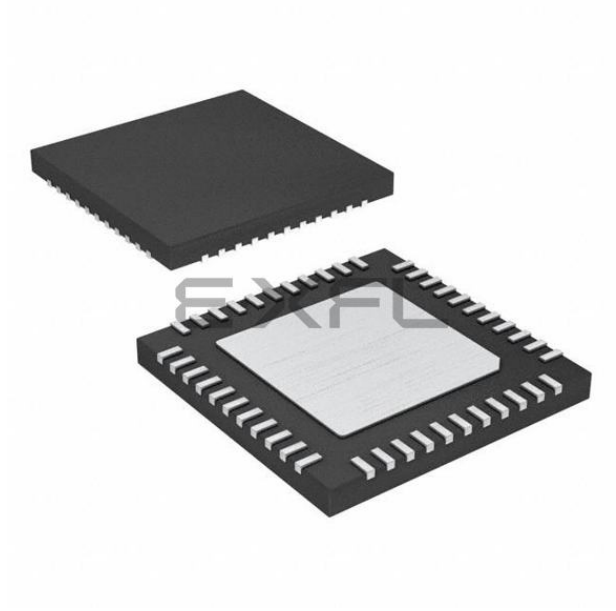

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega16a4u-mnr

11. Power Management and Sleep Modes

11.1 Features

- Power management for adjusting power consumption and functions
- Five sleep modes
  - Idle
  - Power down
  - Power save
  - Standby
  - Extended standby
- Power reduction register to disable clock and turn off unused peripherals in active and idle modes

11.2 Overview

Various sleep modes and clock gating are provided in order to tailor power consumption to application requirements. This enables the Atmel AVR XMEGA microcontroller to stop unused modules to save power.

All sleep modes are available and can be entered from active mode. In active mode, the CPU is executing application code. When the device enters sleep mode, program execution is stopped and interrupts or a reset is used to wake the device again. The application code decides which sleep mode to enter and when. Interrupts from enabled peripherals and all enabled reset sources can restore the microcontroller from sleep to active mode.

In addition, power reduction registers provide a method to stop the clock to individual peripherals from software. When this is done, the current state of the peripheral is frozen, and there is no power consumption from that peripheral. This reduces the power consumption in active mode and idle sleep modes and enables much more fine-tuned power management than sleep modes alone.

11.3 Sleep Modes

Sleep modes are used to shut down modules and clock domains in the microcontroller in order to save power. XMEGA microcontrollers have five different sleep modes tuned to match the typical functional stages during application execution. A dedicated sleep instruction (SLEEP) is available to enter sleep mode. Interrupts are used to wake the device from sleep, and the available interrupt wake-up sources are dependent on the configured sleep mode. When an enabled interrupt occurs, the device will wake up and execute the interrupt service routine before continuing normal program execution from the first instruction after the SLEEP instruction. If other, higher priority interrupts are pending when the wake-up occurs, their interrupt service routines will be executed according to their priority before the interrupt service routine for the wake-up interrupt is executed. After wake-up, the CPU is halted for four cycles before execution starts.

The content of the register file, SRAM and registers are kept during sleep. If a reset occurs during sleep, the device will reset, start up, and execute from the reset vector.

11.3.1 Idle Mode

In idle mode the CPU and nonvolatile memory are stopped (note that any ongoing programming will be completed), but all peripherals, including the interrupt controller, event system and DMA controller are kept running. Any enabled interrupt will wake the device.

11.3.2 Power-down Mode

In power-down mode, all clocks, including the real-time counter clock source, are stopped. This allows operation only of asynchronous modules that do not require a running clock. The only interrupts that can wake up the MCU are the two-wire interface address match interrupt, asynchronous port interrupts, and the USB resume interrupt.

27. CRC – Cyclic Redundancy Check Generator

27.1 Features

- Cyclic redundancy check (CRC) generation and checking for
  - Communication data
  - Program or data in flash memory
  - Data in SRAM and I/O memory space
- Integrated with flash memory, DMA controller and CPU
  - Continuous CRC on data going through a DMA channel
  - Automatic CRC of the complete or a selectable range of the flash memory
  - CPU can load data to the CRC generator through the I/O interface
- CRC polynomial software selectable to
  - CRC-16 (CRC-CCITT)
  - CRC-32 (IEEE 802.3)
- Zero remainder detection

27.2 Overview

A cyclic redundancy check (CRC) is an error detection technique test algorithm used to find accidental errors in data, and it is commonly used to determine the correctness of a data transmission, and data present in the data and program memories. A CRC takes a data stream or a block of data as input and generates a 16- or 32-bit output that can be appended to the data and used as a checksum. When the same data are later received or read, the device or application repeats the calculation. If the new CRC result does not match the one calculated earlier, the block contains a data error. The application will then detect this and may take a corrective action, such as requesting the data to be sent again or simply not using the incorrect data.

Typically, an n-bit CRC applied to a data block of arbitrary length will detect any single error burst not longer than n bits (any single alteration that spans no more than n bits of the data), and will detect the fraction $1-2^{-n}$ of all longer error bursts. The CRC module in Atmel AVR XMEGA devices supports two commonly used CRC polynomials; CRC-16 (CRC-CCITT) and CRC-32 (IEEE 802.3).

- **CRC-16:**

Polynomial:	$x^{16}+x^{12}+x^5+1$
Hex value:	0x1021

- **CRC-32:**

Polynomial:	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$
Hex value:	0x04C11DB7

36.1.14 Clock and Oscillator Characteristics

36.1.14.1 Calibrated 32.768kHz Internal Oscillator characteristics

Table 36-22. 32.768kHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	%

36.1.14.2 Calibrated 2MHz RC Internal Oscillator characteristics

Table 36-23. 2MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8		2.2	MHz
	Factory calibrated frequency			2.0		MHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	%
	DFLL calibration stepsize			0.21		%

36.1.14.3 Calibrated and tunable 32MHz internal oscillator characteristics

Table 36-24. 32MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30		55	MHz
	Factory calibrated frequency			32		MHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	%
	DFLL calibration step size			0.22		%

36.1.14.4 32kHz Internal ULP Oscillator characteristics

Table 36-25. 32kHz internal ULP oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Output frequency			32		kHz
	Accuracy		-30		30	%

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Offset error, input referred	1x gain, normal mode			-2.0		mV
		8x gain, normal mode			-5.0		
		64x gain, normal mode			-4.0		
	Noise	1x gain, normal mode	V_{CC} = 3.6V Ext. V_{REF}		0.5		mV rms
		8x gain, normal mode			1.5		
		64x gain, normal mode			11		

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.

36.2.7 DAC Characteristics

Table 36-44. Power supply, reference and output range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	V
AV_{REF}	External reference voltage		1.0		V_{CC}- 0.6	V
$R_{channel}$	DC output impedance				50	Ω
	Linear output voltage range		0.15		AV_{CC}-0.15	V
R_{AREF}	Reference input resistance			>10		MΩ
CAREF	Reference input capacitance	Static load		7.0		pF
	Minimum Resistance load		1.0			kΩ
	Maximum capacitance load				100	pF
		1000Ω serial resistance			1.0	nF
	Output sink/source	Operating within accuracy specification			AV_{CC}/1000	mA
		Safe operation			10	

Table 36-45. Clock and timing.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
f_{DAC}	Conversion rate	C_{load}=100pF, maximum step size	Normal mode	0		1000	ksps
			Low power mode			500	

36.4 ATxmega128A4U

36.4.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 36-97 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 36-97. Absolute maximum ratings.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	mA
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC}+0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	°C

36.4.2 General Operating Ratings

The device must operate within the ratings listed in Table 36-98 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 36-98. General operating conditions.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	V
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	°C

Table 36-99. Operating voltage and frequency.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 36-22 the Frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

37.1.1.5 Standby mode supply current

Figure 37-19. Standby supply current vs. V_{CC}.

Standby, f_{SYS} = 1MHz.

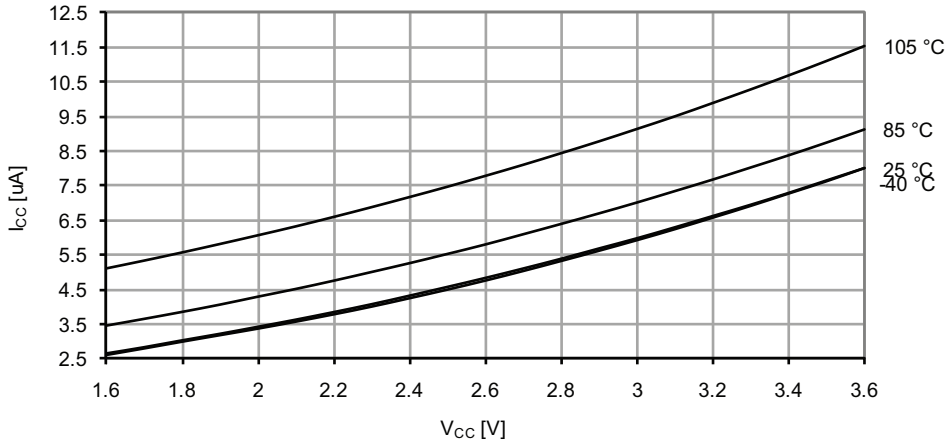


Figure 37-20. Standby supply current vs. V_{CC}.

25°C, running from different crystal oscillators.

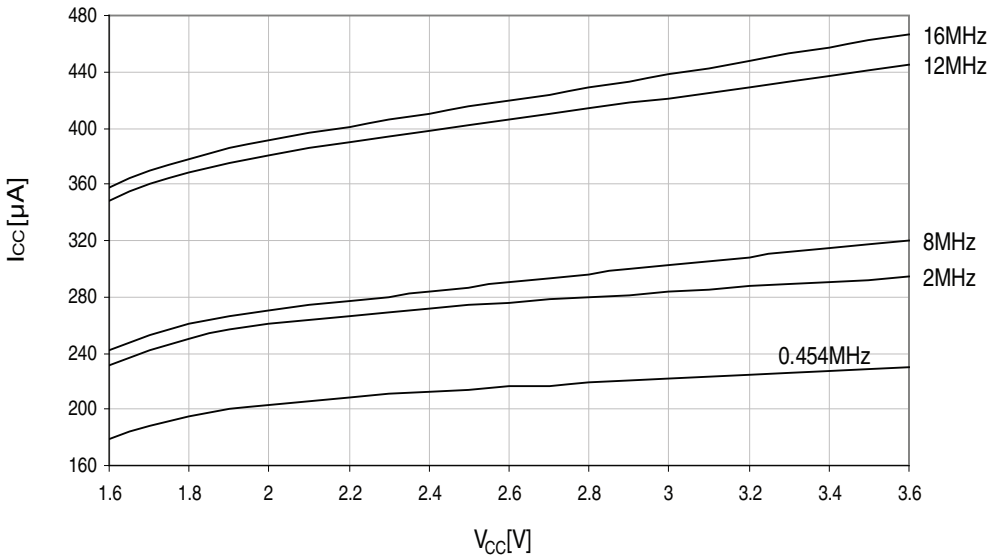
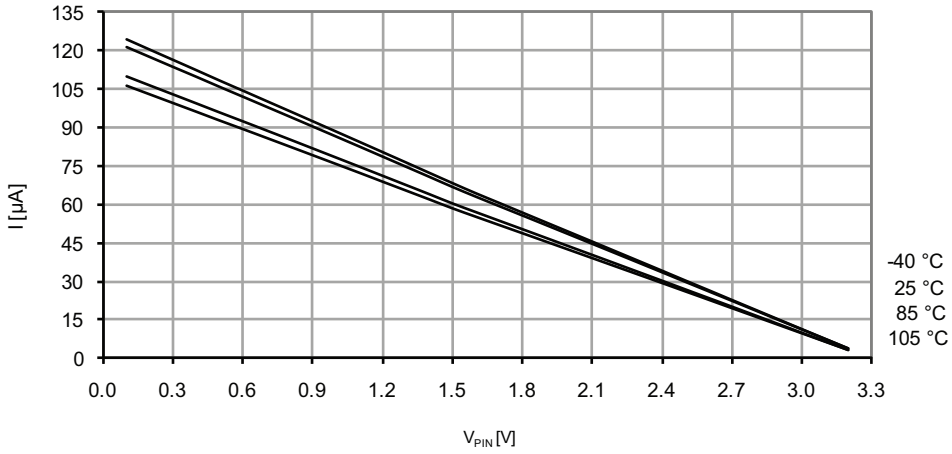


Figure 37-23. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 3.3V.



37.1.2.2 Output Voltage vs. Sink/Source Current

Figure 37-24. I/O pin output voltage vs. source current.

V_{CC} = 1.8V.

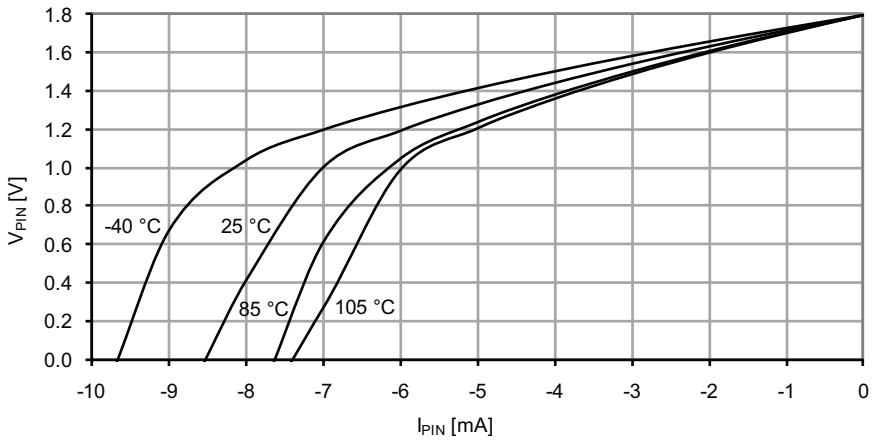


Figure 37-34. I/O pin input threshold voltage vs. V_{CC}.

V_{IL} I/O pin read as "0".

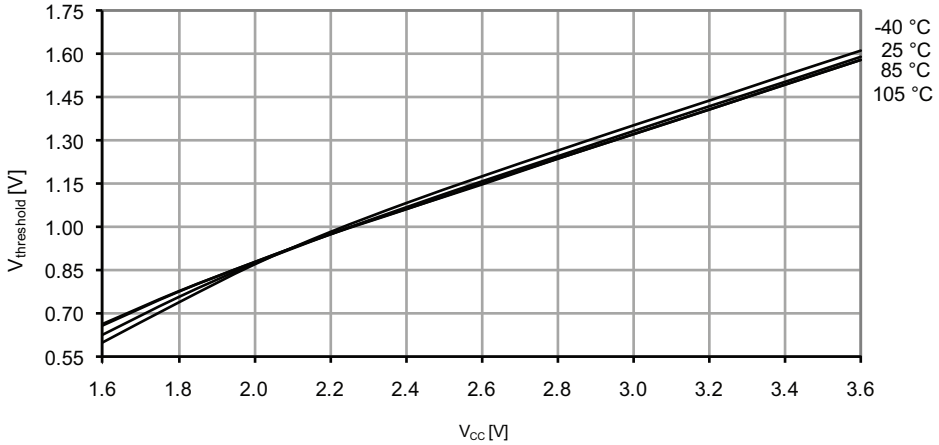


Figure 37-35. I/O pin input hysteresis vs. V_{CC}.

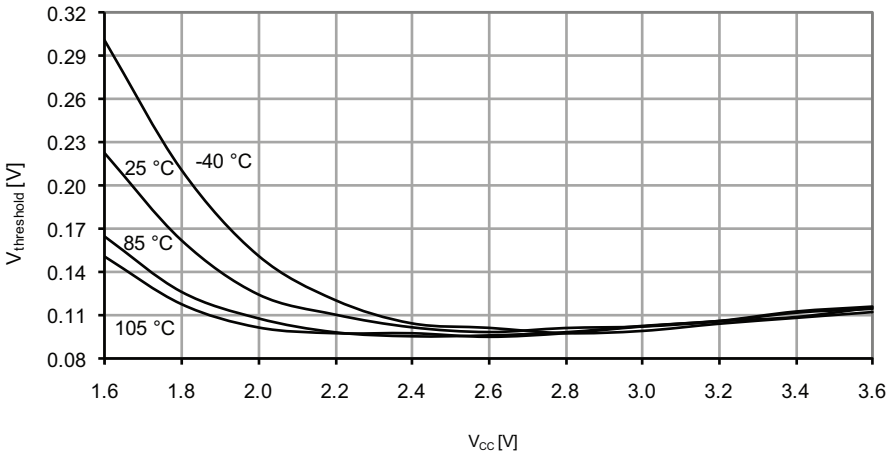


Figure 37-46. Offset error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.

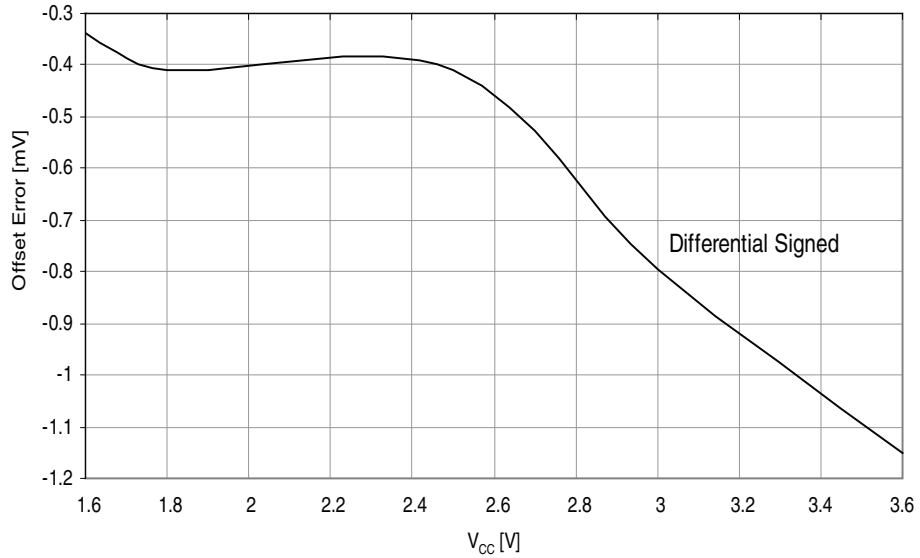


Figure 37-47. Noise vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps.

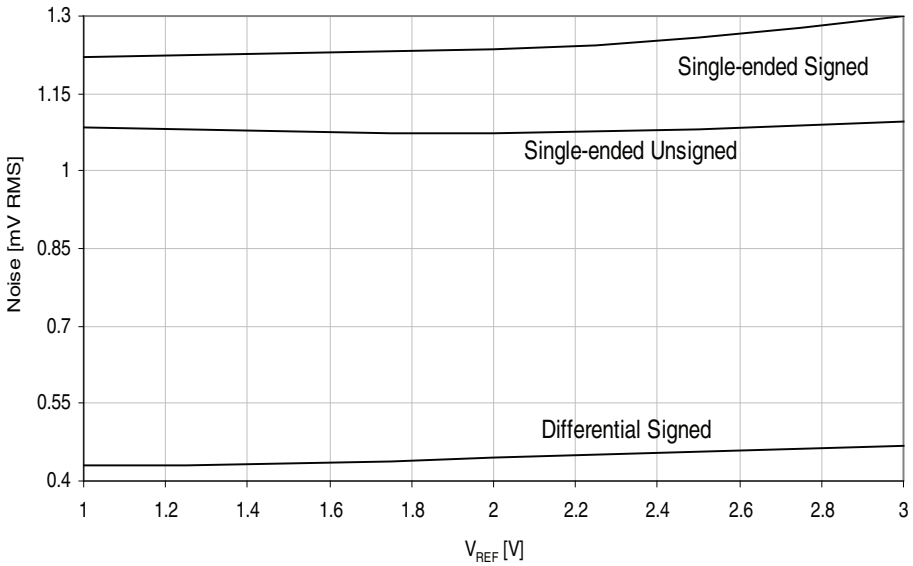
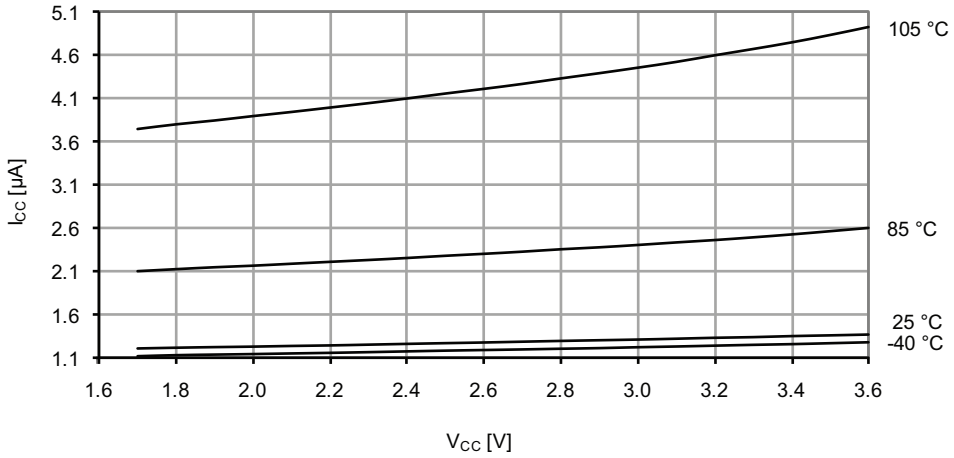


Figure 37-101. Power-down mode supply current vs. V_{CC}.

Watchdog and sampled BOD enabled.



37.2.1.4 Power-save mode supply current

Figure 37-102. Power-save mode supply current vs.V_{CC}.

Real Time Counter enabled and running from 1.024kHz output of 32.768kHz TOSC.

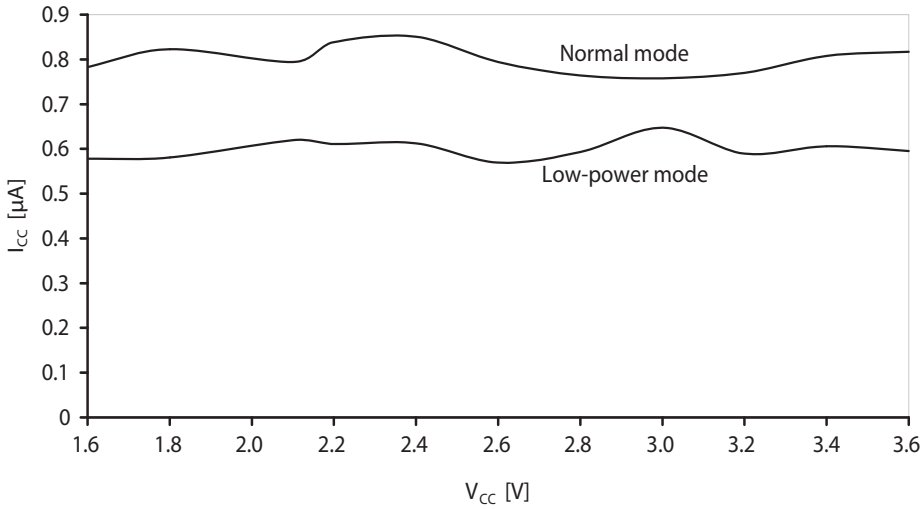


Figure 37-134. DNL error vs. V_{REF}.

V_{CC} = 3.6V.

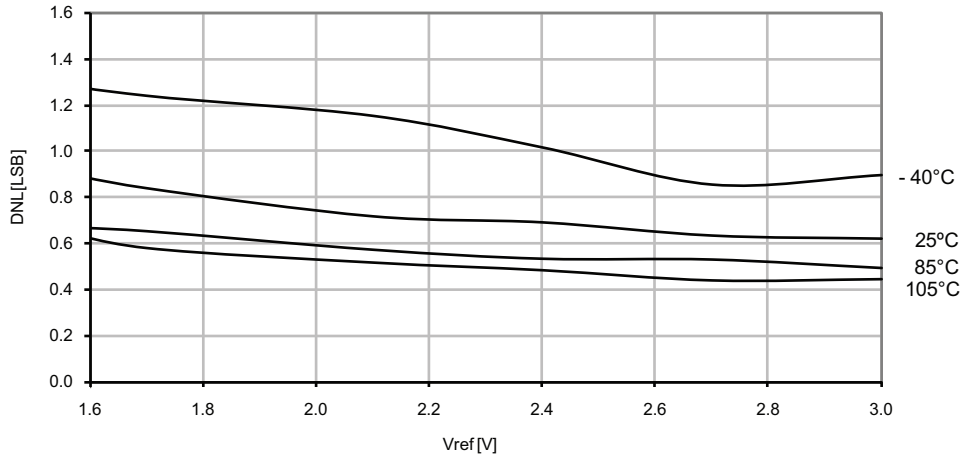


Figure 37-135. DAC noise vs. temperature.

V_{CC} = 3.0V, V_{REF} = 2.4V .

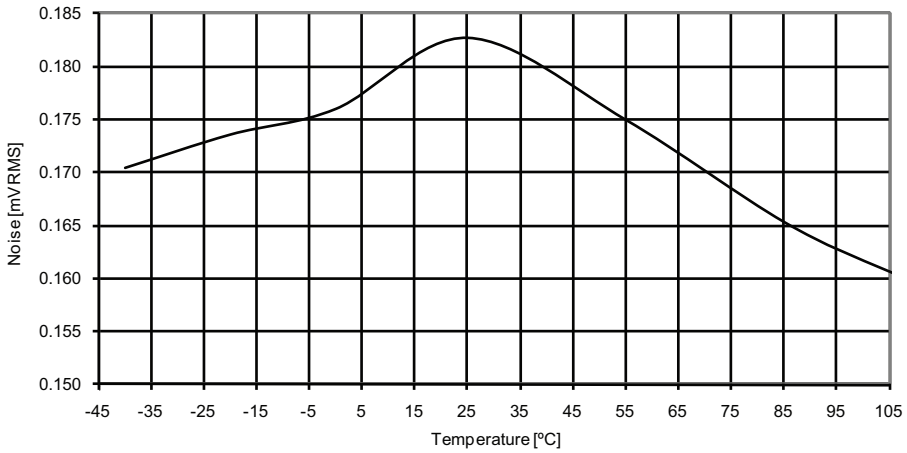


Figure 37-138. Analog comparator hysteresis vs. V_{CC}.

High-speed mode, large hysteresis.

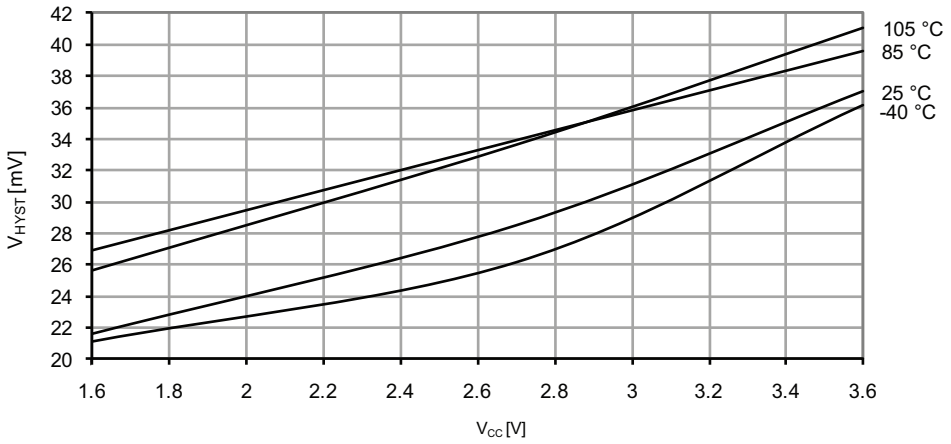
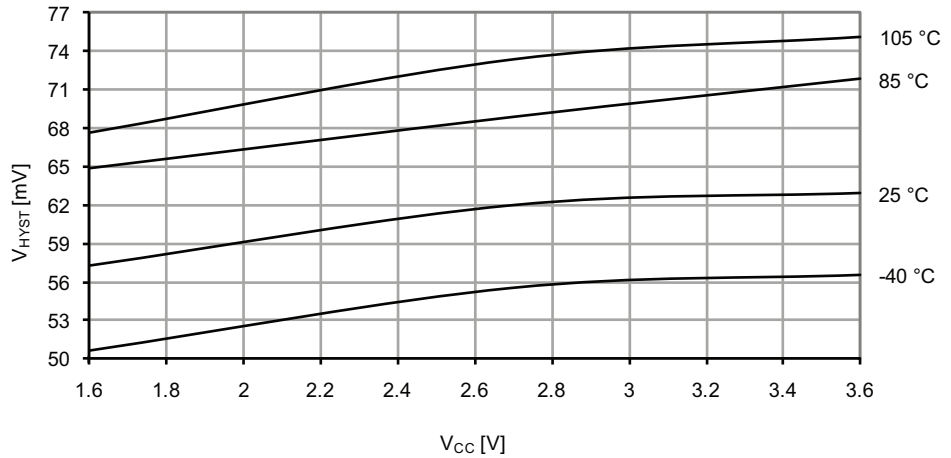


Figure 37-139. Analog comparator hysteresis vs. V_{CC}.

Low power, large hysteresis.



37.2.7 BOD Characteristics

Figure 37-144. BOD thresholds vs. temperature.

BOD level = 1.6V.

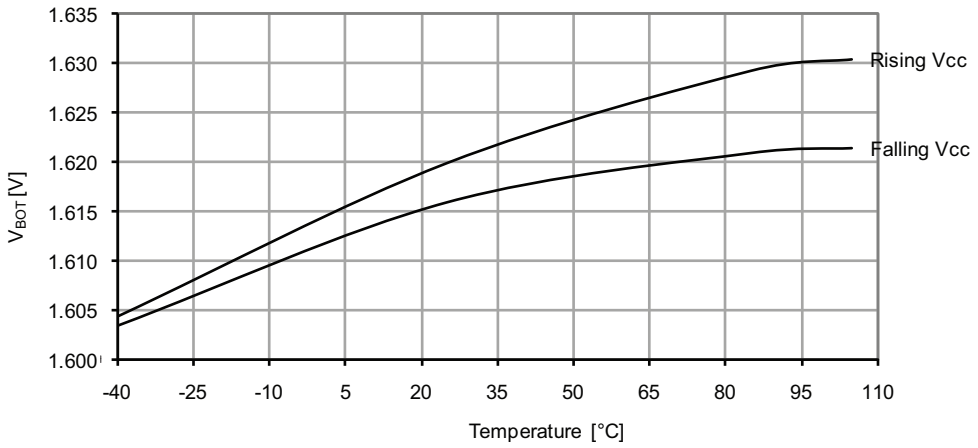


Figure 37-145. BOD thresholds vs. temperature.

BOD level = 3.0V.

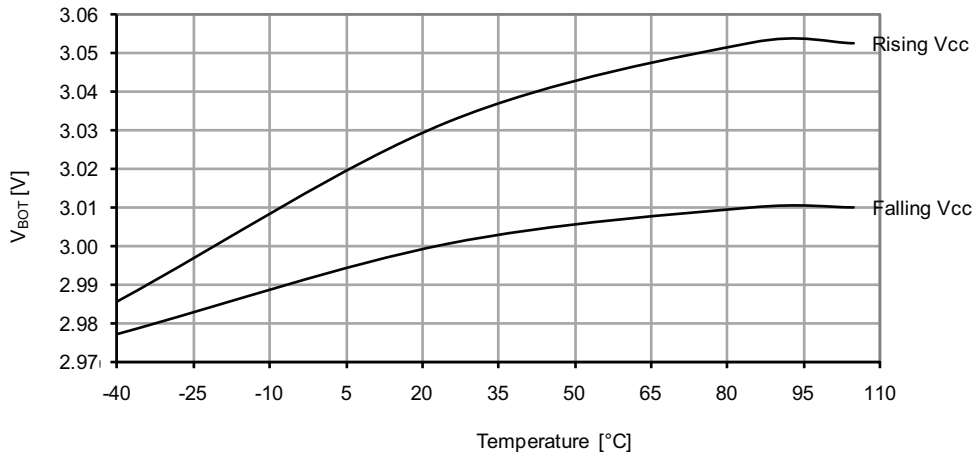
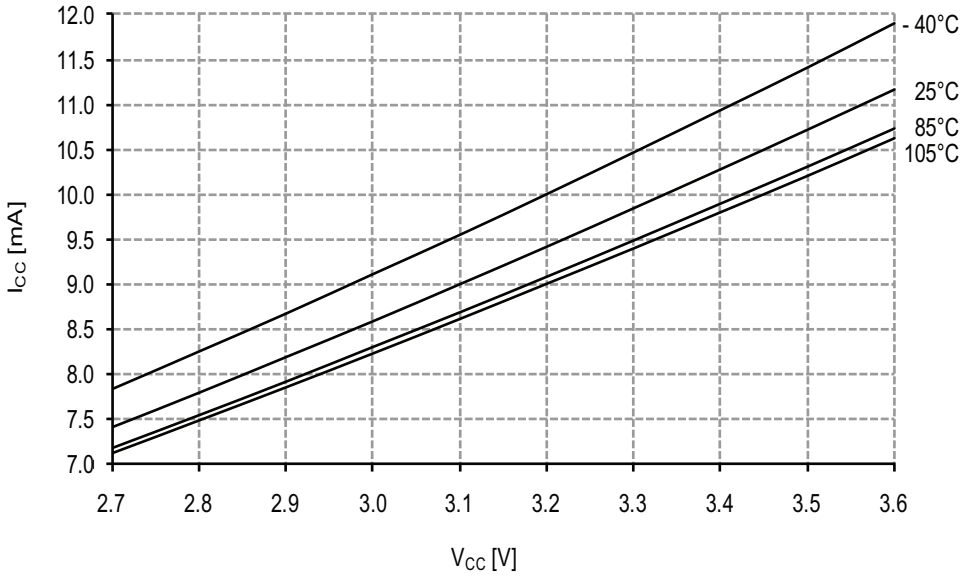


Figure 37-175. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator.



37.3.1.2 Idle mode supply current

Figure 37-176. Idle mode supply current vs. frequency.

f_{SYS} = 0 - 1MHz external clock, T = 25°C.

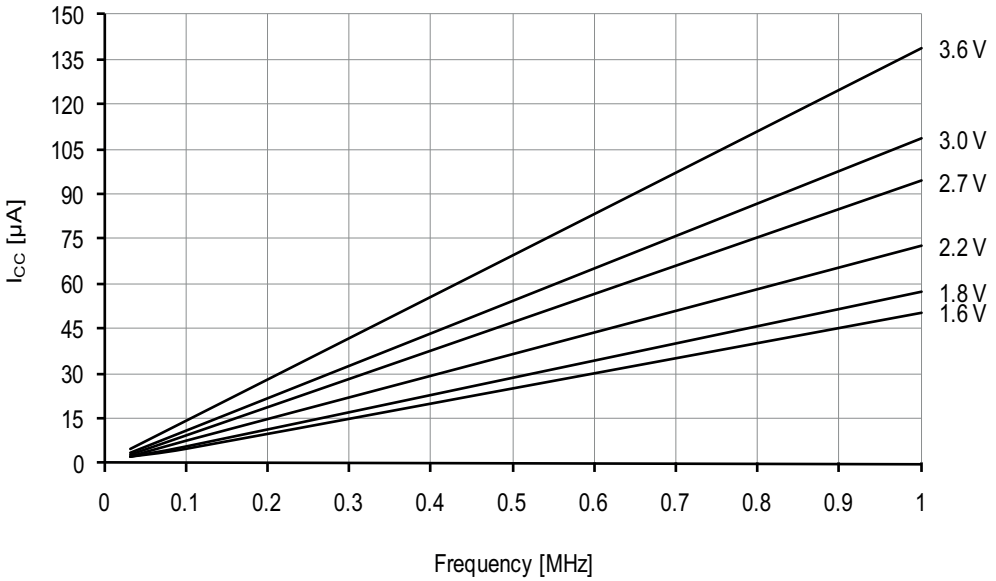


Figure 37-179. Idle mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

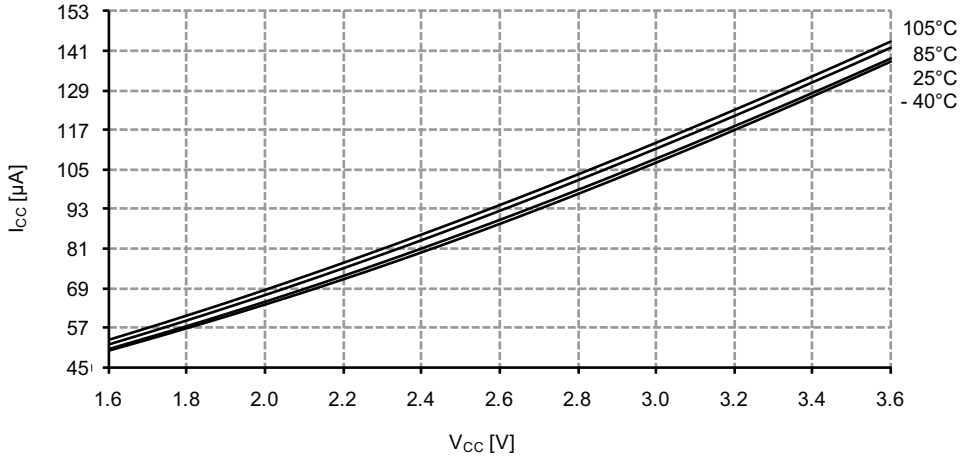
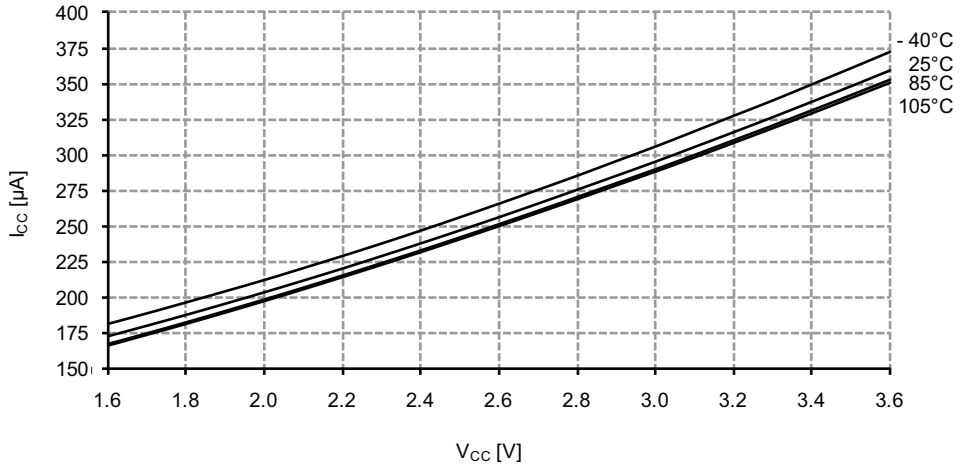


Figure 37-180. Idle mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.



37.3.1.5 Standby mode supply current

Figure 37-187. Standby supply current vs. V_{CC}.

Standby, f_{SYS} = 1MHz.

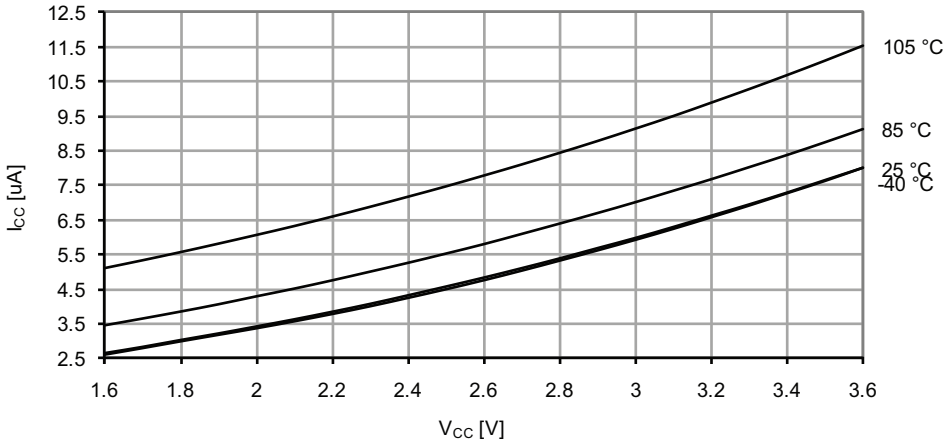


Figure 37-188. Standby supply current vs. V_{CC}.

25°C, running from different crystal oscillators.

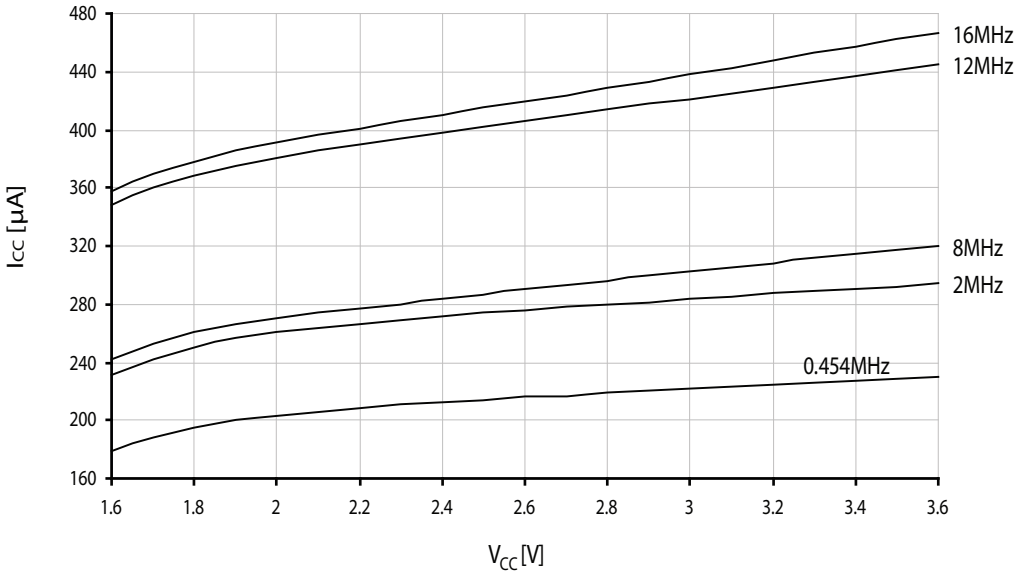
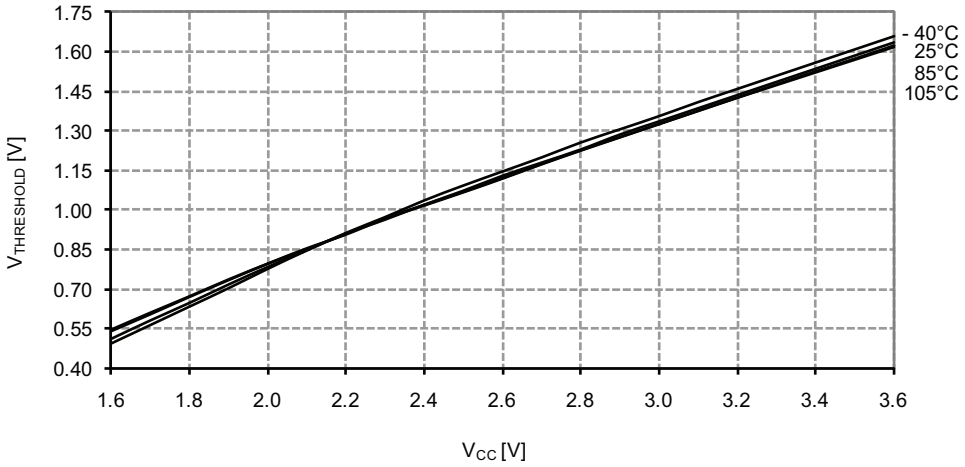


Figure 37-235. Reset pin input threshold voltage vs. V_{CC}.

V_{IL} - Reset pin read as "0".



37.3.9 Power-on Reset Characteristics

Figure 37-236. Power-on reset current consumption vs. V_{CC}.

BOD level = 3.0V, enabled in continuous mode.

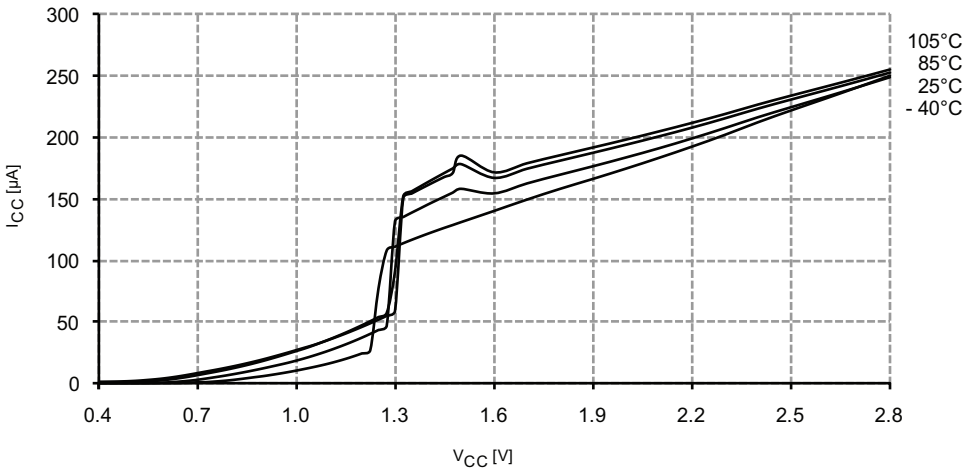


Figure 37-263. Idle mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock

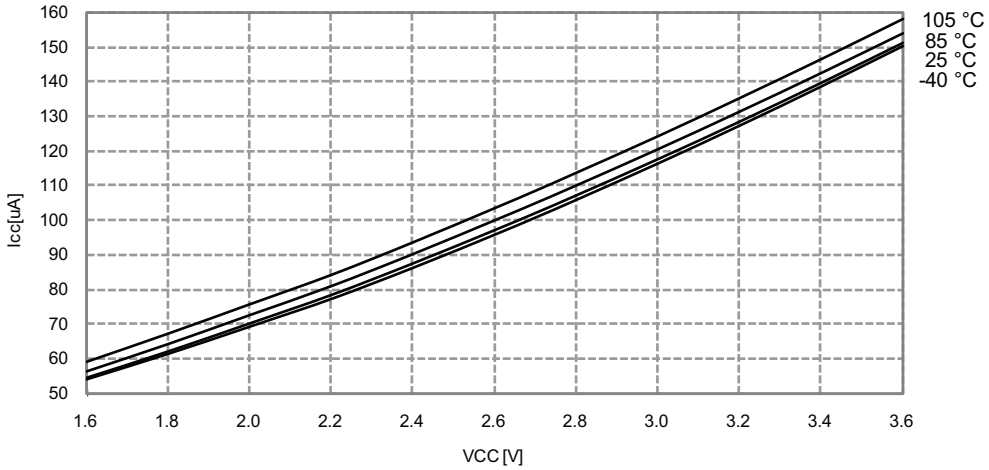


Figure 37-264. Idle mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator

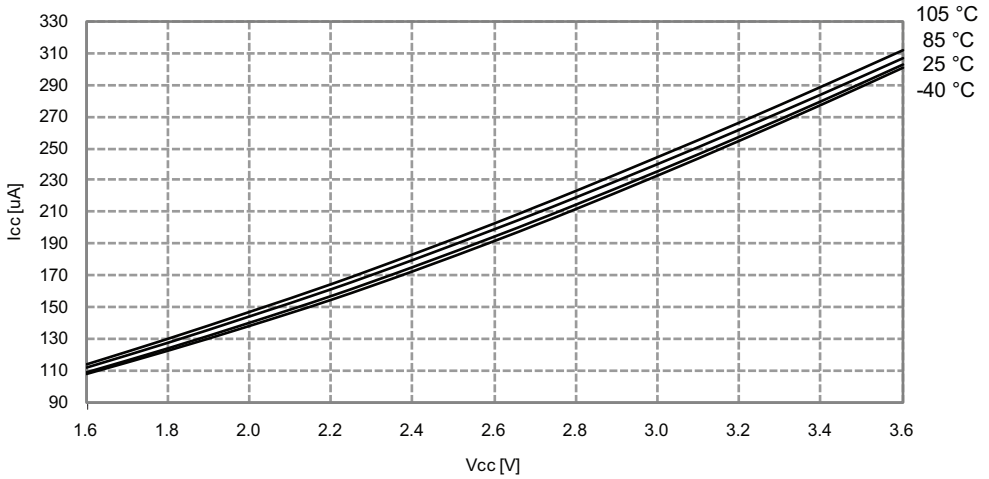
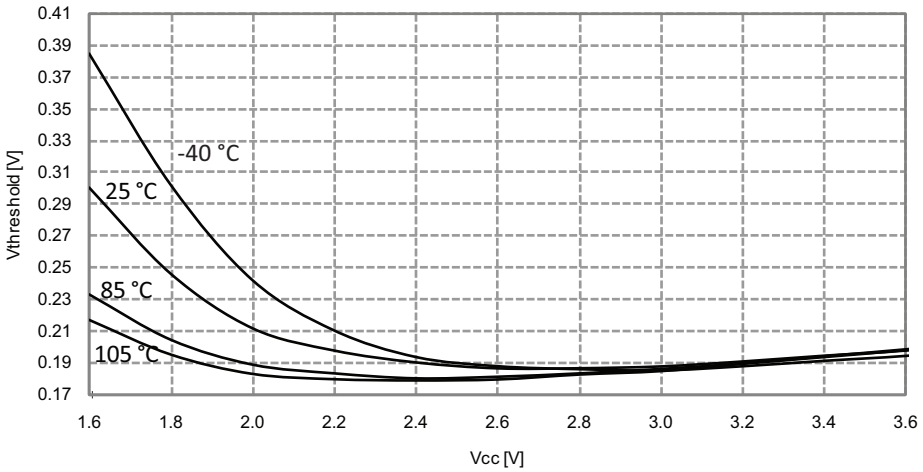


Figure 37-287. I/O pin input hysteresis vs. V_{CC}



37.4.3 ADC Characteristics

Figure 37-288. INL error vs. external V_{REF}

T = 25°C, V_{CC} = 3.6V, external reference

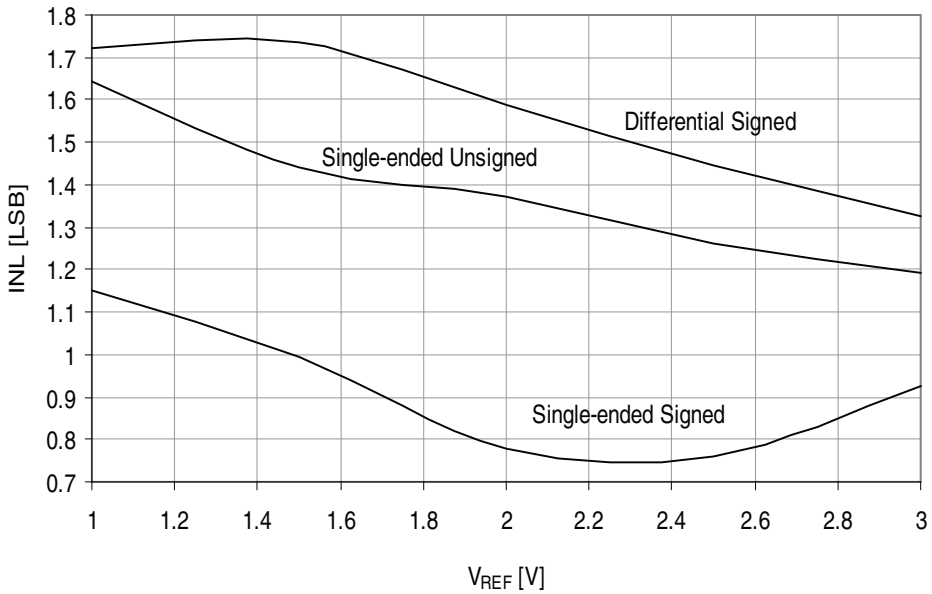


Figure 37-307. Analog comparator hysteresis vs. V_{CC}.

Low power, large hysteresis

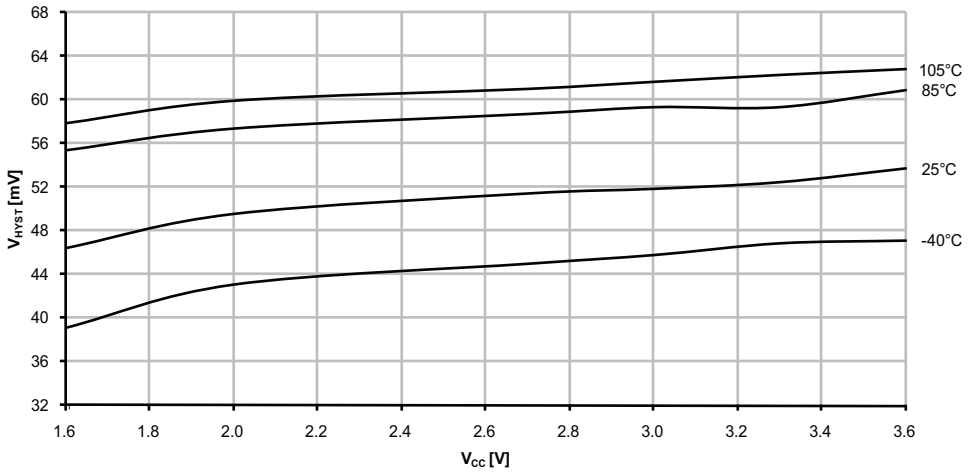


Figure 37-308. Analog comparator current source vs. calibration value.

Temperature = 25°C