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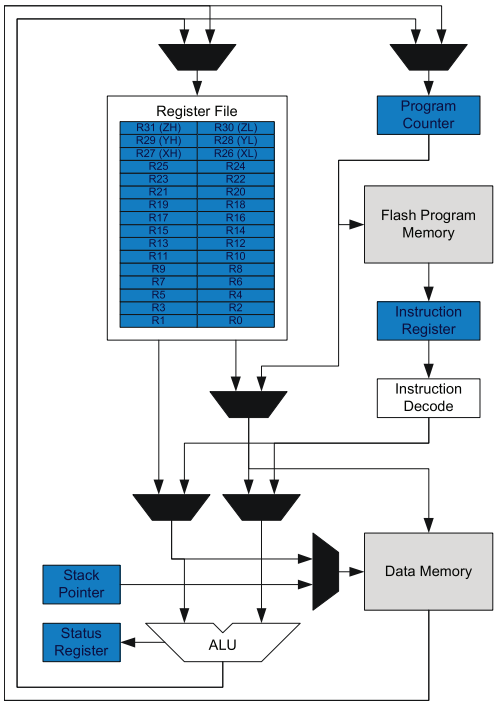
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32a4u-an

Figure 6-1. Block diagram of the AVR CPU architecture.



The arithmetic logic unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single-register operations can also be executed in the ALU. After an arithmetic operation, the status register is updated to reflect information about the result of the operation.

The ALU is directly connected to the fast-access register file. The 32 x 8-bit general purpose working registers all have single clock cycle access time allowing single-cycle arithmetic logic unit (ALU) operation between registers or between a register and an immediate. Six of the 32 registers can be used as three 16-bit address pointers for program and data space addressing, enabling efficient address calculations.

The memory spaces are linear. The data memory space and the program memory space are two different memory spaces.

The data memory space is divided into I/O registers, SRAM, and external RAM. In addition, the EEPROM can be memory mapped in the data memory.

All I/O status and control registers reside in the lowest 4KB addresses of the data memory. This is referred to as the I/O memory space. The lowest 64 addresses can be accessed directly, or as the data space locations from 0x00 to 0x3F. The rest is the extended I/O memory space, ranging from 0x0040 to 0x0FFF. I/O registers here must be accessed as data space locations using load (LD/LDS/LDD) and store (ST/STS/STD) instructions.

The SRAM holds data. Code execution from SRAM is not supported. It can easily be accessed through the five different addressing modes supported in the AVR architecture. The first SRAM address is 0x2000.

Data addresses 0x1000 to 0x1FFF are reserved for memory mapping of EEPROM.

The program memory is divided in two sections, the application program section and the boot program section. Both sections have dedicated lock bits for write and read/write protection. The SPM instruction that is used for self-programming of the application flash memory must reside in the boot program section. The application section contains an application table section with separate lock bits for write and read/write protection. The application table section can be used for safe storing of nonvolatile data in the program memory.

6.4 ALU - Arithmetic Logic Unit

The arithmetic logic unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single-register operations can also be executed. The ALU operates in direct connection with all 32 general

7.3 Flash Program Memory

The Atmel AVR XMEGA devices contain on-chip, in-system reprogrammable flash memory for program storage. The flash memory can be accessed for read and write from an external programmer through the PDI or from application software running in the device.

All AVR CPU instructions are 16 or 32 bits wide, and each flash location is 16 bits wide. The flash memory is organized in two main sections, the application section and the boot loader section. The sizes of the different sections are fixed, but device-dependent. These two sections have separate lock bits, and can have different levels of protection. The store program memory (SPM) instruction, which is used to write to the flash from the application software, will only operate when executed from the boot loader section.

The application section contains an application table section with separate lock settings. This enables safe storage of nonvolatile data in the program memory.

Table 7-1. Flash Program Memory (Hexadecimal address).

Word Address				
ATxmega128A4U	ATxmega64A4U	ATxmega32A4U	ATxmega16A4U	
0	0	0	0	Application Section (128K/64K/32K/16K)
				...
EFFF /	77FF /	37FF /	17FF	
F000 /	7800 /	3800 /	1800	Application Table Section (8K/4K/4K/4K)
FFFF /	7FFF /	3FFF /	1FFF	
10000 /	8000 /	4000 /	2000	Boot Section (8K/4K/4K/4K)
10FFF /	87FF /	47FF /	27FF	

7.3.1 Application Section

The Application section is the section of the flash that is used for storing the executable application code. The protection level for the application section can be selected by the boot lock bits for this section. The application section can not store any boot loader code since the SPM instruction cannot be executed from the application section.

7.3.2 Application Table Section

The application table section is a part of the application section of the flash memory that can be used for storing data. The size is identical to the boot loader section. The protection level for the application table section can be selected by the boot lock bits for this section. The possibilities for different protection levels on the application section and the application table section enable safe parameter storage in the program memory. If this section is not used for data, application code can reside here.

7.3.3 Boot Loader Section

While the application section is used for storing the application code, the boot loader software must be located in the boot loader section because the SPM instruction can only initiate programming when executing from this section. The SPM instruction can access the entire flash, including the boot loader section itself. The protection level for the boot loader section can be selected by the boot loader lock bits. If this section is not used for boot loader software, application code can be stored here.

19. Hi-Res – High Resolution Extension

19.1 Features

- Increases waveform generator resolution up to 8x (three bits)
- Supports frequency, single-slope PWM, and dual-slope PWM generation
- Supports the AWeX when this is used for the same timer/counter

19.2 Overview

The high-resolution (hi-res) extension can be used to increase the resolution of the waveform generation output from a timer/counter by four or eight. It can be used for a timer/counter doing frequency, single-slope PWM, or dual-slope PWM generation. It can also be used with the AWeX if this is used for the same timer/counter.

The hi-res extension uses the peripheral 4x clock (Clk_{PER4}). The system clock prescalers must be configured so the peripheral 4x clock frequency is four times higher than the peripheral and CPU clock frequency when the hi-res extension is enabled.

There are three hi-res extensions that each can be enabled for each timer/counters pair on PORTC, PORTD and PORTE. The notation of these are HIRESC, HIRESD and HIRESE, respectively.

25. IRCOM – IR Communication Module

25.1 Features

- Pulse modulation/demodulation for infrared communication
- IrDA compatible for baud rates up to 115.2Kbps
- Selectable pulse modulation scheme
  - 3/16 of the baud rate period
  - Fixed pulse period, 8-bit programmable
  - Pulse modulation disabled
- Built-in filtering
- Can be connected to and used by any USART

25.2 Overview

Atmel AVR XMEGA devices contain an infrared communication module (IRCOM) that is IrDA compatible for baud rates up to 115.2Kbps. It can be connected to any USART to enable infrared pulse encoding/decoding for that USART.

36.1.14.5 Internal Phase Locked Loop (PLL) characteristics

Table 36-26. Internal PLL characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency (1)	V_{CC}= 1.6 - 1.8V	20		48	MHz
		V_{CC}= 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		µs

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

36.1.14.6 External clock characteristics

Figure 36-3. External clock drive waveform

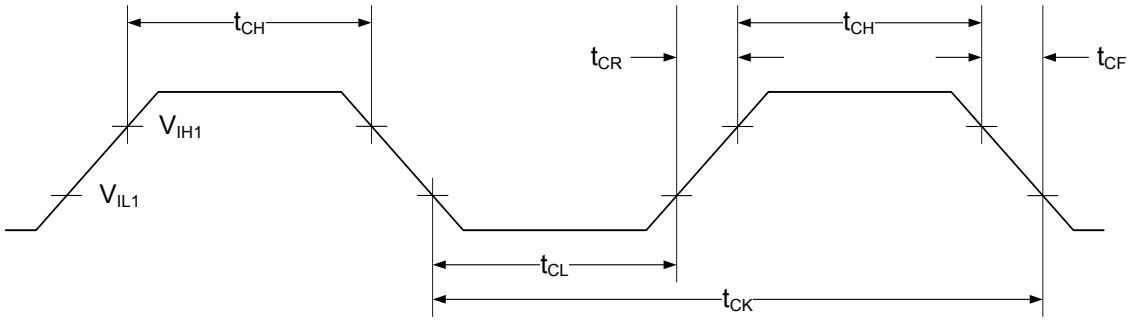


Table 36-27. External clock used as system clock without prescaling.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (1)	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

36.3 ATxmega64A4U

36.3.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 36-65 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 36-65. Absolute maximum ratings.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4.0	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	mA
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC}+0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	°C

36.3.2 General Operating Ratings

The device must operate within the ratings listed in Table 36-66 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 36-66. General operating conditions.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	V
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	°C

Table 36-67. Operating voltage and frequency.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 36-15 the Frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Table 36-69. Current consumption for modules and peripherals.

Symbol	Parameter	Condition [1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				1.0		µA
	32.768kHz int. oscillator				29		µA
	2MHz int. oscillator				85		µA
		DFLL enabled with 32.768kHz int. osc. as reference			120		
	32MHz int. oscillator				300		µA
		DFLL enabled with 32.768kHz int. osc. as reference			465		
	PLL	20x multiplication factor, 32MHz int. osc. DIV4 as reference			320		µA
	Watchdog timer				1.0		µA
	BOD	Continuous mode			138		µA
		Sampled mode, includes ULP oscillator			1.0		
	Internal 1.0V reference				103		µA
	Temperature sensor				100		µA
	ADC	250ksps V_{REF} = Ext ref			3.0		mA
			CURRLIMIT = LOW		2.6		
			CURRLIMIT = MEDIUM		2.1		
			CURRLIMIT = HIGH		1.6		
	DAC	250ksps V_{REF} = Ext ref No load	Normal mode		1.9		mA
			Low power mode		1.1		
	AC	High speed mode			330		µA
		Low pPower mode			130		
	DMA	615KBps between I/O registers and SRAM			108		µA
	Timer/counter				16		µA
	USART	Rx and Tx enabled, 9600 BAUD			2.5		µA
	Flash memory and EEPROM programming				8.0		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Offset error, input referred	1x gain, normal mode			-2		mV
		8x gain, normal mode			-5		
		64x gain, normal mode			-4		
	Noise	1x gain, normal mode	V_{CC} = 3.6V Ext. V_{REF}		0.5		mV rms
		8x gain, normal mode			1.5		
		64x gain, normal mode			11		

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.

36.3.7 DAC Characteristics

Table 36-76. Power supply, reference and output range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	V
AV_{REF}	External reference voltage		1.0		V_{CC}- 0.6	V
$R_{channel}$	DC output impedance				50	Ω
	Linear output voltage range		0.15		AV_{CC}-0.15	V
R_{AREF}	Reference input resistance			>10		MΩ
CAREF	Reference input capacitance	Static load		7		pF
	Minimum resistance load		1.0			kΩ
	Maximum capacitance load				100	pF
		1000Ω serial resistance			1.0	nF
	Output sink/source	Operating within accuracy specification			AV_{CC}/1000	mA
		Safe operation			10	

Table 36-77. Clock and timing.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
f_{DAC}	Conversion rate	C_{load}=100pF, maximum step size	Normal mode	0		1000	ksps
			Low power mode			500	

Figure 37-13. Idle mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

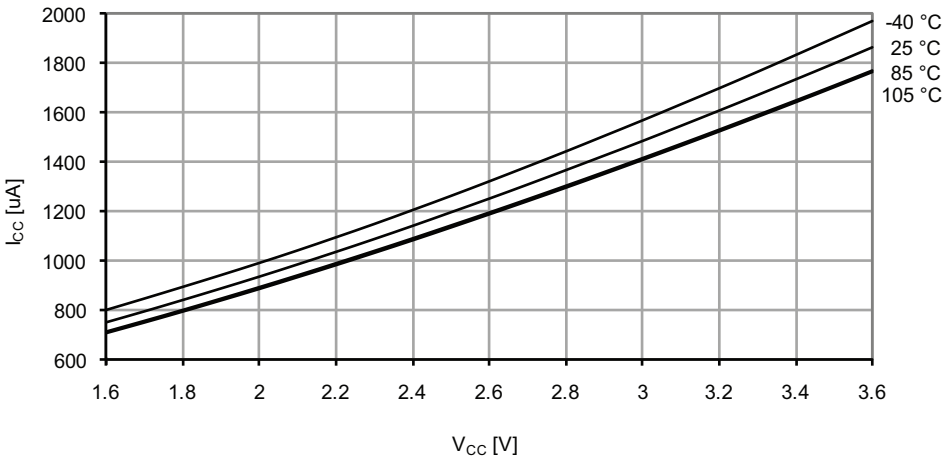


Figure 37-14. Idle mode current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator.

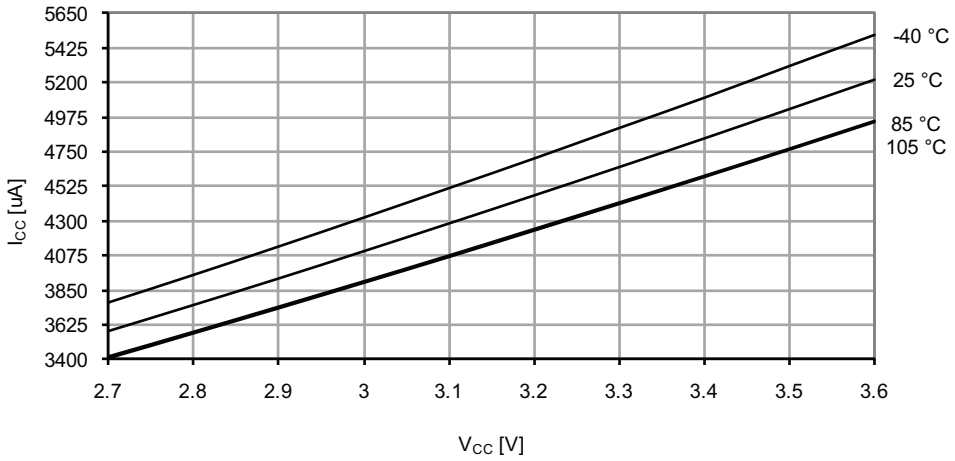
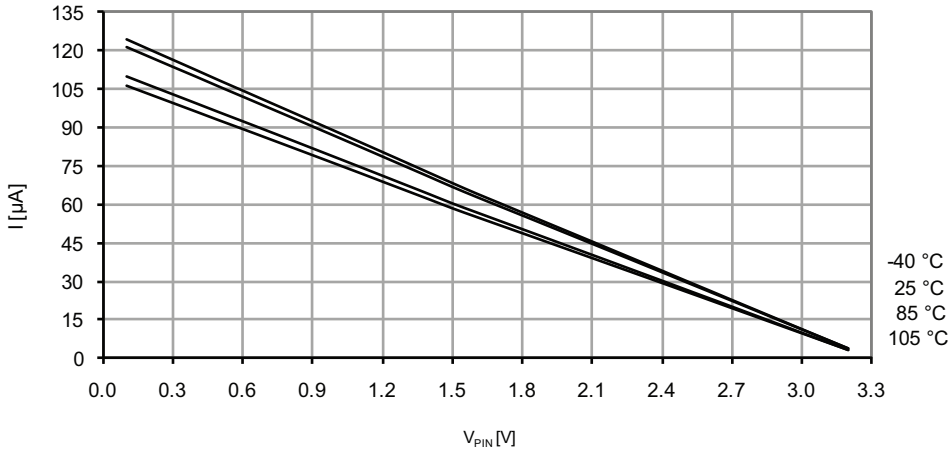


Figure 37-23. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 3.3V.



37.1.2.2 Output Voltage vs. Sink/Source Current

Figure 37-24. I/O pin output voltage vs. source current.

V_{CC} = 1.8V.

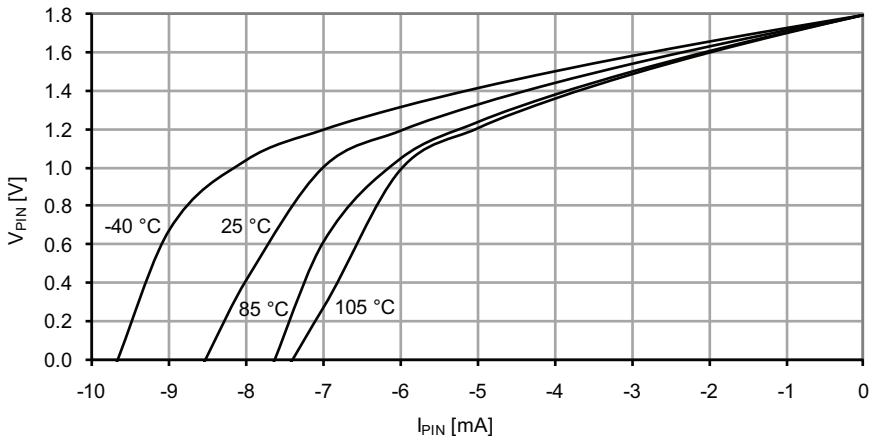


Figure 37-40. DNL error vs. sample rate.

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external.

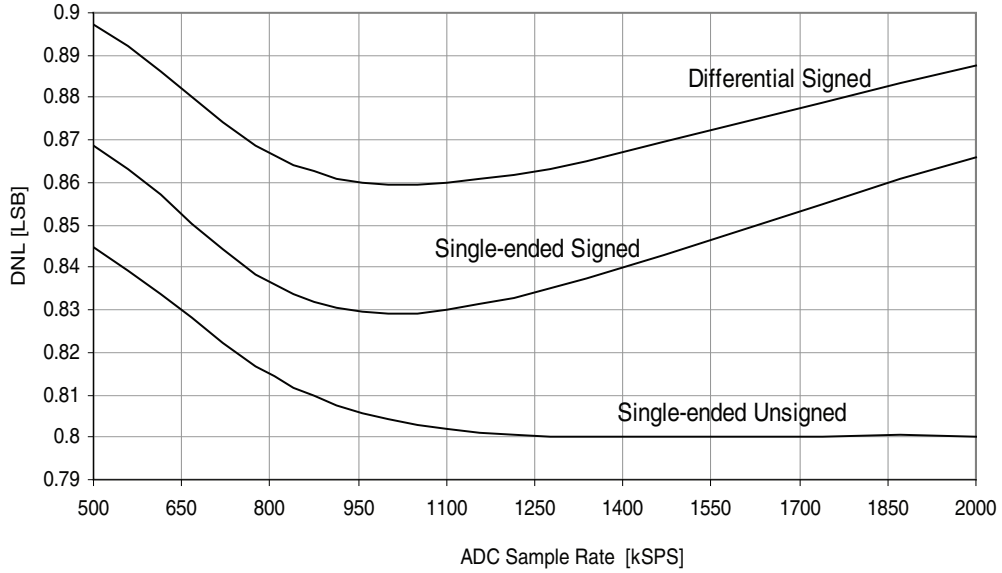


Figure 37-41. DNL error vs. input code.

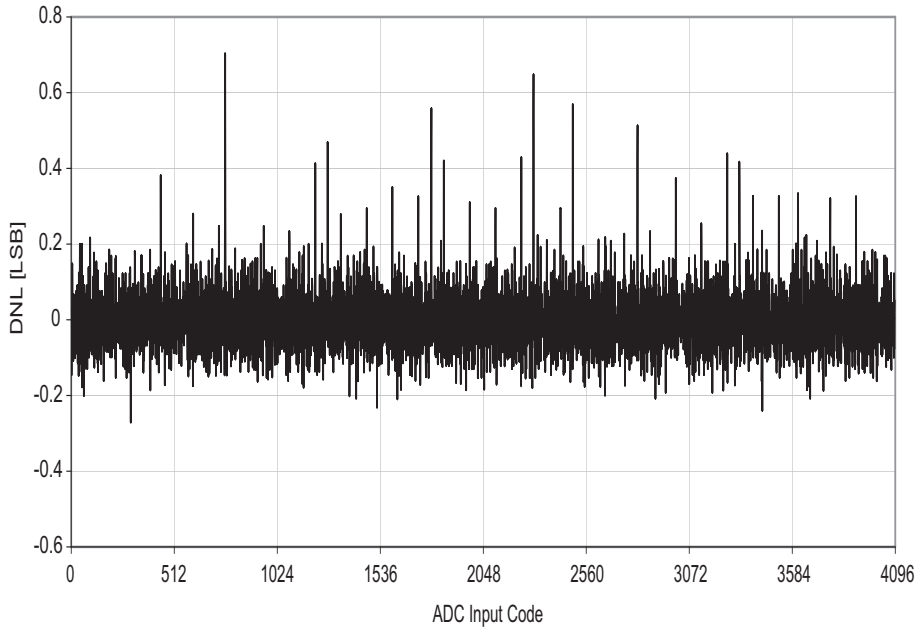


Figure 37-50. DNL error vs. V_{REF}.

V_{CC} = 3.6V.

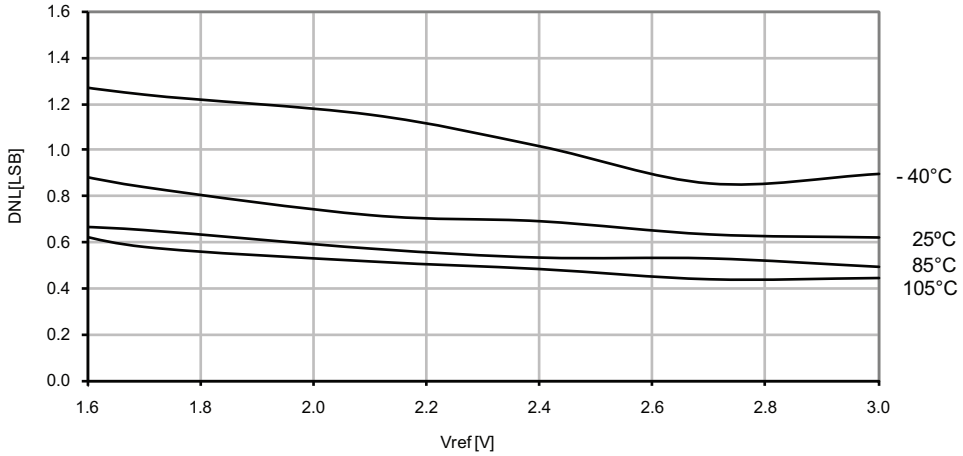
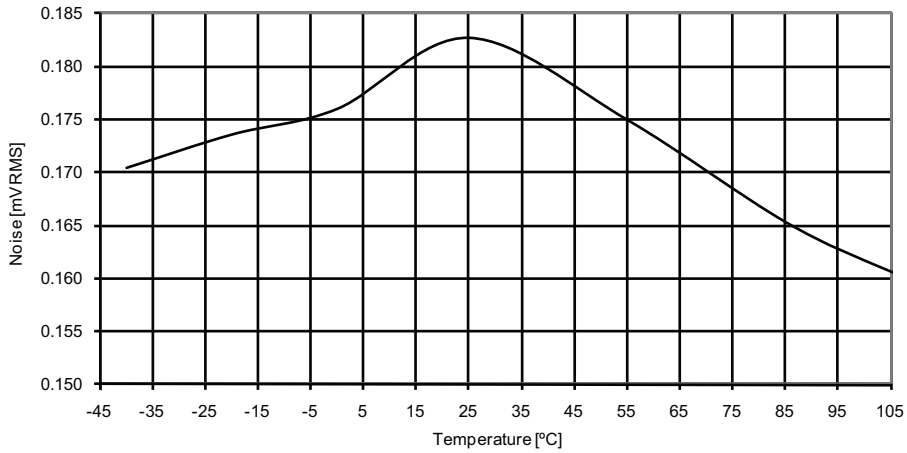


Figure 37-51. DAC noise vs. temperature.

V_{CC} = 3.0V, V_{REF} = 2.4V .



37.1.7 BOD Characteristics

Figure 37-60. BOD thresholds vs. temperature.

BOD level = 1.6V.

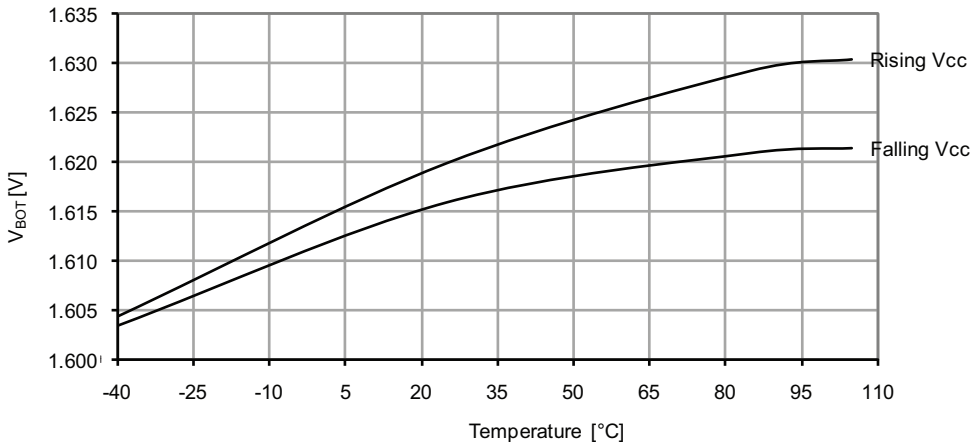
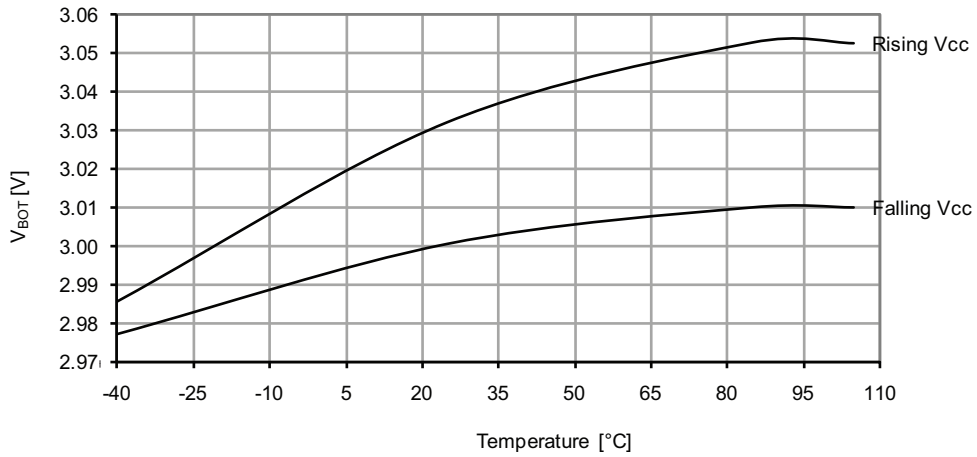


Figure 37-61. BOD thresholds vs. temperature.

BOD level = 3.0V.



37.1.8 External Reset Characteristics

Figure 37-62. Minimum Reset pin pulse width vs. V_{CC}.

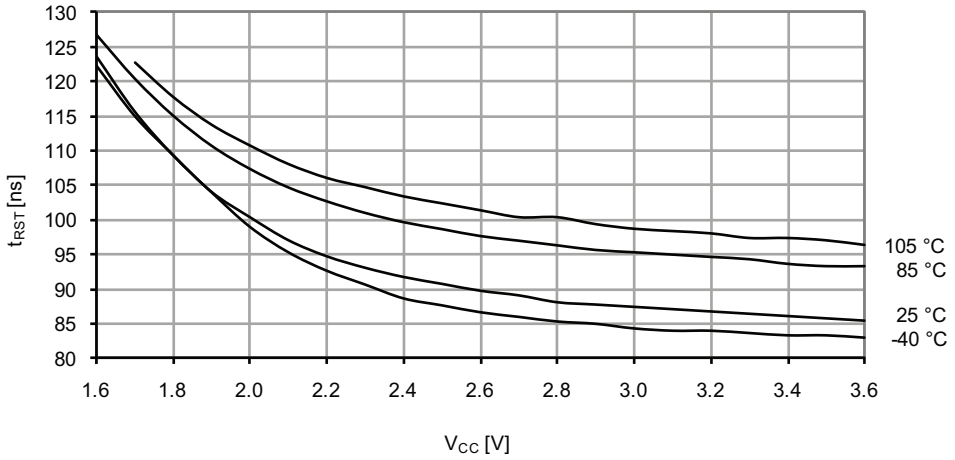


Figure 37-63. Reset pin pull-up resistor current vs. reset pin voltage.
V_{CC} = 1.8V.

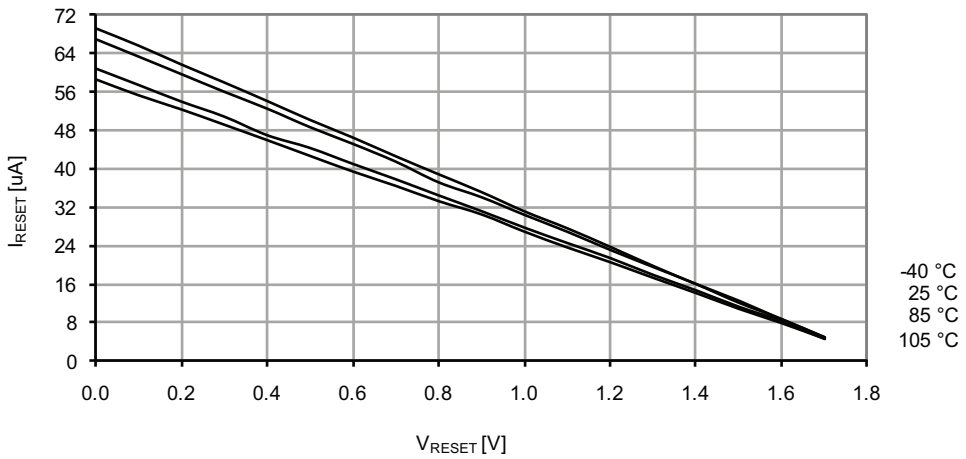


Figure 37-130. Offset error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.

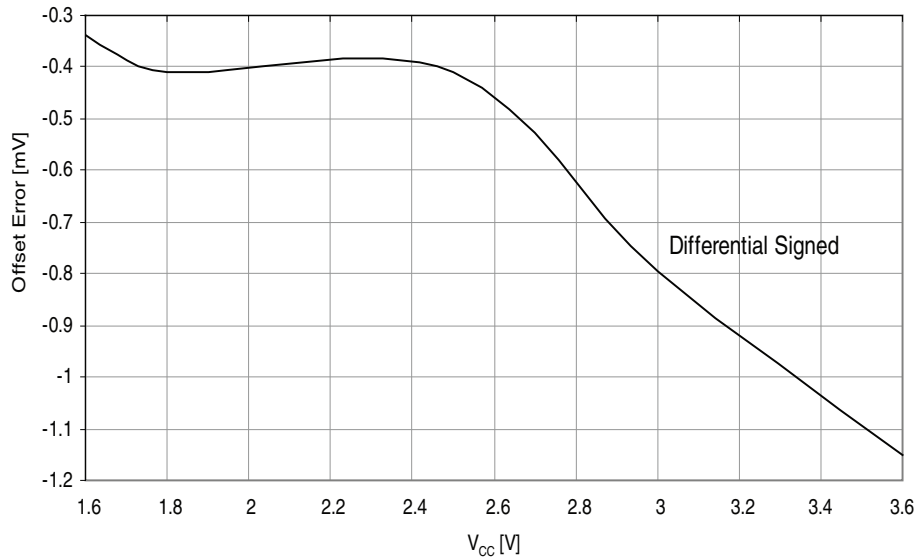
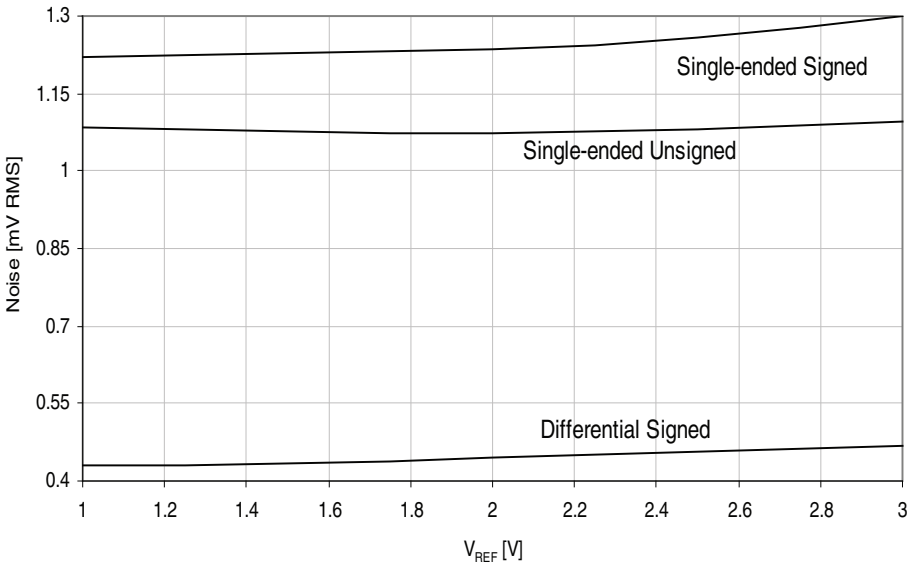


Figure 37-131. Noise vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps.



37.2.5 Analog Comparator Characteristics

Figure 37-136. Analog comparator hysteresis vs. V_{CC}.

High-speed, small hysteresis.

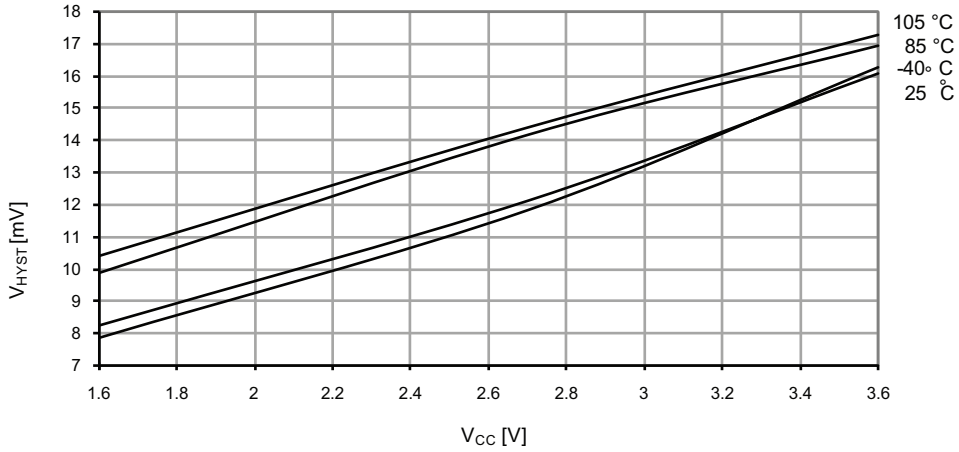


Figure 37-137. Analog comparator hysteresis vs. V_{CC}.

Low power, small hysteresis.

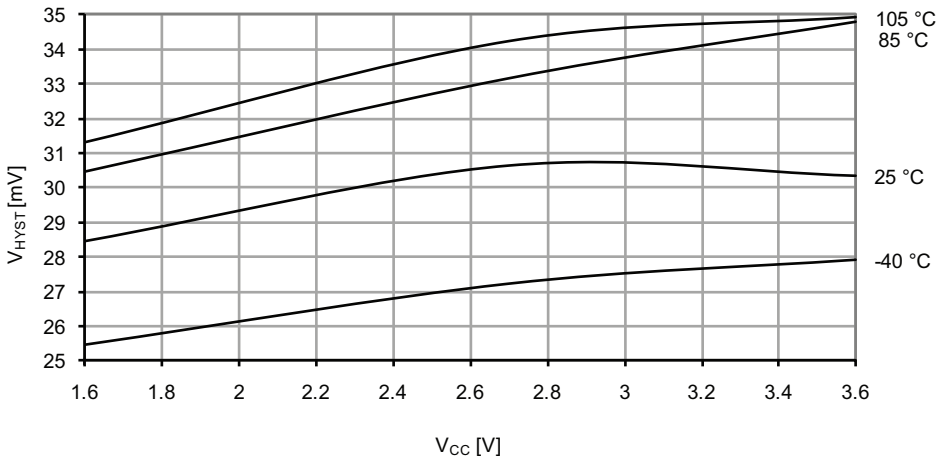
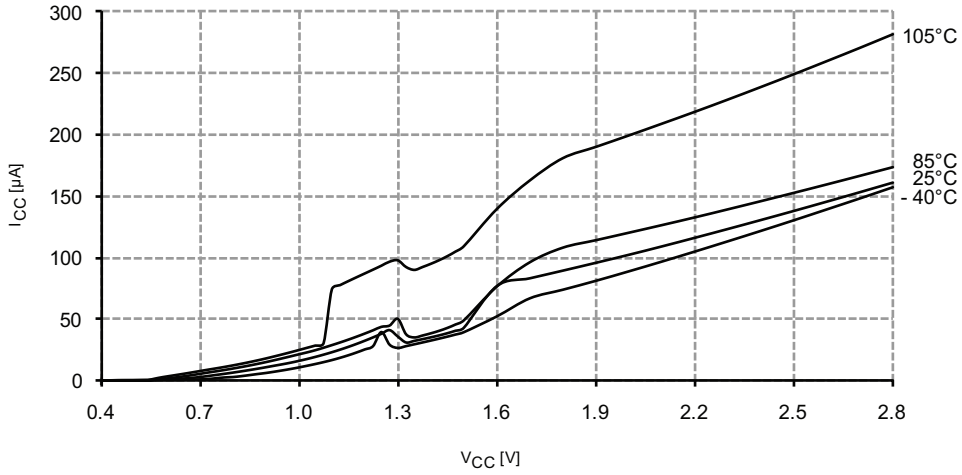


Figure 37-237. Power-on reset current consumption vs. V_{CC}.

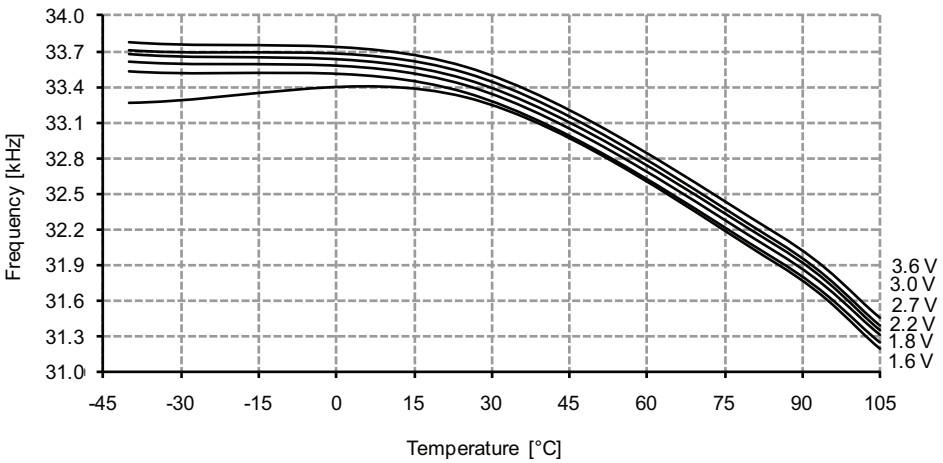
BOD level = 3.0V, enabled in sampled mode.



37.3.10 Oscillator Characteristics

37.3.10.1 Ultra Low-Power internal oscillator

Figure 37-238. Ultra Low-Power internal oscillator frequency vs. temperature.



37.3.10.3 2MHz Internal Oscillator

Figure 37-241. 2MHz internal oscillator frequency vs. temperature.

DFLL disabled.

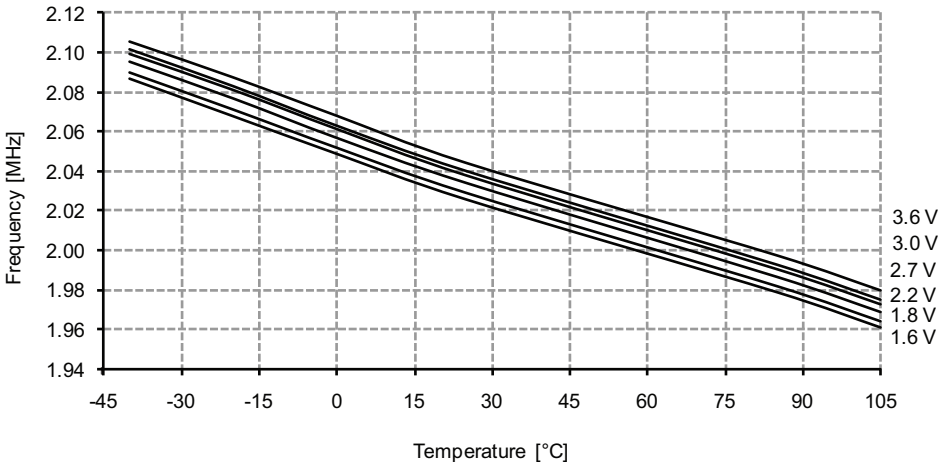


Figure 37-242. 2MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator .

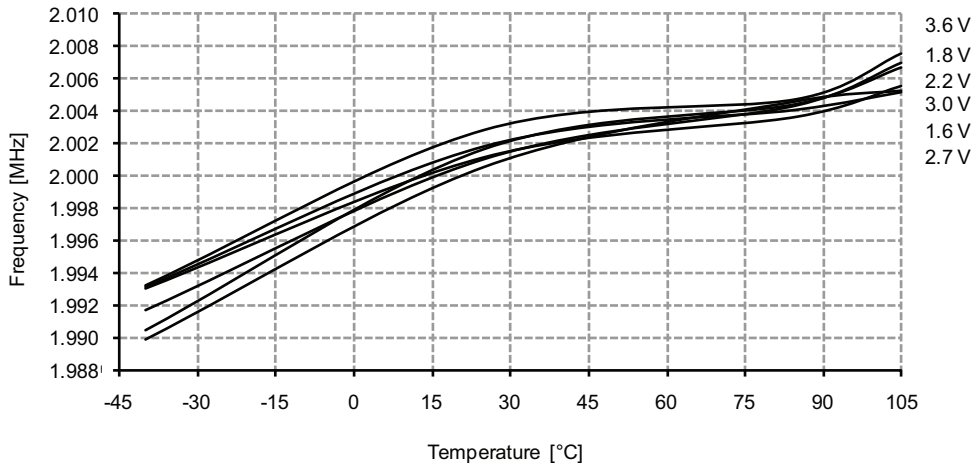


Figure 37-249. 48MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator.

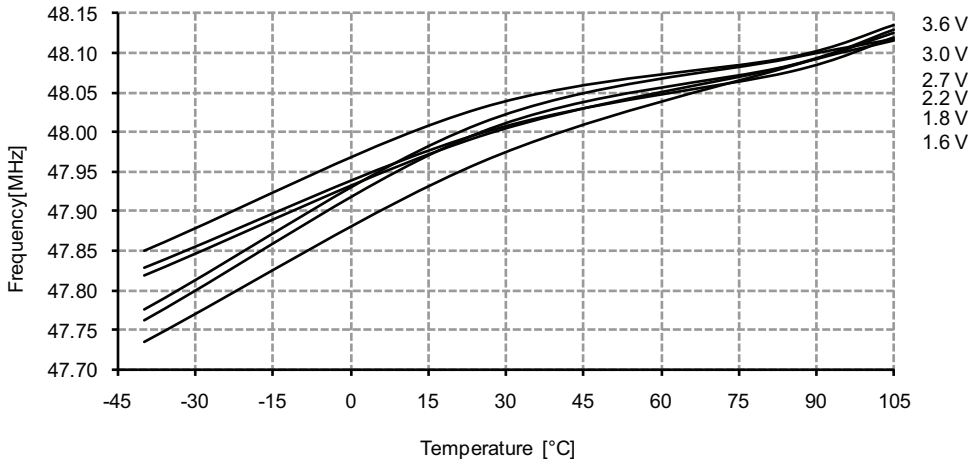


Figure 37-250. 48MHz internal oscillator CALA calibration step size.

V_{CC} = 3.0V

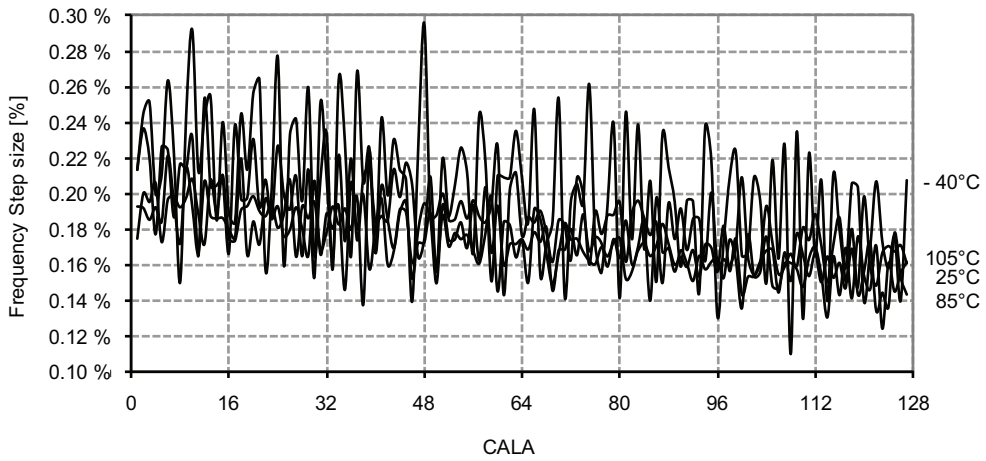


Figure 37-317. Reset pin pull-up resistor current vs. reset pin voltage

V_{CC} = 3.3V

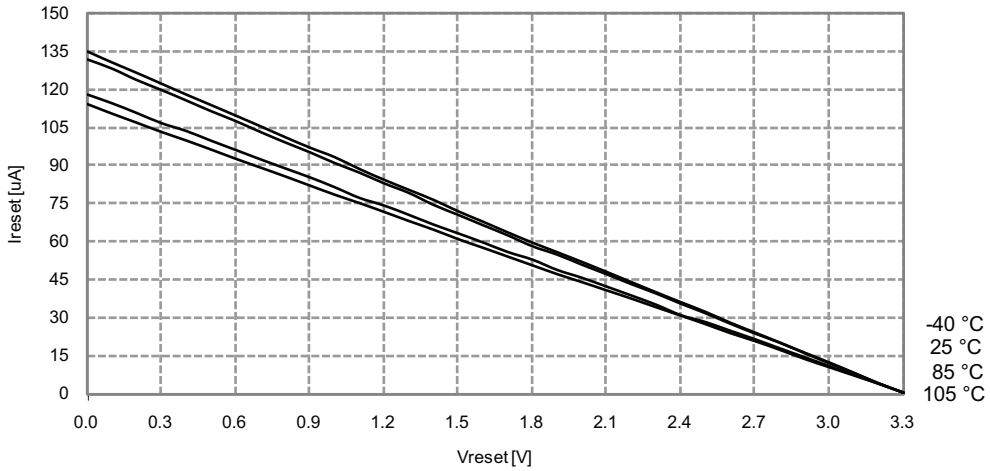


Figure 37-318. Reset pin input threshold voltage vs. V_{CC}

V_{IH} - Reset pin read as "1"