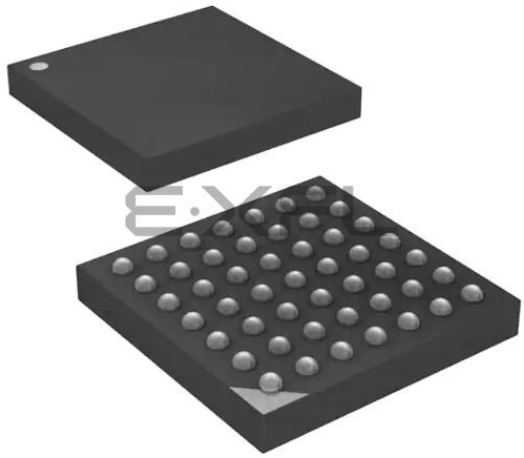

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	49-VFBGA
Supplier Device Package	49-VFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32a4u-cur

During interrupts or subroutine calls, the return address is automatically pushed on the stack. The return address can be two or three bytes, depending on program memory size of the device. For devices with 128KB or less of program memory, the return address is two bytes, and hence the stack pointer is decremented/incremented by two. For devices with more than 128KB of program memory, the return address is three bytes, and hence the SP is decremented/incremented by three. The return address is popped off the stack when returning from interrupts using the RETI instruction, and from subroutine calls using the RET instruction.

The SP is decremented by one when data are pushed on the stack with the PUSH instruction, and incremented by one when data is popped off the stack using the POP instruction.

To prevent corruption when updating the stack pointer from software, a write to SPL will automatically disable interrupts for up to four instructions or until the next I/O memory write.

After reset the stack pointer is initialized to the highest address of the SRAM. See Figure 7-1 on page 16.

6.8 Register File

The register file consists of 32 x 8-bit general purpose working registers with single clock cycle access time. The register file supports the following input/output schemes:

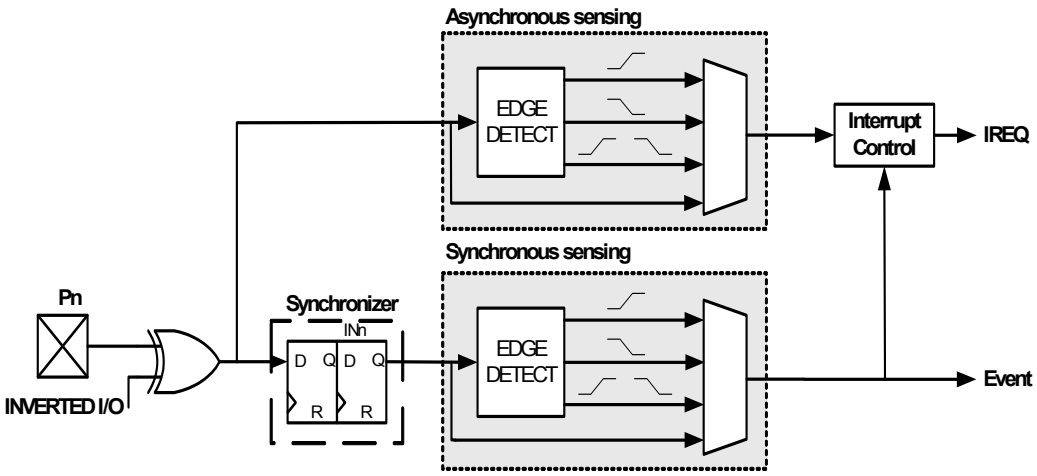
- One 8-bit output operand and one 8-bit result input
- Two 8-bit output operands and one 8-bit result input
- Two 8-bit output operands and one 16-bit result input
- One 16-bit output operand and one 16-bit result input

Six of the 32 registers can be used as three 16-bit address register pointers for data space addressing, enabling efficient address calculations. One of these address pointers can also be used as an address pointer for lookup tables in flash program memory.

15.4 Input sensing

Input sensing is synchronous or asynchronous depending on the enabled clock for the ports, and the configuration is shown in Figure 15-7.

Figure 15-7. Input sensing system overview.

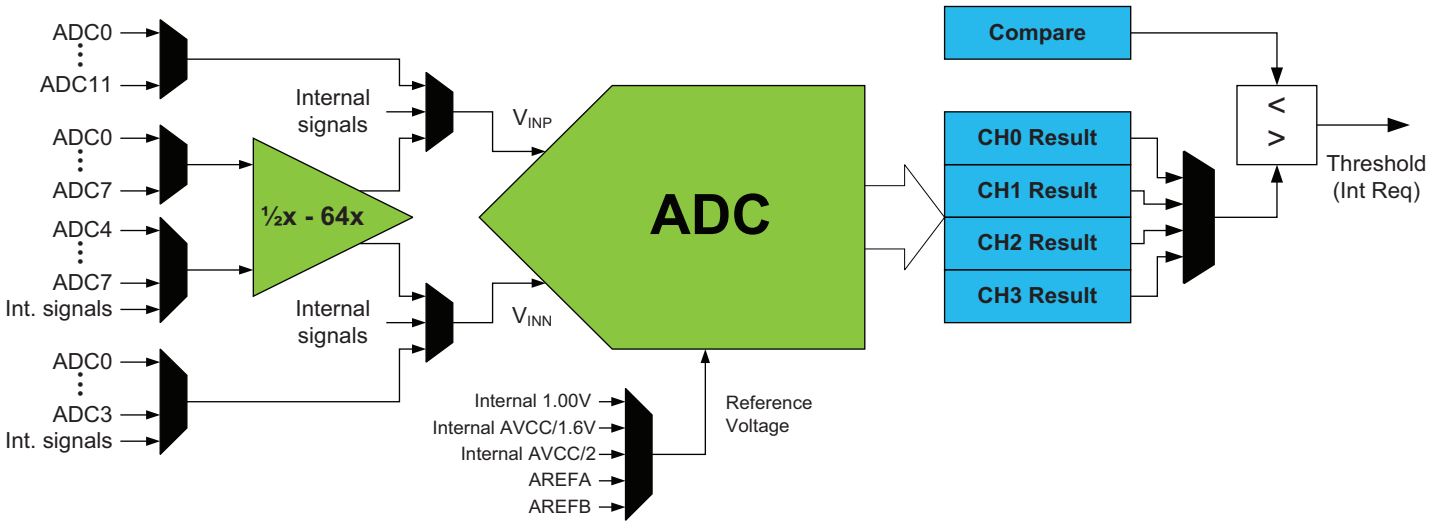


When a pin is configured with inverted I/O, the pin value is inverted before the input sensing.

15.5 Alternate Port Functions

Most port pins have alternate pin functions in addition to being a general purpose I/O pin. When an alternate function is enabled, it might override the normal port pin function or pin value. This happens when other peripherals that require pins are enabled or configured to use pins. If and how a peripheral will override and use pins is described in the section for that peripheral. “Pinout and Pin Functions” on page 55 shows which modules on peripherals that enable alternate functions on a pin, and which alternate functions that are available on a pin.

Figure 28-1. ADC overview.



Two inputs can be sampled simultaneously as both the ADC and the gain stage include sample and hold circuits, and the gain stage has 1x gain setting. Four inputs can be sampled within 1.5µs without any intervention by the application.

The ADC may be configured for 8- or 12-bit result, reducing the minimum conversion time (propagation delay) from 3.5µs for 12-bit to 2.5µs for 8-bit result.

ADC conversion results are provided left- or right adjusted with optional ‘1’ or ‘0’ padding. This eases calculation when the result is represented as a signed integer (signed 16-bit number).

PORTA has one ADC. Notation of this peripheral is ADCA.

36. Electrical Characteristics

All typical values are measured at T = 25°C unless other temperature condition is given. All minimum and maximum values are valid across operating temperature and voltage unless other conditions are given.

36.1 ATxmega16A4U

36.1.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 36-1 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 36-1. Absolute maximum ratings.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	mA
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC}+0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	°C

36.1.2 General Operating Ratings

The device must operate within the ratings listed in Table 36-2 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 36-2. General operating conditions.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	V
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	°C

36.1.8 Analog Comparator Characteristics

Table 36-15. Analog Comparator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage			<±10		mV
I_{lk}	Input leakage current			<1.0		nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			100		µs
V_{hys1}	Hysteresis, none			0		mV
V_{hys2}	Hysteresis, small	mode = High Speed (HS)		13		mV
		mode = Low Power (LP)		30		
V_{hys3}	Hysteresis, large	mode = HS		30		mV
		mode = LP		60		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T= 85°C mode = HS		30	90	ns
		mode = HS		30		
		V_{CC} = 3.0V, T= 85°C mode = LP		130	500	
		mode = LP		130		
	64-level voltage scaler	Integral non-linearity (INL)		0.3	0.5	lsb

36.1.9 Bandgap and Internal 1.0V Reference Characteristics

Table 36-16. Bandgap and Internal 1.0V reference characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC or DAC	1 Clk_{PER} + 2.5µs			µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T= 85°C, after calibration	0.99	1.0	1.01	V
	Variation over voltage and temperature	Relative to T= 85°C, V_{CC} = 3.0V		±1.5		%

36.4 ATxmega128A4U

36.4.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 36-97 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 36-97. Absolute maximum ratings.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	mA
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC}+0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	°C

36.4.2 General Operating Ratings

The device must operate within the ratings listed in Table 36-98 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 36-98. General operating conditions.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	V
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	°C

Table 36-99. Operating voltage and frequency.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 36-22 the Frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Table 36-127. SPI timing characteristics and requirements.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{SCK}	SCK Period	Master		(See Table 21-4 in XMEGA AU Manual)		ns
t_{SCKW}	SCK high/low width	Master		0.5×SCK		
t_{SCKR}	SCK Rise time	Master		2.7		
t_{SCKF}	SCK Fall time	Master		2.7		
t_{MIS}	MISO setup to SCK	Master		10		
t_{MIH}	MISO hold after SCK	Master		10		
t_{MOS}	MOSI setup SCK	Master		0.5×SCK		
t_{MOH}	MOSI hold after SCK	Master		1		
t_{SSCK}	Slave SCK Period	Slave	4×t Clk_{PER}			
t_{SSCKW}	SCK high/low width	Slave	2×t Clk_{PER}			
t_{SSCKR}	SCK Rise time	Slave			1600	
t_{SSCKF}	SCK Fall time	Slave			1600	
t_{SIS}	MOSI setup to SCK	Slave	3			
t_{SIH}	MOSI hold after SCK	Slave	t Clk_{PER}			
t_{SSS}	$\overline{SS}$ setup to SCK	Slave	21			
t_{SSH}	$\overline{SS}$ hold after SCK	Slave	20			
t_{SOS}	MISO setup SCK	Slave		8		
t_{SOH}	MISO hold after SCK	Slave		13		
t_{SOSS}	MISO setup after $\overline{SS}$ low	Slave		11		
t_{SOSH}	MISO hold after $\overline{SS}$ high	Slave		8		

Figure 37-11. Idle mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

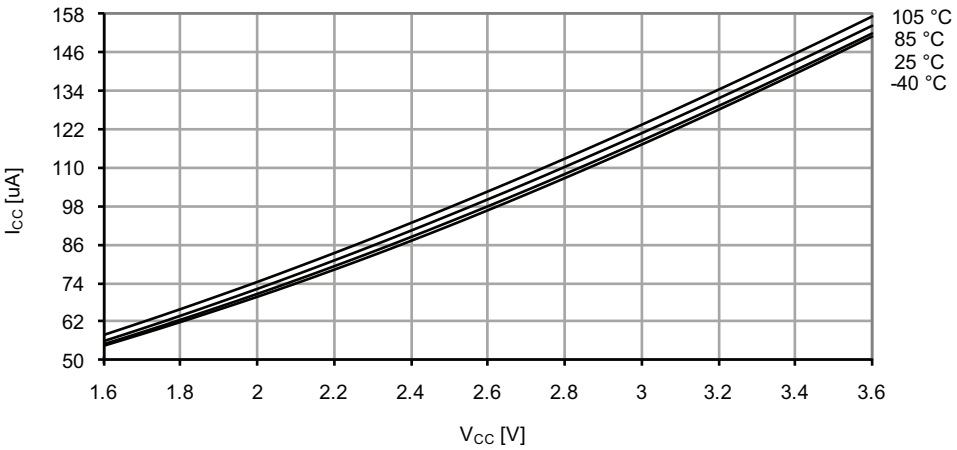
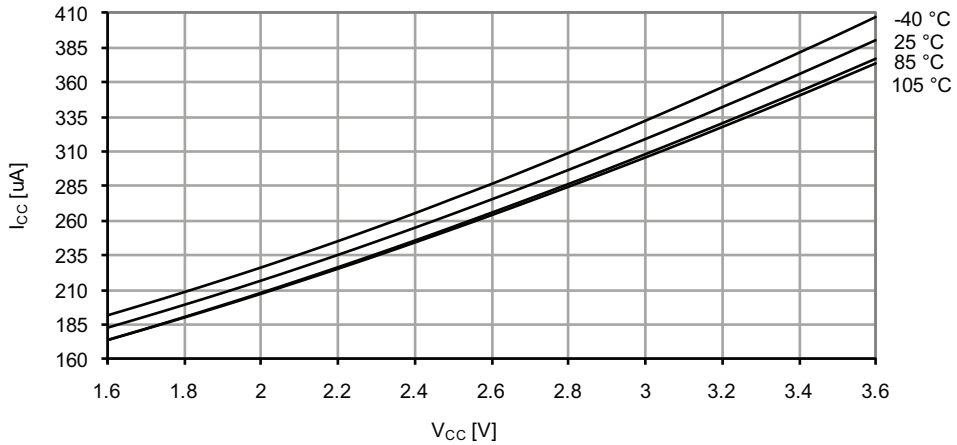


Figure 37-12. Idle mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.



37.1.2 I/O Pin Characteristics

37.1.2.1 Pull-up

Figure 37-21. I/O pin pull-up resistor current vs. input voltage.
V_{CC} = 1.8V.

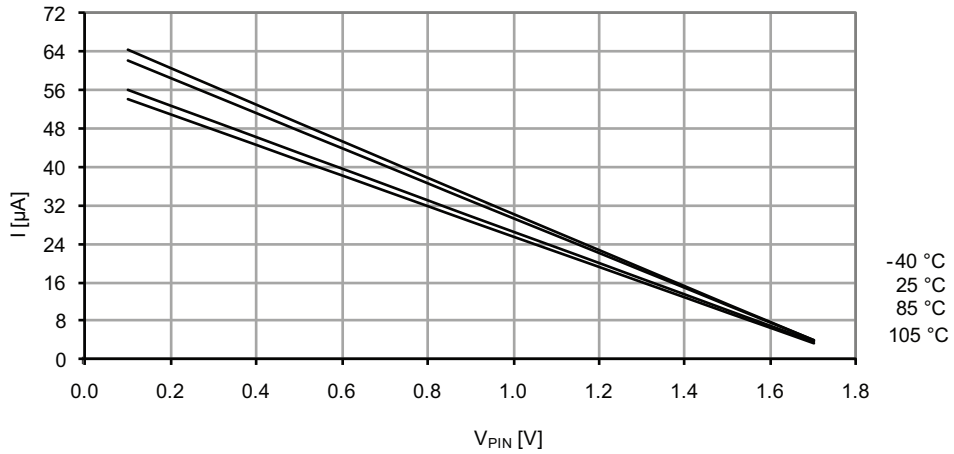


Figure 37-22. I/O pin pull-up resistor current vs. input voltage.
V_{CC} = 3.0V.

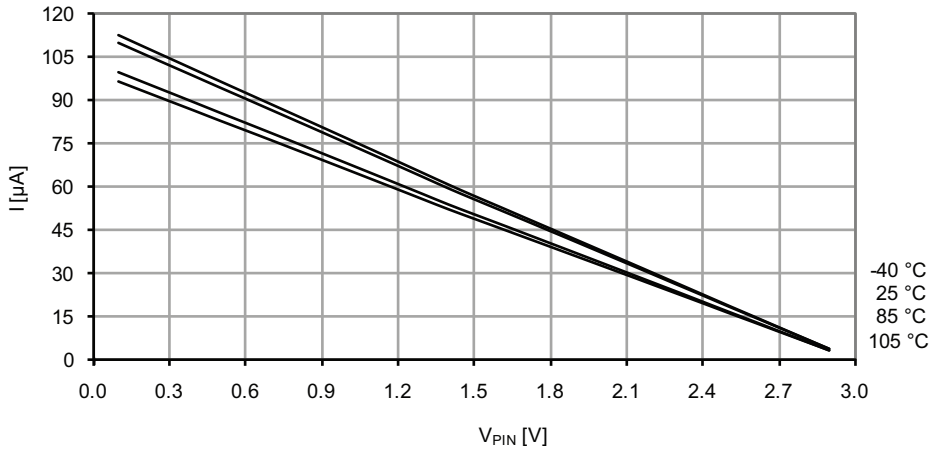


Figure 37-111. I/O pin output voltage vs. source current.

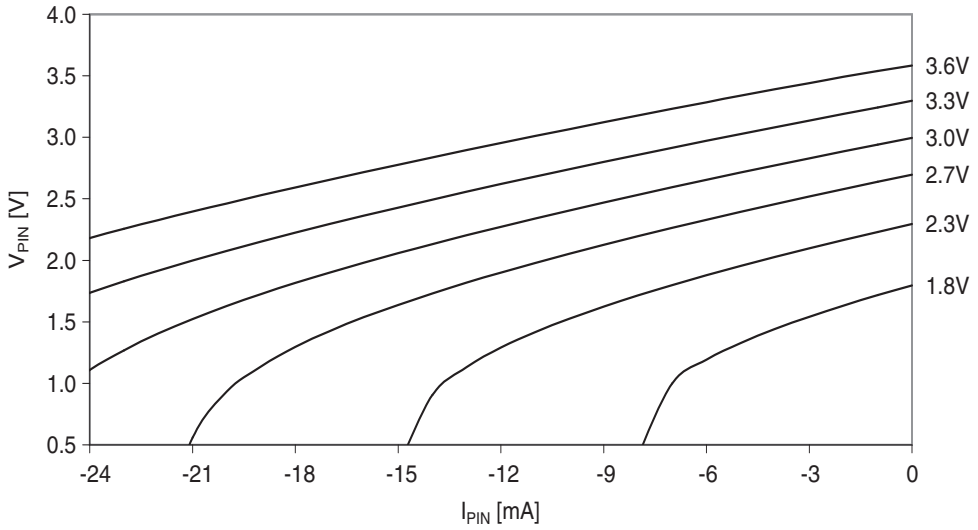
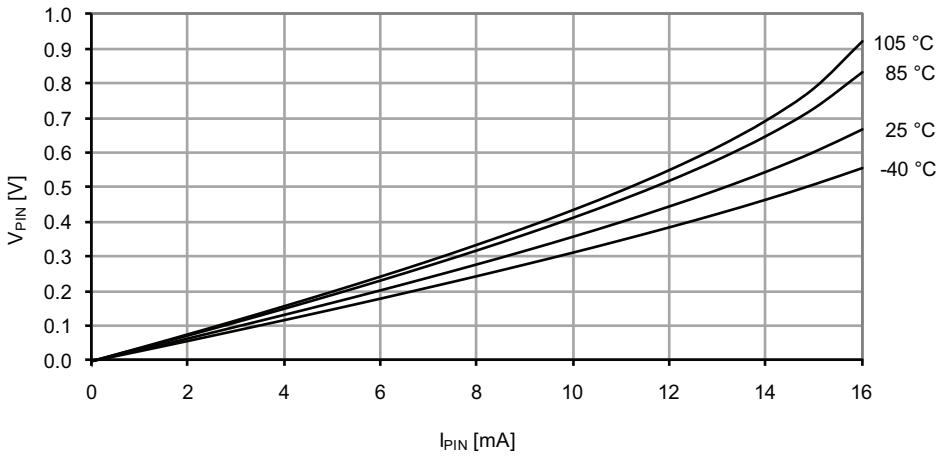


Figure 37-112. I/O pin output voltage vs. sink current.

V_{CC} = 1.8V.



37.2.2.3 Thresholds and Hysteresis

Figure 37-116. I/O pin input threshold voltage vs. V_{CC}.
T = 25°C.

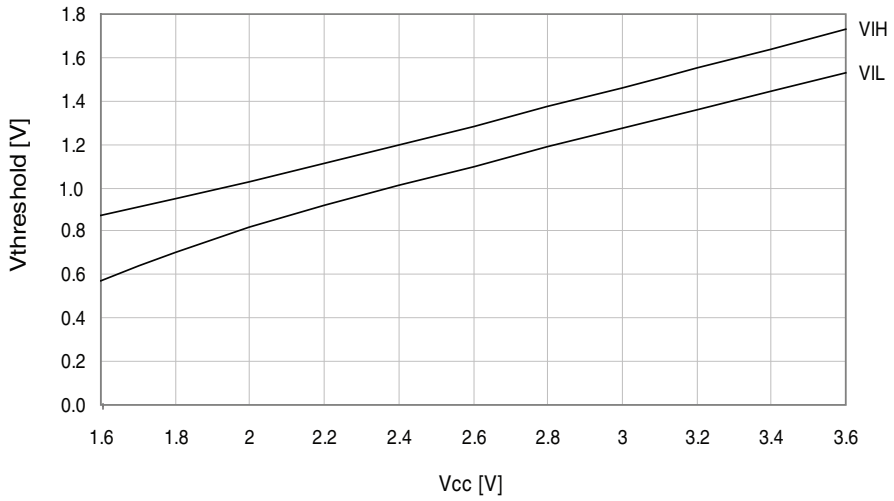


Figure 37-117. I/O pin input threshold voltage vs. V_{CC}.
V_{IH} I/O pin read as "1".

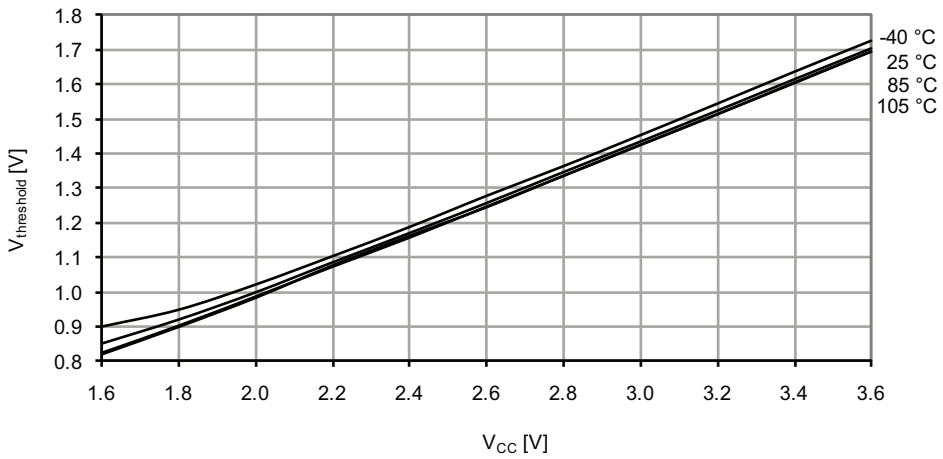


Figure 37-118. I/O pin input threshold voltage vs. V_{CC}.

V_{IL} I/O pin read as "0".

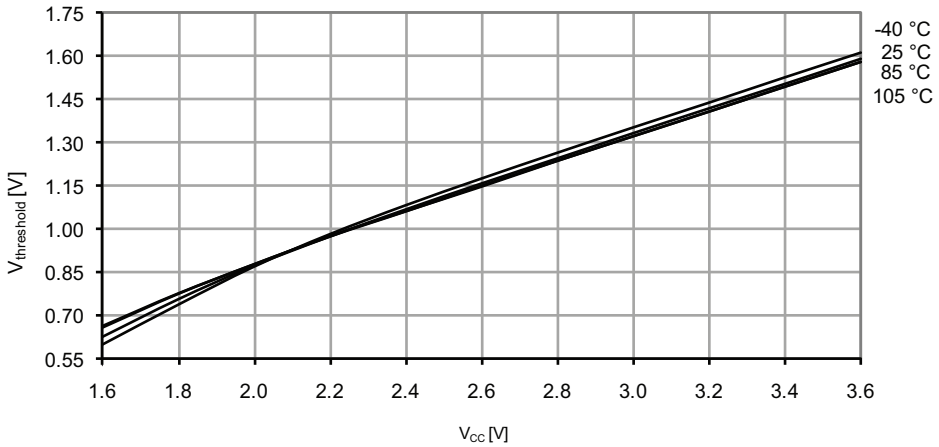
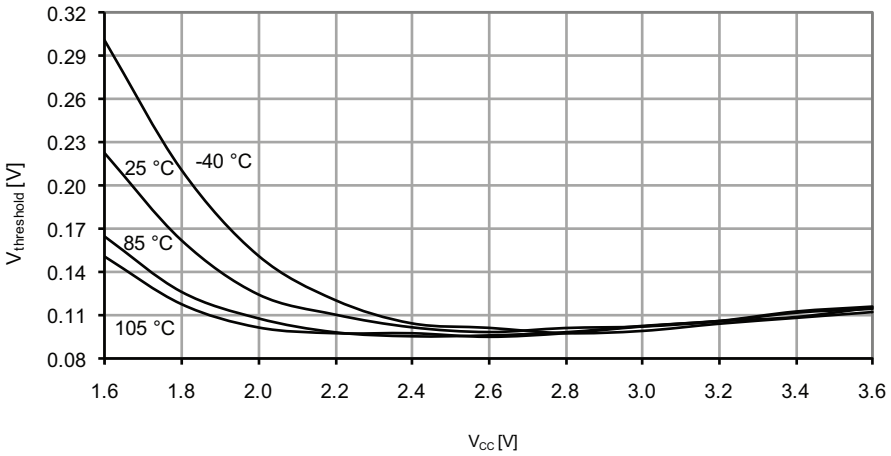


Figure 37-119. I/O pin input hysteresis vs. V_{CC}.



37.3.1.3 Power-down mode supply current

Figure 37-183. Power-down mode supply current vs. temperature.

All functions disabled.

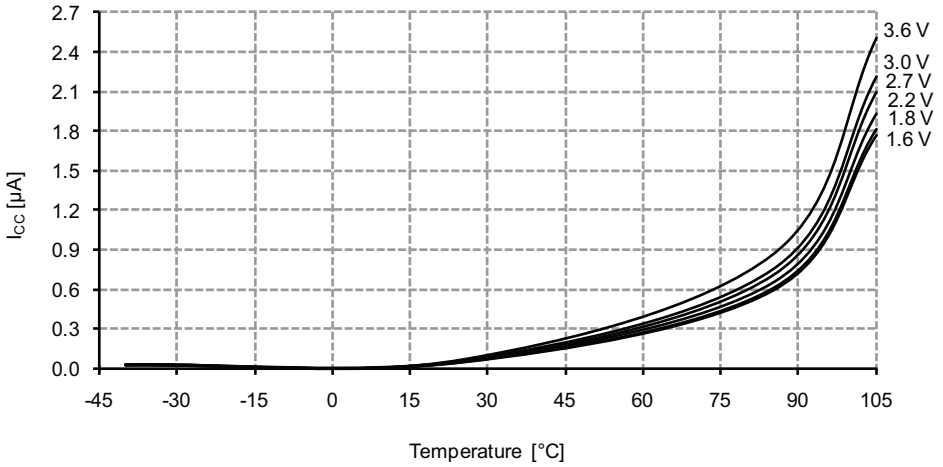


Figure 37-184. Power-down mode supply current vs. V_{CC}.

All functions disabled.

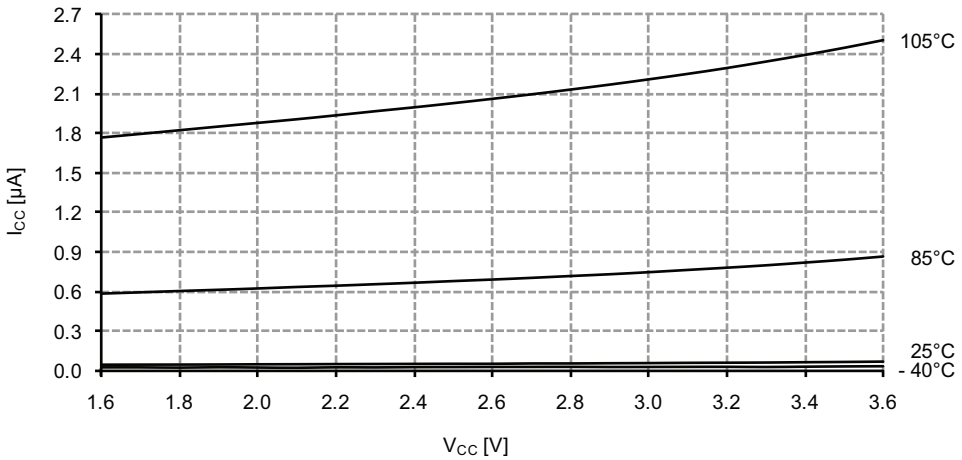
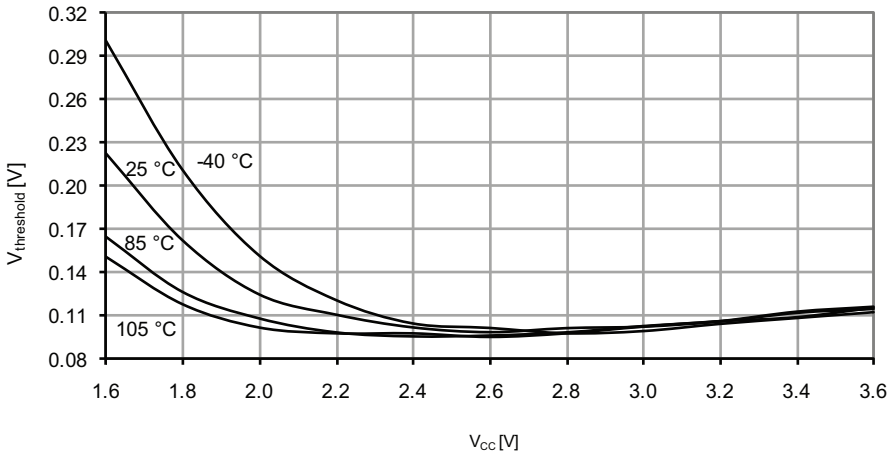


Figure 37-203. I/O pin input hysteresis vs. V_{CC}.



37.3.3 ADC Characteristics

Figure 37-204. INL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

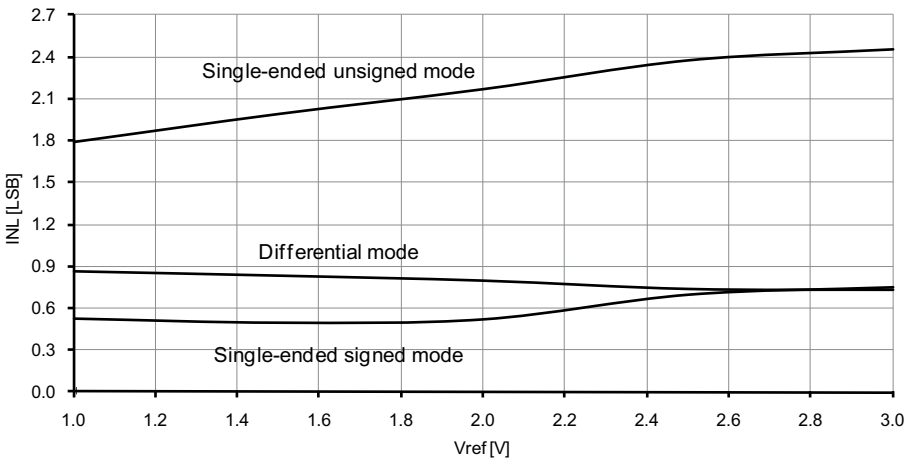


Figure 37-231. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 1.8V.

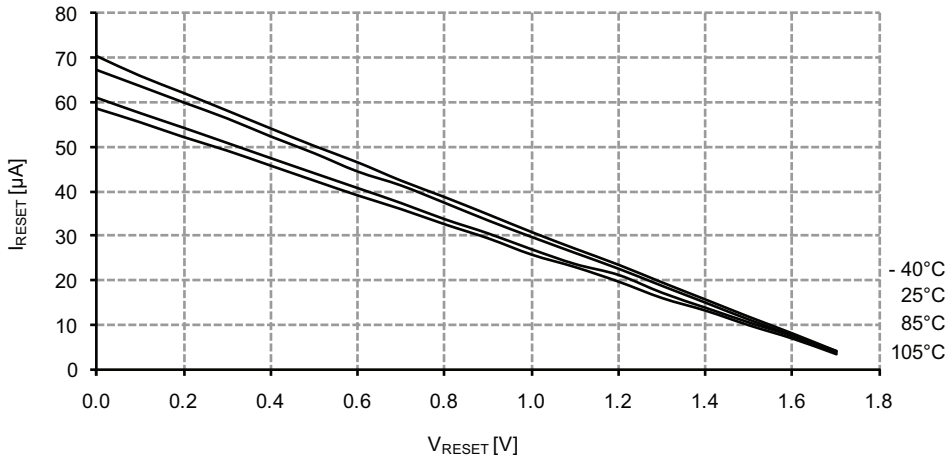


Figure 37-232. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 3.0V.

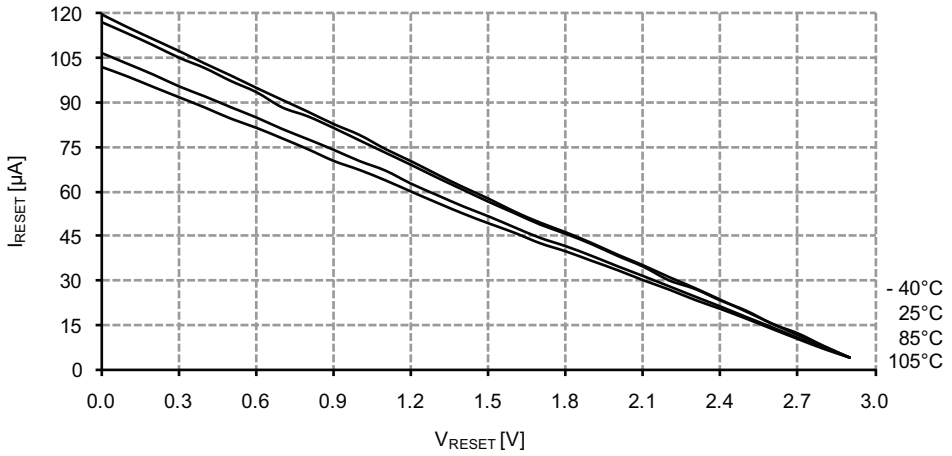
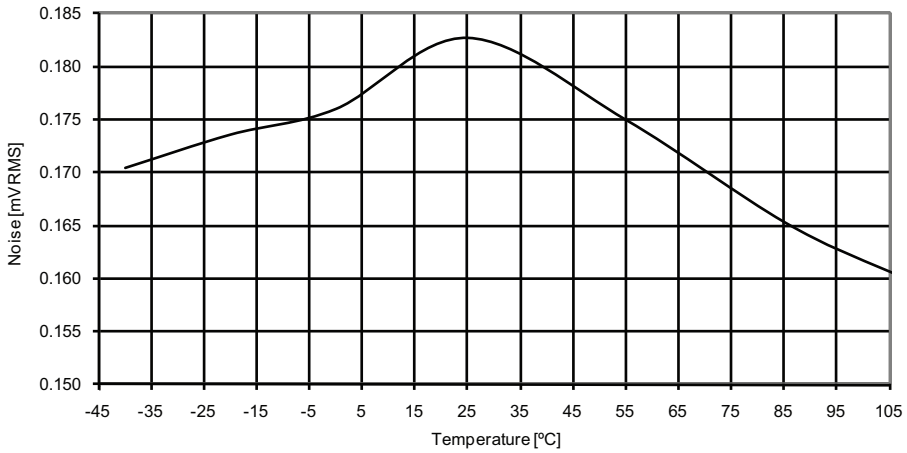


Figure 37-303. DAC noise vs. temperature

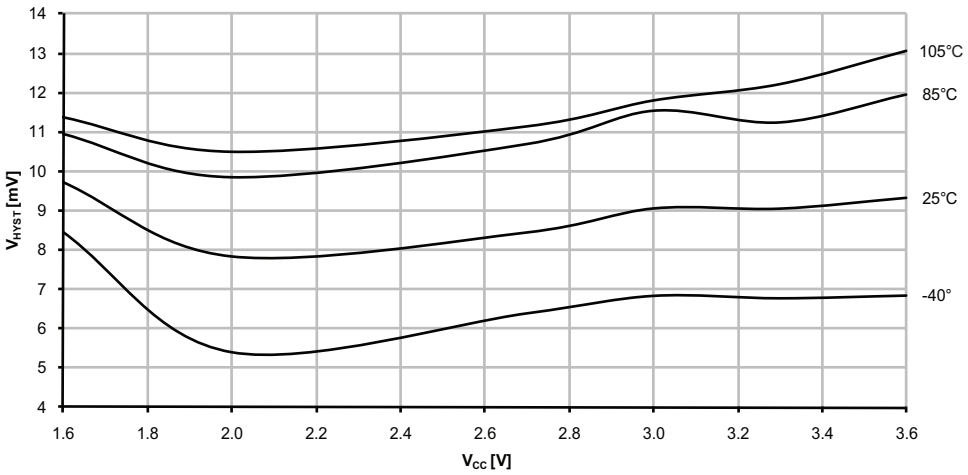
V_{CC} = 3.0V, V_{REF} = 2.4V



37.4.5 Analog Comparator Characteristics

Figure 37-304. Analog comparator hysteresis vs. V_{CC}.

High-speed, small hysteresis



37.4.10.2 32.768kHz Internal Oscillator

Figure 37-323. 32.768kHz internal oscillator frequency vs. temperature

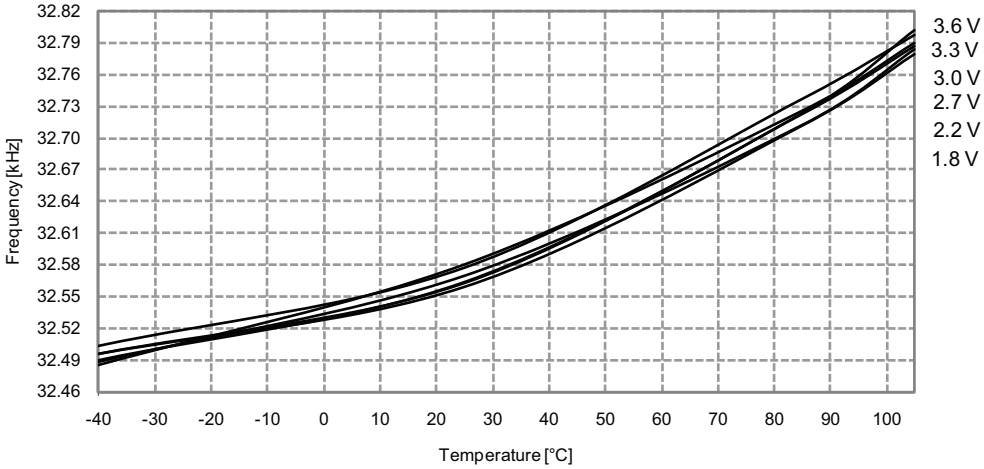
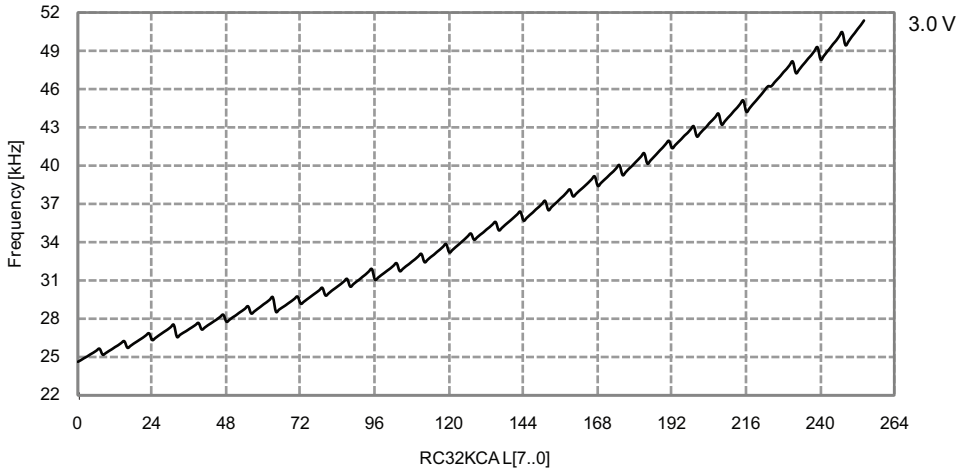


Figure 37-324. 32.768kHz internal oscillator frequency vs. calibration value

V_{CC} = 3.0V, T = 25°C



37.4.10.5 32MHz internal oscillator calibrated to 48MHz

Figure 37-331. 48MHz internal oscillator frequency vs. temperature

DFLL disabled

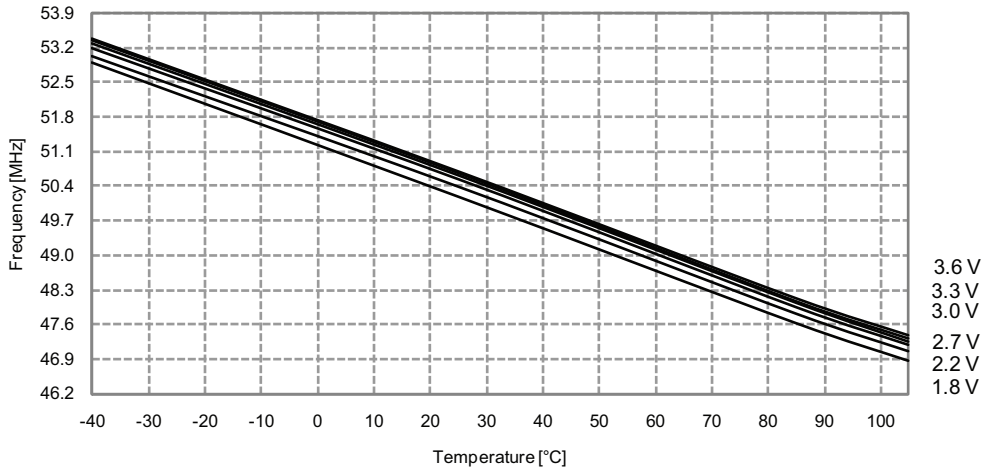
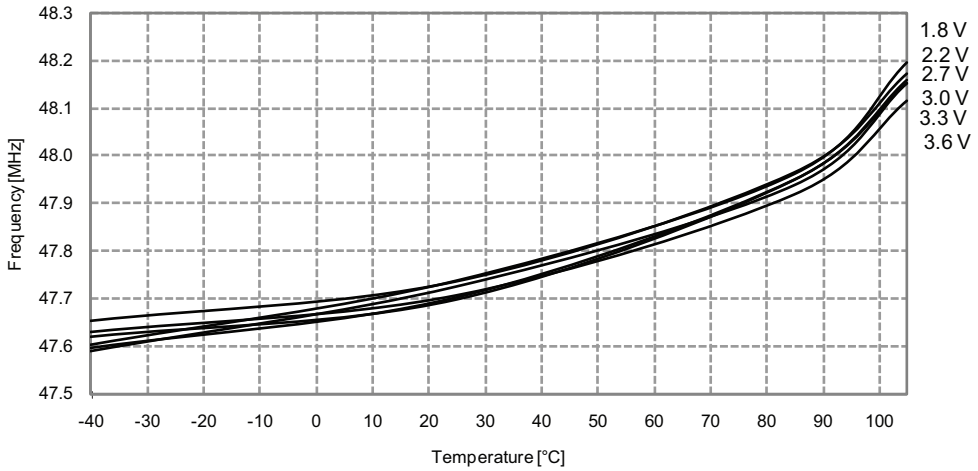


Figure 37-332. 48MHz internal oscillator frequency vs. temperature

DFLL enabled, from the 32.768kHz internal oscillator



39.5 8387D – 02/2013

1.	Updated typos in “Ordering Information” on page 2.
2.	Updated PE2 and PE3 pins in “Pinout/Block Diagram” on page 4 to indicate that these can be used as TOSC pins.
3.	Renamed pin 19 from VDD to VCC in Figure 2-1 on page 4.
4.	Updated page size for ATxmega128A4U in Table 7-3 on page 17.
5.	Added column for TWI using external driver interface in Table 32-3 on page 59.
6.	Updated ATxmega16A4U leakage current in Table 36-7 on page 77.
7.	Added application erase time for ATxmega16A4U in Table 36-21 on page 84.
8.	Updated limits for VIH and VIL: ATxmega16A4U: Table 36-7 on page 77 ATxmega32A4U: Table 36-39 on page 98 ATxmega64A4U: Table 36-71 on page 120 ATxmega128A4U:Table 36-103 on page 142
9.	Updated DAC clock and timing characteristics: ATxmega16A4U: Table 36-13 on page 81 ATxmega32A4U: Table 36-45 on page 101 ATxmega64A4U: Table 36-77 on page 123 ATxmega128A4U: Table 36-109 on page 145.
10.	Updated ATxmega16A4U “ External clock characteristics” on page 86.
11.	Added ESR parameter to the External 16MHz crystal oscillator and XOSC characteristics: ATxmega16A4U: Table 36-29 on page 87 ATxmega32A4U: Table 36-61 on page 108 ATxmega64A4U: Table 36-93 on page 130 ATxmega128A4U: Table 36-125 on page 152.
12.	Updated ATxmega32A4U leakage current in Table 36-39 on page 98.
13.	Added application erase time for ATxmega32A4U in Table 36-53 on page 105.
14.	Updated ATxmega32A4U “ External clock characteristics” on page 107.
15.	Updated ATxmega32A4U current consumption in electrical characteristics section, see “Current consumption” on page 117.
16.	Updated electrical characteristics for “ATxmega64A4U” on page 115.
17.	Updated typical characteristics for “ATxmega64A4U” on page 243.
18.	Added application erase time for ATxmega128A4U in Table 36-117 on page 149.
19.	Updated ATxmega128A4U “ External clock characteristics” on page 151.

39.6 8387C – 03/2012

1.	Updated “Ordering Information” on page 2. Added a new package PW.
2.	Updated “Packaging information” on page 68. A new package PW added.
3.	Updated the Table 36-4 on page 74 with new values for I_{CC} active power consumption.
4.	Updated all typical characteristics in “ Active mode supply current” on page 159.

5.	Updated all typical characteristics in “Power-down mode supply current” on page 166.
6.	Added electrical characteristics for “ATxmega32A4U” on page 93.
7.	Added electrical characteristics for “ATxmega64A4U” on page 115.
8.	Added electrical characteristics for “ATxmega128A4U” on page 137.
9.	Added typical characteristics for “ATxmega64A4U” on page 243
10.	Added typical characteristics for “ATxmega64A4U” on page 243.
12.	Added typical characteristics for “ATxmega128A4U” on page 285.
13.	Updated “Errata” on page 327.
14.	Used Atmel new datasheet template that includes Atmel new addresses on the last page.

39.7 8387B – 12/2011

1.	Updated Figure 2-1 on page 4: “Block Diagram and QFN/TQFP pinout”
2.	Updated Figure 3-1 on page 7: “XMEGA A4U Block Diagram”
3.	Updated “Overview” on page 13.
4.	Updated “ADC – 12-bit Analog to Digital Converter” on page 49.
5.	Updated Figure 28-1 on page 50: “ADC overview.”
6.	Updated “Instruction Set Summary” on page 63.
7.	Updated “Electrical Characteristics” on page 72.
8.	Updated “Typical Characteristics” on page 159.
9.	The order of several figures in the chapter “Typical Characteristics” has been changed
10.	Several new figures have been added to and some figures have been removed from chapter “Typical Characteristics”
11.	Several minor changes/corrections in text and figures have been performed
12.	Table 32-2 on page 59 has been corrected
13.	Table 32-4 on page 60 has been corrected
14.	Table 36-29 on page 85 has been corrected
15.	Table 36-30 on page 86 has been corrected
16.	The heading ”I/O Pin Characteristics” on page 164 has been corrected (the text “and Reset” has been removed)

39.8 8387A – 07/2011

1.	Initial revision.