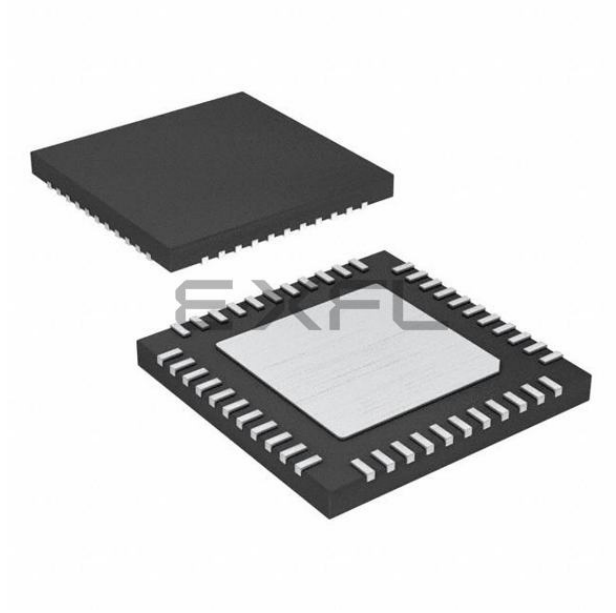

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32a4u-m7

Ordering code	Flash (bytes)	EEPROM (bytes)	SRAM (bytes)	Speed (MHz)	Power supply	Package [1][2][3]	Temp.
ATxmega128A4U-AN	128K + 8K	2K	8K	32	1.6 - 3.6V	44A	0°C - 105°C
ATxmega128A4U-ANR[4]	128K + 8K	2K	8K				
ATxmega64A4U-AN	64K + 4K	2K	4K				
ATxmega64A4U-ANR[4]	64K + 4K	2K	4K				
ATxmega32A4U-AN	32K + 4K	1K	4K				
ATxmega32A4U-ANR[4]	32K + 4K	1K	4K				
ATxmega16A4U-AN	16K + 4K	1K	2K				
ATxmega16A4U-ANR[4]	16K + 4K	1K	2K				
ATxmega128A4U-M7	128K + 8K	2K	8K			PW	
ATxmega128A4U-M7R[4]	128K + 8K	2K	8K				
ATxmega64A4U-M7	64K + 4K	2K	4K				
ATxmega64A4U-M7R[4]	64K + 4K	2K	4K				
ATxmega32A4U-M7	32K + 4K	1K	4K			44M1	
ATxmega32A4U-M7R[4]	32K + 4K	1K	4K				
ATxmega16A4U-M7	16K + 4K	1K	2K				
ATxmega16A4U-M7R[4]	16K + 4K	1K	2K				

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For packaging information, see "Instruction Set Summary" on page 63.
4. Tape and Reel

Package Type	
44A	44-Lead, 10 x 10mm body size, 1.0mm body thickness, 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)
44M1	44-Pad, 7x7x1mm body, lead pitch 0.50mm, 5.20mm exposed pad, thermally enhanced plastic very thin quad no lead package (VQFN)
PW	44-Pad, 7x7x1mm body, lead pitch 0.50mm, 5.20mm exposed pad, thermally enhanced plastic very thin quad no lead package (VQFN)
49C2	49-Ball (7 x 7 Array), 0.65mm Pitch, 5.0 x 5.0 x 1.0mm, very thin, fine-pitch ball grid array package (VFBGA)

Typical Applications

Industrial control	Climate control	Low power battery applications
Factory automation	RF and ZigBee®	Power tools
Building control	USB connectivity	HVAC
Board control	Sensor control	Utility metering
White goods	Optical	Medical applications

Table 14-1. Reset and interrupt vectors

Program address (base address)	Source	Interrupt description
0x000	RESET	
0x002	OSCF_INT_vect	Crystal oscillator failure interrupt vector (NMI)
0x004	PORTC_INT_base	Port C interrupt base
0x008	PORTR_INT_base	Port R interrupt base
0x00C	DMA_INT_base	DMA controller interrupt base
0x014	RTC_INT_base	Real time counter interrupt base
0x018	TWIC_INT_base	Two-Wire Interface on Port C interrupt base
0x01C	TCC0_INT_base	Timer/counter 0 on port C interrupt base
0x028	TCC1_INT_base	Timer/counter 1 on port C interrupt base
0x030	SPIC_INT_vect	SPI on port C interrupt vector
0x032	USARTC0_INT_base	USART 0 on port C interrupt base
0x038	USARTC1_INT_base	USART 1 on port C interrupt base
0x03E	AES_INT_vect	AES interrupt vector
0x040	NVM_INT_base	Nonvolatile Memory interrupt base
0x044	PORTB_INT_base	Port B interrupt base
0x056	PORTE_INT_base	Port E interrupt base
0x05A	TWIE_INT_base	Two-wire Interface on Port E interrupt base
0x05E	TCE0_INT_base	Timer/counter 0 on port E interrupt base
0x06A	TCE1_INT_base	Timer/counter 1 on port E interrupt base
0x074	USARTE0_INT_base	USART 0 on port E interrupt base
0x080	PORTD_INT_base	Port D interrupt base
0x084	PORTA_INT_base	Port A interrupt base
0x088	ACA_INT_base	Analog Comparator on Port A interrupt base
0x08E	ADCA_INT_base	Analog to Digital Converter on Port A interrupt base
0x09A	TCD0_INT_base	Timer/counter 0 on port D interrupt base
0x0A6	TCD1_INT_base	Timer/counter 1 on port D interrupt base
0x0AE	SPID_INT_vector	SPI on port D interrupt vector
0x0B0	USARTD0_INT_base	USART 0 on port D interrupt base
0x0B6	USARTD1_INT_base	USART 1 on port D interrupt base
0x0FA	USB_INT_base	USB on port D interrupt base

A DAC conversion is automatically started when new data to be converted are available. Events from the event system can also be used to trigger a conversion, and this enables synchronized and timed conversions between the DAC and other peripherals, such as a timer/counter. The DMA controller can be used to transfer data to the DAC.

The DAC has high drive strength, and is capable of driving both resistive and capacitive loads, aswell as loads which combine both. A low-power mode is available, which will reduce the drive strength of the output. Internal and external voltage references can be used. The DAC output is also internally available for use as input to the analog comparator or ADC.

PORTB has one DAC. Notation of this peripheral is DACB.

30. AC – Analog Comparator

30.1 Features

- Two Analog Comparators (ACs)
- Selectable propagation delay versus current consumption
- Selectable hysteresis
  - No
  - Small
  - Large
- Analog comparator output available on pin
- Flexible input selection
  - All pins on the port
  - Output from the DAC
  - Bandgap reference voltage
  - A 64-level programmable voltage scaler of the internal AV_{CC} voltage
- Interrupt and event generation on:
  - Rising edge
  - Falling edge
  - Toggle
- Window function interrupt and event generation on:
  - Signal above window
  - Signal inside window
  - Signal below window
- Constant current source with configurable output pin selection

30.2 Overview

The analog comparator (AC) compares the voltage levels on two inputs and gives a digital output based on this comparison. The analog comparator may be configured to generate interrupt requests and/or events upon several different combinations of input change.

Two important properties of the analog comparator's dynamic behavior are: hysteresis and propagation delay. Both of these parameters may be adjusted in order to achieve the optimal operation for each application.

The input selection includes analog port pins, several internal signals, and a 64-level programmable voltage scaler. The analog comparator output state can also be output on a pin for use by external devices.

A constant current source can be enabled and output on a selectable pin. This can be used to replace, for example, external resistors used to charge capacitors in capacitive touch sensing applications.

The analog comparators are always grouped in pairs on each port. These are called analog comparator 0 (AC0) and analog comparator 1 (AC1). They have identical behavior, but separate control registers. Used as pair, they can be set in window mode to compare a signal to a voltage range instead of a voltage level.

PORTA has one AC pair. Notation is ACA.

32.1.1 Operation/Power Supply

V_{CC}	Digital supply voltage
AV_{CC}	Analog supply voltage
GND	Ground

32.1.2 Port Interrupt functions

SYNC	Port pin with full synchronous and limited asynchronous interrupt function
ASYNC	Port pin with full synchronous and full asynchronous interrupt function

32.1.3 Analog functions

ACn	Analog Comparator input pin n
ACnOUT	Analog Comparator n Output
ADCn	Analog to Digital Converter input pin n
DACn	Digital to Analog Converter output pin n
A_{REF}	Analog Reference input pin

32.1.4 Timer/Counter and AWEX functions

OCnxLS	Output Compare Channel x Low Side for Timer/Counter n
OCnxHS	Output Compare Channel x High Side for Timer/Counter n

33. Peripheral Module Address Map

The address maps show the base address for each peripheral and module in Atmel AVR XMEGA A4U. For complete register description and summary for each peripheral module, refer to the XMEGA AU manual.

Table 33-1. Peripheral module address map.

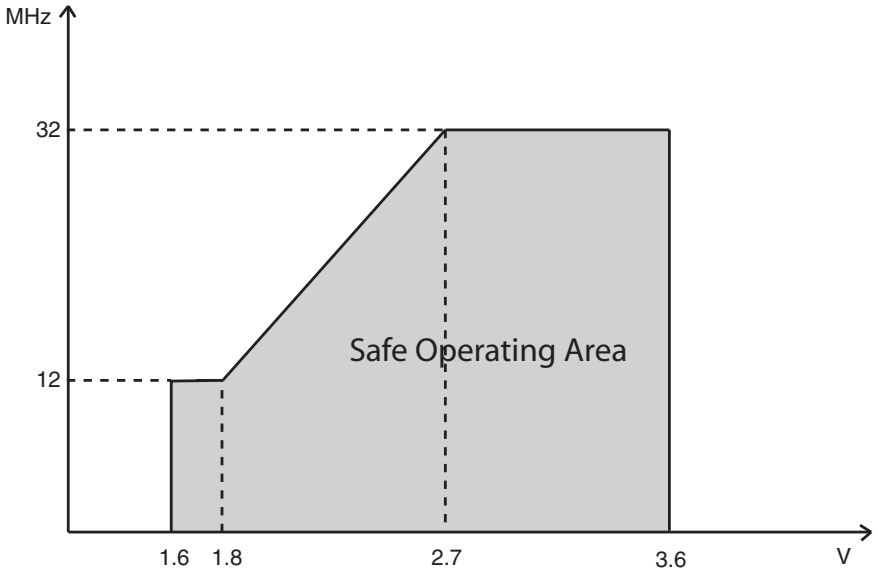
Base address	Name	Description
0x0000	GPIO	General Purpose IO Registers
0x0010	VPORT0	Virtual Port 0
0x0014	VPORT1	Virtual Port 1
0x0018	VPORT2	Virtual Port 2
0x001C	VPORT3	Virtual Port 2
0x0030	CPU	CPU
0x0040	CLK	Clock Control
0x0048	SLEEP	Sleep Controller
0x0050	OSC	Oscillator Control
0x0060	DFLLRC32M	DFLL for the 32MHz Internal RC Oscillator
0x0068	DFLLRC2M	DFLL for the 2MHz RC Oscillator
0x0070	PR	Power Reduction
0x0078	RST	Reset Controller
0x0080	WDT	Watch-Dog Timer
0x0090	MCU	MCU Control
0x00A0	PMIC	Programmable MUltilevel Interrupt Controller
0x00B0	PORTCFG	Port Configuration
0x00C0	AES	AES Module
0x00D0	CRC	CRC Module
0x0100	DMA	DMA Module
0x0180	EVSYS	Event System
0x01C0	NVM	Non Volatile Memory (NVM) Controller
0x0200	ADCA	Analog to Digital Converter on port A
0x0380	ACA	Analog Comparator pair on port A
0x0400	RTC	Real Time Counter
0x0480	TWIC	Two Wire Interface on port C
0x04A0	TWIE	Two Wire Interface on port E
0x04C0	USB	Universal Serial Bus Interface
0x0600	PORTA	Port A

Table 36-3. Operating voltage and frequency.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 36-1 the Frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

Figure 36-1. Maximum Frequency vs. V_{CC}.



36.1.8 Analog Comparator Characteristics

Table 36-15. Analog Comparator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage			<±10		mV
I_{lk}	Input leakage current			<1.0		nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			100		µs
V_{hys1}	Hysteresis, none			0		mV
V_{hys2}	Hysteresis, small	mode = High Speed (HS)		13		mV
		mode = Low Power (LP)		30		
V_{hys3}	Hysteresis, large	mode = HS		30		mV
		mode = LP		60		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T= 85°C mode = HS		30	90	ns
		mode = HS		30		
		V_{CC} = 3.0V, T= 85°C mode = LP		130	500	
		mode = LP		130		
	64-level voltage scaler	Integral non-linearity (INL)		0.3	0.5	lsb

36.1.9 Bandgap and Internal 1.0V Reference Characteristics

Table 36-16. Bandgap and Internal 1.0V reference characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC or DAC	1 Clk_{PER} + 2.5µs			µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T= 85°C, after calibration	0.99	1.0	1.01	V
	Variation over voltage and temperature	Relative to T= 85°C, V_{CC} = 3.0V		±1.5		%

36.2.3 Current consumption

Table 36-36. Current consumption for Active mode and sleep modes.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption[1]	32kHz, Ext. Clk	V_{CC} = 1.8V		40		µA
			V_{CC} = 3.0V		80		
		1MHz, Ext. Clk	V_{CC} = 1.8V		230		
			V_{CC} = 3.0V		480		
		2MHz, Ext. Clk	V_{CC} = 1.8V		430	600	
			V_{CC} = 3.0V		0.9	1.4	mA
		32MHz, Ext. Clk			9.6	12	
	Idle power consumption[1]	32kHz, Ext. Clk	V_{CC} = 1.8V		2.4		µA
			V_{CC} = 3.0V		3.9		
		1MHz, Ext. Clk	V_{CC} = 1.8V		62		
			V_{CC} = 3.0V		118		
		2MHz, Ext. Clk	V_{CC} = 1.8V		125	225	
			V_{CC} = 3.0V		240	350	
		32MHz, Ext. Clk			3.8	5.5	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			1.2	4.5	
		T = 105°C			3.5	6.0	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.3	3.0	
		WDT and sampled BOD enabled, T = 85°C			2.4	6.0	
		WDT and sampled BOD enabled, T = 105°C			4.5	8.0	
	Power-save power consumption[2]	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.2		µA
			V_{CC} = 3.0V		1.3		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.6	2.0	
			V_{CC} = 3.0V		0.7	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.8	3.0	
			V_{CC} = 3.0V		1.0	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		320		

Notes:
1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

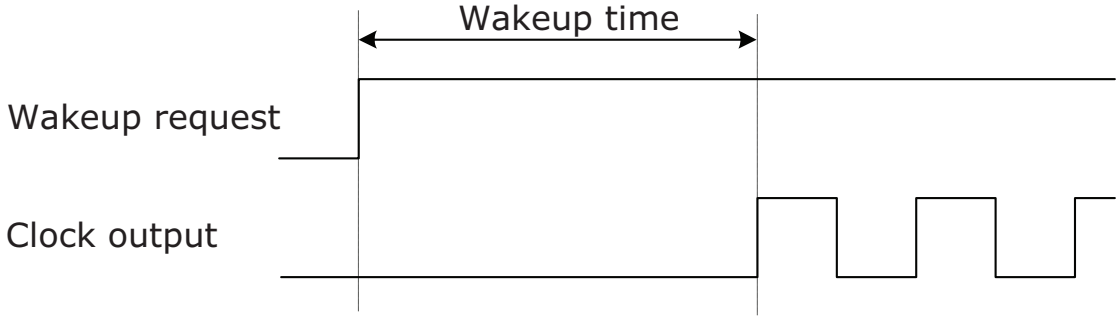
36.2.4 Wake-up time from sleep modes

Table 36-38. Device wake-up time from sleep modes with various system clock sources.

Symbol	Parameter	Condition	Min.	Typ. (1)	Max.	Units
t_{wakeup}	Wake-up time from idle, standby, and extended standby mode	External 2MHz clock		2.0		µs
		32.768kHz internal oscillator		120		
		2MHz internal oscillator		2.0		
		32MHz internal oscillator		0.2		
	Wake-up time from power-save and power-down mode	External 2MHz clock		4.5		µs
		32.768kHz internal oscillator		320		
		2MHz internal oscillator		9.0		
		32MHz internal oscillator		5.0		

Note: 1. The wake-up time is the time from the wake-up request is given until the peripheral clock is available on pin, see Figure 36-9. All peripherals and modules start execution from the first clock cycle, expect the CPU that is halted for four clock cycles before program execution starts.

Figure 36-9. Wake-up time definition.



Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$t_{HD;DAT}$	Data hold time	$f_{SCL} \leq 100kHz$	0		3.45	µs
		$f_{SCL} > 100kHz$	0		0.9	
$t_{SU;DAT}$	Data setup time	$f_{SCL} \leq 100kHz$	250			ns
		$f_{SCL} > 100kHz$	100			
$t_{SU;STO}$	Setup time for STOP condition	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
t_{BUF}	Bus free time between a STOP and START condition	$f_{SCL} \leq 100kHz$	4.7			µs
		$f_{SCL} > 100kHz$	1.3			

Notes:
1. Required only for $f_{SCL} > 100kHz$.
2. C_b = Capacitance of one bus line in pF.
3. f_{PER} = Peripheral clock frequency.

Figure 37-74. 2MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator .

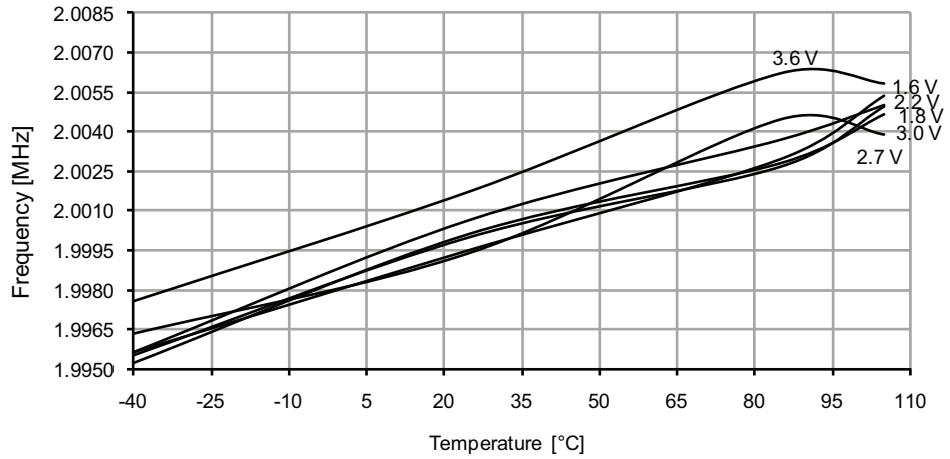


Figure 37-75. 2MHz internal oscillator CALA calibration step size.

V_{CC} = 3V.

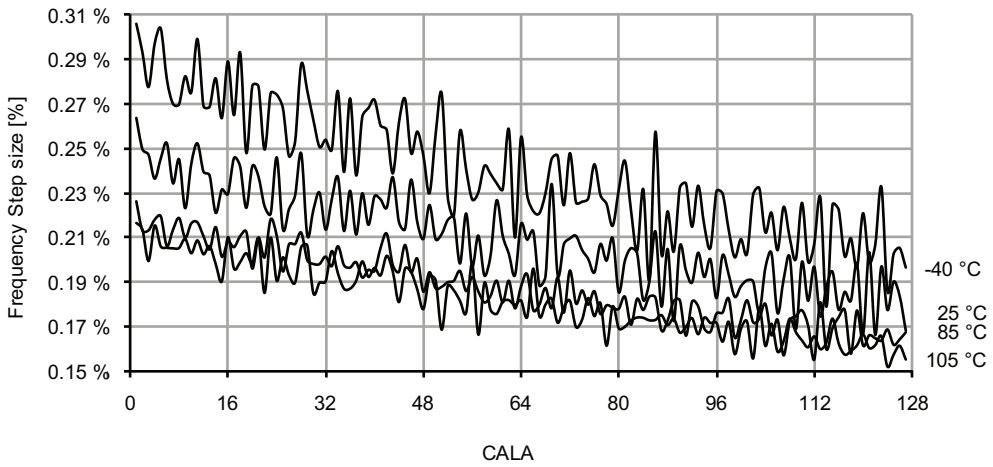


Figure 37-109. I/O pin output voltage vs. source current.

V_{CC} = 3.0V.

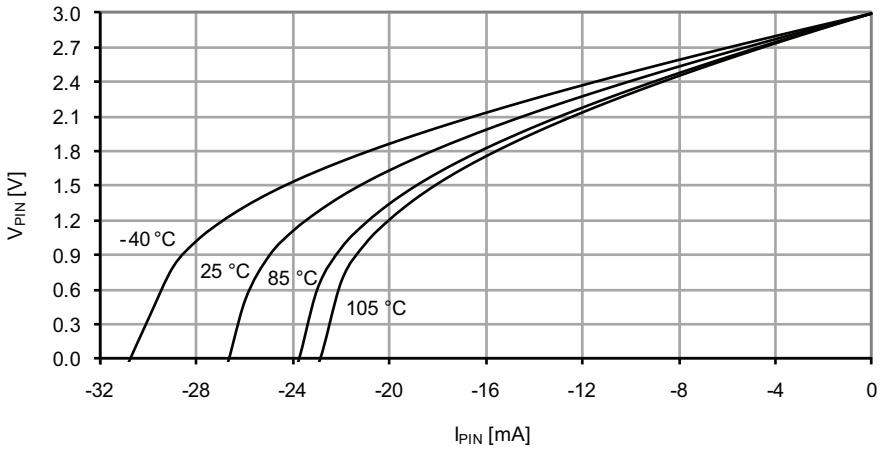


Figure 37-110. I/O pin output voltage vs. source current.

V_{CC} = 3.3V.

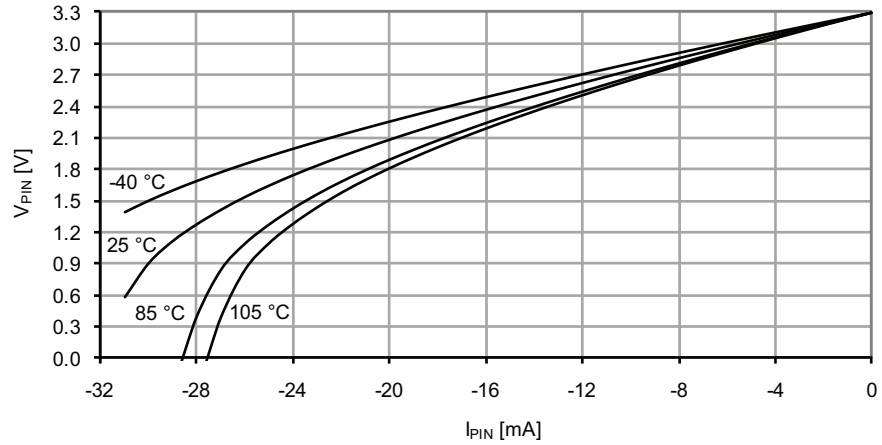
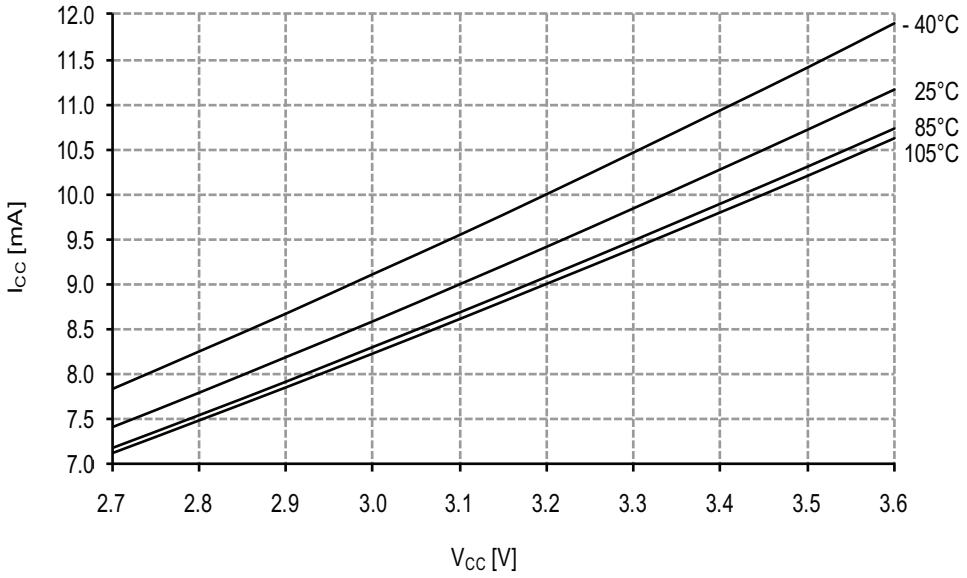


Figure 37-175. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator.



37.3.1.2 Idle mode supply current

Figure 37-176. Idle mode supply current vs. frequency.

f_{SYS} = 0 - 1MHz external clock, T = 25°C.

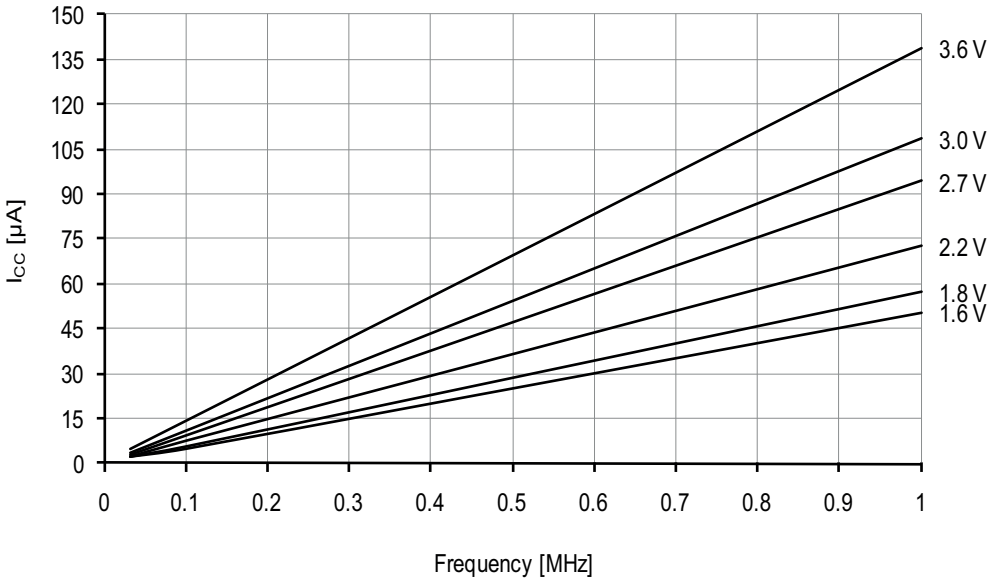
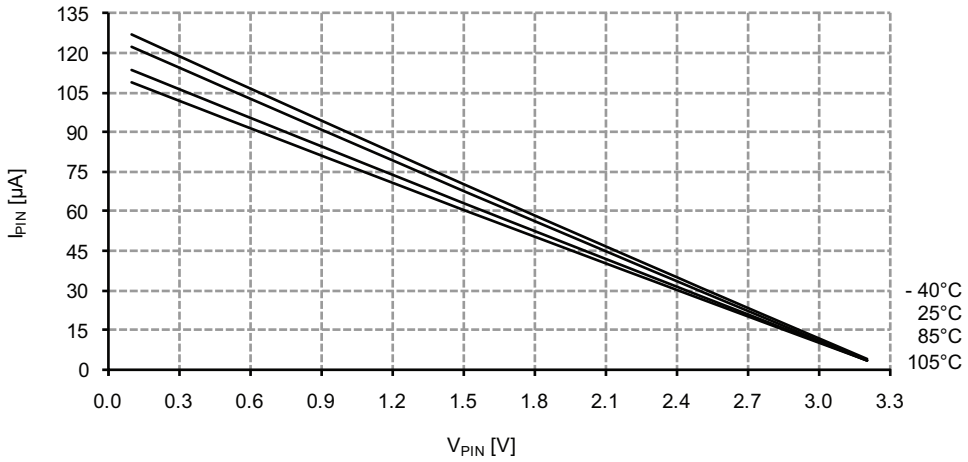


Figure 37-191. I/O pin pull-up resistor current vs. input voltage.

V_{CC} = 3.3V.



37.3.2.2 Output Voltage vs. Sink/Source Current

Figure 37-192. I/O pin output voltage vs. source current.

V_{CC} = 1.8V.

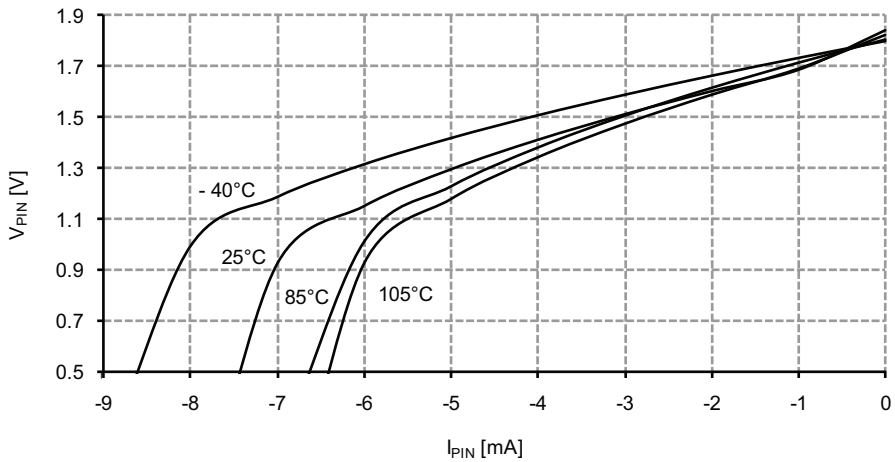
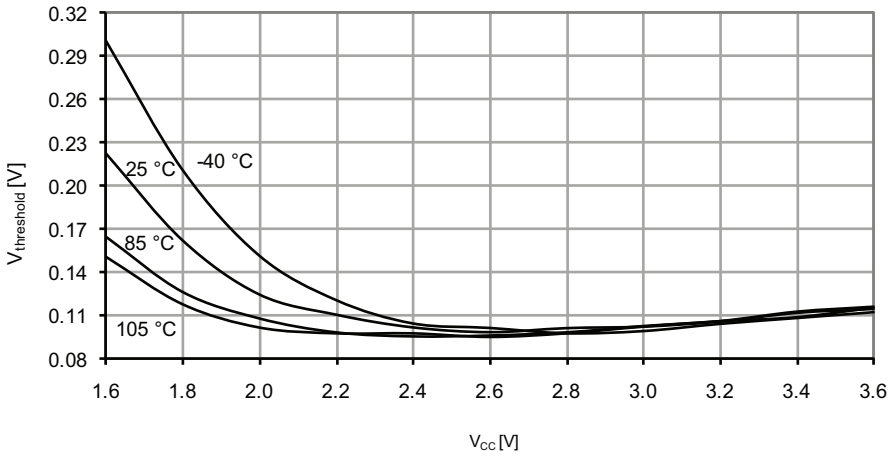


Figure 37-203. I/O pin input hysteresis vs. V_{CC}.



37.3.3 ADC Characteristics

Figure 37-204. INL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

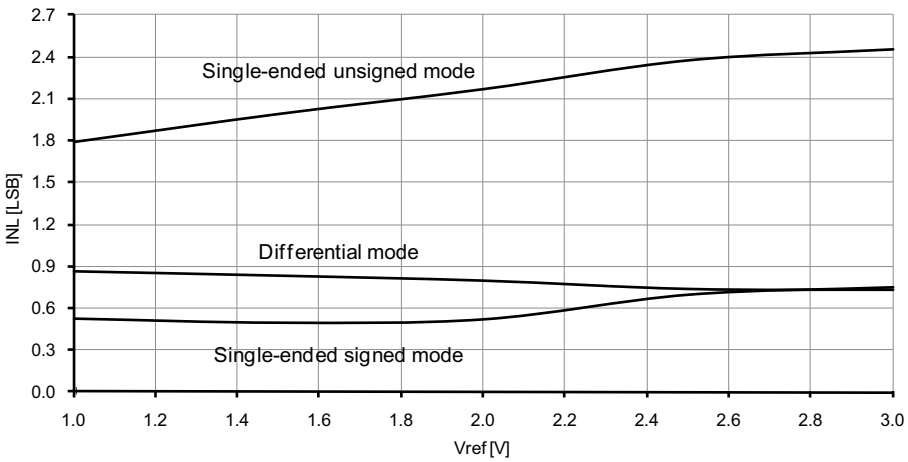


Figure 37-213. Gain error vs. temperature.

V_{CC} = 2.7V, V_{REF} = external 1.0V.

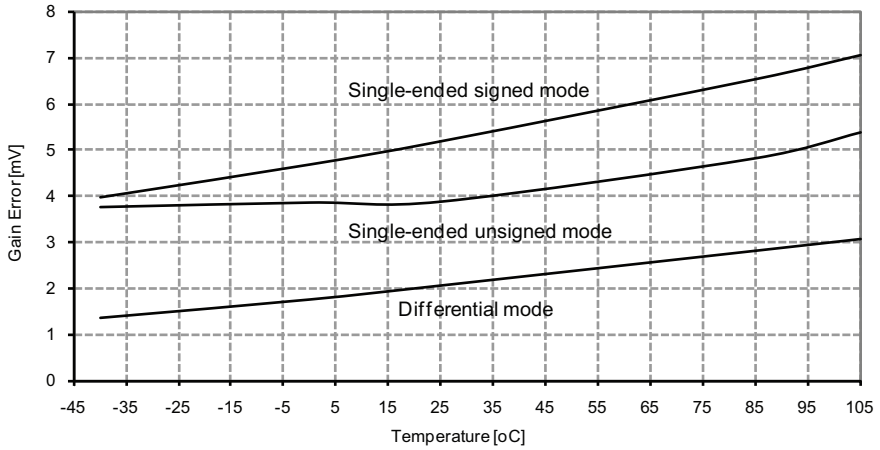
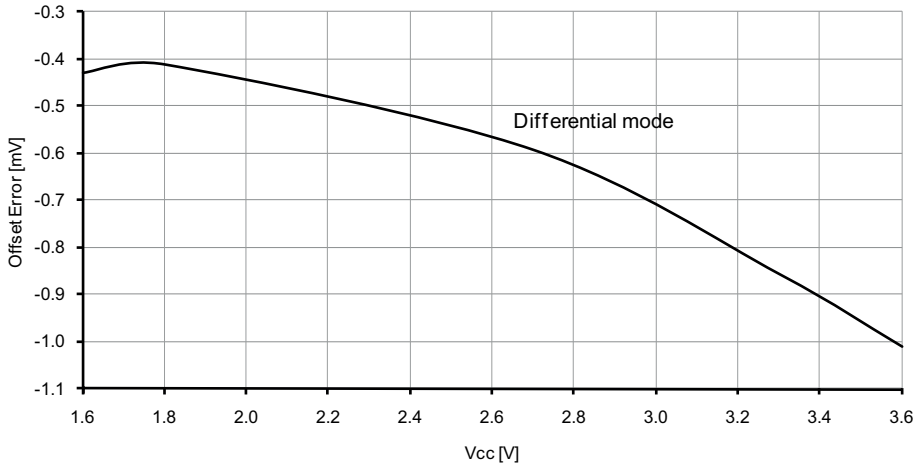


Figure 37-214. Offset error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.



37.3.10.2 32.768kHz Internal Oscillator

Figure 37-239. 32.768kHz internal oscillator frequency vs. temperature.

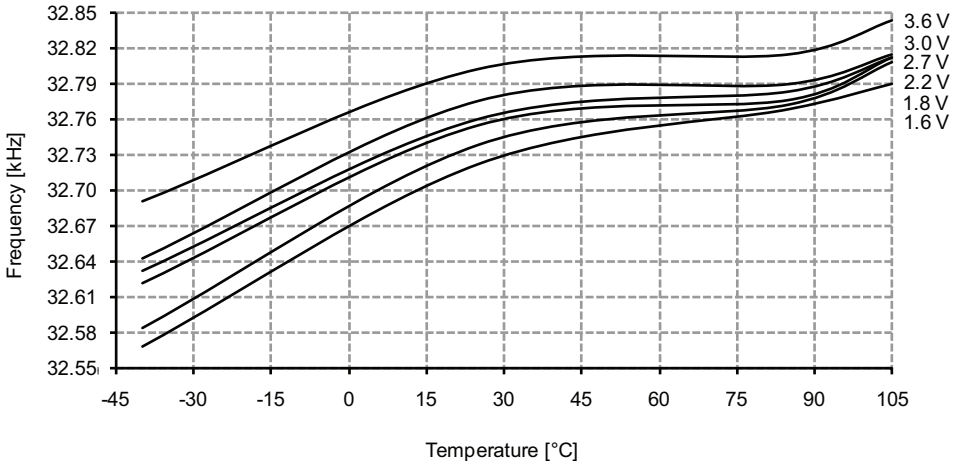
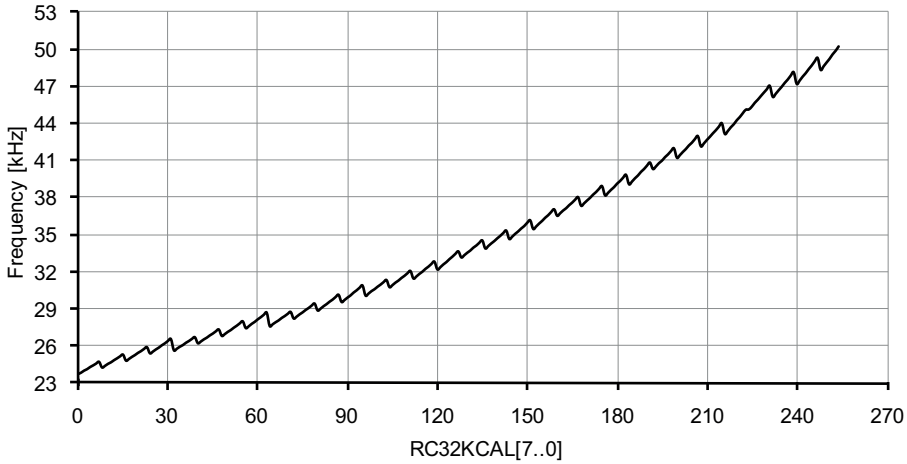


Figure 37-240. 32.768kHz internal oscillator frequency vs. calibration value.

V_{CC} = 3.0V, T = 25°C.



37.3.10.3 2MHz Internal Oscillator

Figure 37-241. 2MHz internal oscillator frequency vs. temperature.

DFLL disabled.

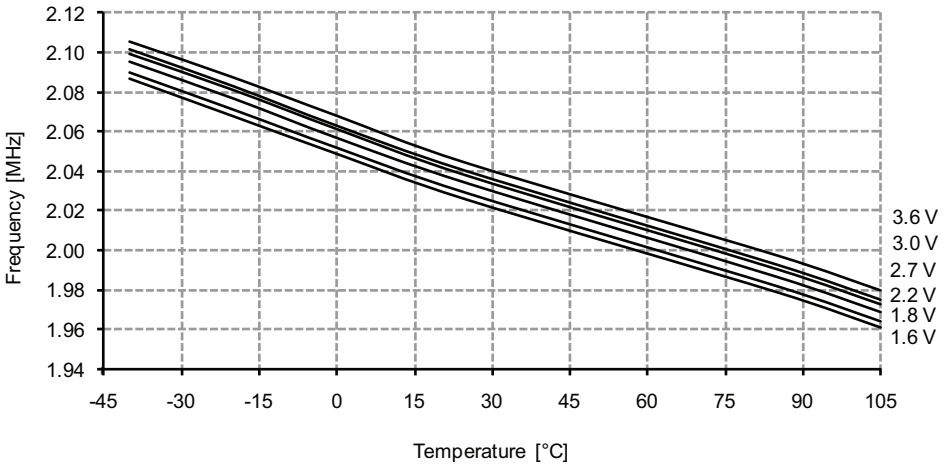


Figure 37-242. 2MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator .