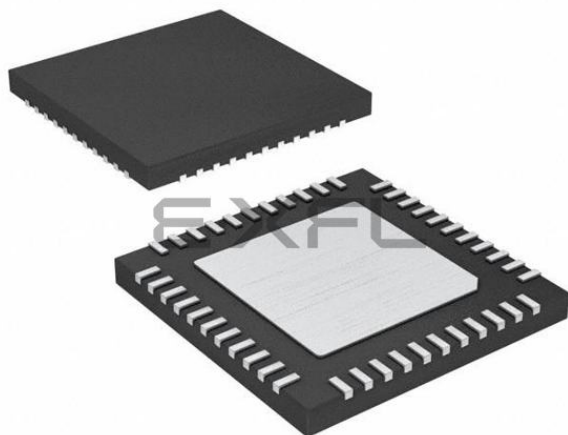




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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32a4u-m7r

20. RTC – 16-bit Real-Time Counter

20.1 Features

- 16-bit resolution
- Selectable clock source
 - 32.768kHz external crystal
 - External clock
 - 32.768kHz internal oscillator
 - 32kHz internal ULP oscillator
- Programmable 10-bit clock prescaling
- One compare register
- One period register
- Clear counter on period overflow
- Optional interrupt/event on overflow and compare match

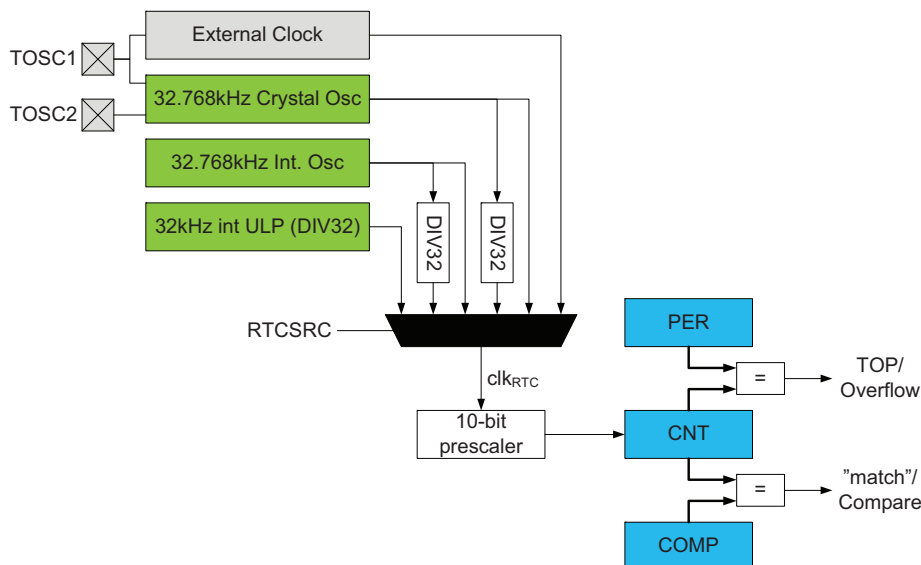
20.2 Overview

The 16-bit real-time counter (RTC) is a counter that typically runs continuously, including in low-power sleep modes, to keep track of time. It can wake up the device from sleep modes and/or interrupt the device at regular intervals.

The reference clock is typically the 1.024kHz output from a high-accuracy crystal of 32.768kHz, and this is the configuration most optimized for low power consumption. The faster 32.768kHz output can be selected if the RTC needs a resolution higher than 1ms. The RTC can also be clocked from an external clock signal, the 32.768kHz internal oscillator or the 32kHz internal ULP oscillator.

The RTC includes a 10-bit programmable prescaler that can scale down the reference clock before it reaches the counter. A wide range of resolutions and time-out periods can be configured. With a 32.768kHz clock source, the maximum resolution is 30.5μs, and time-out periods can range up to 2000 seconds. With a resolution of 1s, the maximum timeout period is more than 18 hours (65536 seconds). The RTC can give a compare interrupt and/or event when the counter equals the compare register value, and an overflow interrupt and/or event when it equals the period register value.

Figure 20-1. Real-time counter overview.



PORTC and PORTE each has one TWI. Notation of these peripherals are TWIC and TWIE.

23. SPI – Serial Peripheral Interface

23.1 Features

- Two identical SPI peripherals
- Full-duplex, three-wire synchronous data transfer
- Master or slave operation
- Lsb first or msb first data transfer
- Eight programmable bit rates
- Interrupt flag at the end of transmission
- Write collision flag to indicate data collision
- Wake up from idle sleep mode
- Double speed master mode

23.2 Overview

The Serial Peripheral Interface (SPI) is a high-speed synchronous data transfer interface using three or four pins. It allows fast communication between an Atmel AVR XMEGA device and peripheral devices or between several microcontrollers. The SPI supports full-duplex communication.

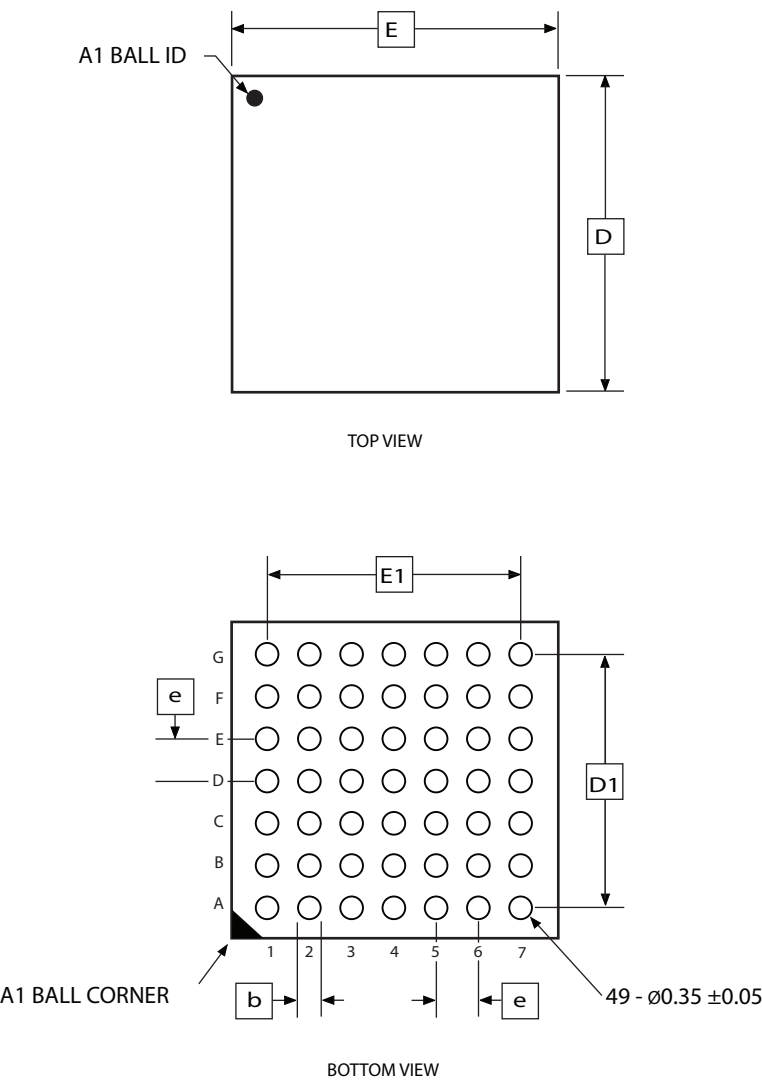
A device connected to the bus must act as a master or slave. The master initiates and controls all data transactions. PORTC and PORTD each has one SPI. Notation of these peripherals are SPIC and SPID.

A DAC conversion is automatically started when new data to be converted are available. Events from the event system can also be used to trigger a conversion, and this enables synchronized and timed conversions between the DAC and other peripherals, such as a timer/counter. The DMA controller can be used to transfer data to the DAC.

The DAC has high drive strength, and is capable of driving both resistive and capacitive loads, as well as loads which combine both. A low-power mode is available, which will reduce the drive strength of the output. Internal and external voltage references can be used. The DAC output is also internally available for use as input to the analog comparator or ADC.

PORTB has one DAC. Notation of this peripheral is DACB.

35.4 49C2



COMMON DIMENSIONS (Unit of Measure = mm)				
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.00	
A1	0.20	–	–	
A2	0.65	–	–	
D	4.90	5.00	5.10	
D1	3.90 BSC			
E 4.90	5.00	5.10		
E1	3.90 BSC			
b	0.30	0.35	0.40	
e	0.65 BSC			

3/14/08

 Package Drawing Contact: packagedrawings@atmel.com	TITLE 49C2, 49-ball (7 x 7 array), 0.65mm pitch, 5.0 x 5.0 x 1.0mm, very thin, fine-pitch ball grid array package (VFBGA)	GPC	DRAWING NO.	REV.
		CBD	49C2	A

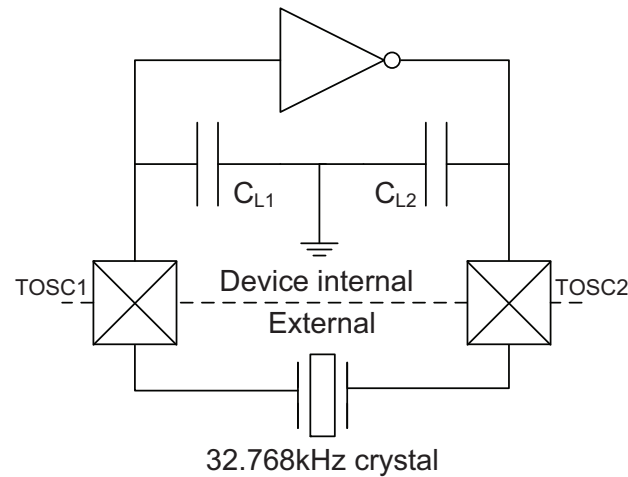
36.1.14.8 External 32.768kHz crystal oscillator and TOSC characteristics

Table 36-30. External 32.768kHz crystal oscillator and TOSC characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
C _{TOSC1}	Parasitic capacitance TOSC1 pin			5.4		pF
		Alternate TOSC location		4.0		
C _{TOSC2}	Parasitic capacitance TOSC2 pin			7.1		pF
		Alternate TOSC location		4.0		
	Recommended safety factor	capacitance load matched to crystal specification	3			

Note: 1. See Figure 36-4 for definition.

Figure 36-4. TOSC input capacitance.



The parasitic capacitance between the TOSC pins is $C_{L1} + C_{L2}$ in series as seen from the crystal when oscillating without external capacitors.

36.2.14 Clock and Oscillator Characteristics

36.2.14.1 Calibrated 32.768kHz Internal Oscillator characteristics

Table 36-54. 32.768kHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V _{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	%

36.2.14.2 Calibrated 2MHz RC Internal Oscillator characteristics

Table 36-55. 2MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8		2.2	MHz
	Factory calibrated frequency			2.0		MHz
	Factory calibration accuracy	T = 85°C, V _{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	%
	DFLL calibration stepsize			0.21		%

36.2.14.3 Calibrated and tunable 32MHz internal oscillator characteristics

Table 36-56. 32MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30		55	MHz
	Factory calibrated frequency			32		MHz
	Factory calibration accuracy	T = 85°C, V _{CC} = 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	%
	DFLL calibration step size			0.22		%

36.2.14.4 32kHz Internal ULP Oscillator characteristics

Table 36-57. 32kHz internal ULP oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Output frequency			32		kHz
	Accuracy		-30		30	%

Table 36-60. External clock with prescaler ⁽¹⁾ for system clock.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency ⁽²⁾	$V_{CC} = 1.6 - 1.8V$	0		90	MHz
		$V_{CC} = 2.7 - 3.6V$	0		142	
t_{CK}	Clock Period	$V_{CC} = 1.6 - 1.8V$	11			ns
		$V_{CC} = 2.7 - 3.6V$	7			
t_{CH}	Clock High Time	$V_{CC} = 1.6 - 1.8V$	4.5			ns
		$V_{CC} = 2.7 - 3.6V$	2.4			
t_{CL}	Clock Low Time	$V_{CC} = 1.6 - 1.8V$	4.5			ns
		$V_{CC} = 2.7 - 3.6V$	2.4			
t_{CR}	Rise Time (for maximum frequency)	$V_{CC} = 1.6 - 1.8V$			1.5	ns
		$V_{CC} = 2.7 - 3.6V$			1.0	
t_{CF}	Fall Time (for maximum frequency)	$V_{CC} = 1.6 - 1.8V$			1.5	ns
		$V_{CC} = 2.7 - 3.6V$			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

36.2.14.7 External 16MHz crystal oscillator and XOSC characteristic

Table 36-61. External 16MHz crystal oscillator and XOSC characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0		<10		ns
			FRQRANGE=1, 2, or 3		<1		
		XOSCPWR=1			<1		
	Long term jitter	XOSCPWR=0	FRQRANGE=0		<6		ns
			FRQRANGE=1, 2, or 3		<0.5		
		XOSCPWR=1			<0.5		
	Frequency error	XOSCPWR=0	FRQRANGE=0		<0.1		%
			FRQRANGE=1		<0.05		
			FRQRANGE=2 or 3		<0.005		
		XOSCPWR=1			<0.005		
	Duty cycle	XOSCPWR=0	FRQRANGE=0		40		%
			FRQRANGE=1		42		
			FRQRANGE=2 or 3		45		
		XOSCPWR=1			48		

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Offset error, input referred	1x gain, normal mode			-2		mV
		8x gain, normal mode			-5		
		64x gain, normal mode			-4		
	Noise	1x gain, normal mode	$V_{CC} = 3.6V$ Ext. V_{REF}		0.5		mV rms
		8x gain, normal mode			1.5		
		64x gain, normal mode			11		

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.

36.3.7 DAC Characteristics

Table 36-76. Power supply, reference and output range.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage			$V_{CC} - 0.3$		$V_{CC} + 0.3$	V
AV_{REF}	External reference voltage			1.0		$V_{CC} - 0.6$	V
$R_{channel}$	DC output impedance					50	Ω
	Linear output voltage range			0.15		$AV_{CC} - 0.15$	V
R_{AREF}	Reference input resistance				>10		M Ω
C_{AREF}	Reference input capacitance	Static load			7		pF
	Minimum resistance load			1.0			k Ω
	Maximum capacitance load					100	pF
		1000 Ω serial resistance				1.0	nF
	Output sink/source	Operating within accuracy specification				$AV_{CC}/1000$	mA
		Safe operation				10	

Table 36-77. Clock and timing.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
f_{DAC}	Conversion rate	$C_{load} = 100pF$, maximum step size	Normal mode	0		1000	ksps
			Low power mode			500	

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Long term jitter	XOSCPWR=0	FRQRANGE=0		<6		ns
			FRQRANGE=1, 2, or 3		<0.5		
		XOSCPWR=1			<0.5		
	Frequency error	XOSCPWR=0	FRQRANGE=0		<0.1		%
			FRQRANGE=1		<0.05		
			FRQRANGE=2 or 3		<0.005		
		XOSCPWR=1			<0.005		
	Duty cycle	XOSCPWR=0	FRQRANGE=0		40		%
			FRQRANGE=1		42		
			FRQRANGE=2 or 3		45		
		XOSCPWR=1			48		
R _Q	Negative impedance ⁽¹⁾	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF	2.4k			Ω
			1MHz crystal, CL=20pF	8.7k			
			2MHz crystal, CL=20pF	2.1k			
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal	4.2k			
			8MHz crystal	250			
			9MHz crystal	195			
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal	360			
			9MHz crystal	285			
			12MHz crystal	155			
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal	365			
			12MHz crystal	200			
			16MHz crystal	105			
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal	435			
			12MHz crystal	235			
			16MHz crystal	125			
		XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal	495			
			12MHz crystal	270			
			16MHz crystal	145			
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal	305			
			16MHz crystal	160			
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal	380			
			16MHz crystal	205			

Table 36-106. Accuracy characteristics.

Symbol	Parameter	Condition ⁽²⁾		Min.	Typ.	Max.	Units
RES	Resolution	Programmable to 8 or 12 bit		8	12	12	Bits
INL ⁽¹⁾	Integral non-linearity	500ksps	$V_{CC}-1.0V < V_{REF} < V_{CC}-0.6V$		±1.2	±2	lsb
			All V_{REF}		±1.5	±3	
		2000ksps	$V_{CC}-1.0V < V_{REF} < V_{CC}-0.6V$		±1.0	±2	
			All V_{REF}		±1.5	±3	
DNL ⁽¹⁾	Differential non-linearity	guaranteed monotonic			<±0.8	<±1	lsb
	Offset error				-1.0		mV
		Temperature drift			<0.01		mV/K
		Operating voltage drift			<0.6		mV/V
	Gain error	Differential mode	External reference		-1		mV
			$AV_{CC}/1.6$		10		
			$AV_{CC}/2.0$		8.0		
			Bandgap		±5		
		Temperature drift			<0.02		mV/K
		Operating voltage drift			<0.5		mV/V
	Noise	Differential mode, shorted input 2msps, $V_{CC} = 3.6V$, $Clk_{PER} = 16MHz$			0.4		mV rms

Notes: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external V_{REF} is used.

Table 36-107. Gain stage characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_{in}	Input resistance	Switched in normal mode			4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode			4.4		pF
	Signal range	Gain stage output		0		$V_{CC} - 0.6$	V
	Propagation delay	ADC conversion rate			1.0		Clk_{ADC} cycles
	Sample rate	Same as ADC		100		1000	kHz
INL ⁽¹⁾	Integral Non-Linearity	500ksps	All gain settings		±1.5	±4.0	lsb
	Gain error	1x gain, normal mode			-0.8		%
		8x gain, normal mode			-2.5		
		64x gain, normal mode			-3.5		

36.4.14.5 Internal Phase Locked Loop (PLL) characteristics

Table 36-122. Internal PLL characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency ⁽¹⁾	$V_{CC} = 1.6 - 1.8V$	20		48	MHz
		$V_{CC} = 2.7 - 3.6V$	20		128	
	Start-up time			25		μs
	Re-lock time			25		μs

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

36.4.14.6 External clock characteristics

Figure 36-24. External clock drive waveform

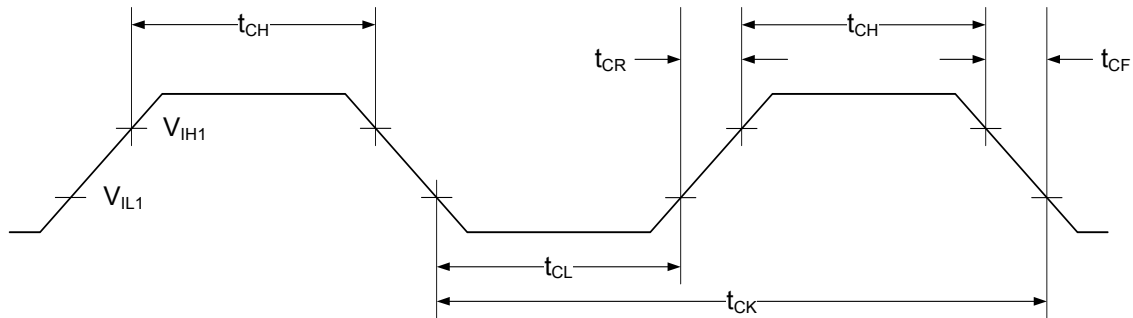


Table 36-123. External clock used as system clock without prescaling.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency ⁽¹⁾	$V_{CC} = 1.6 - 1.8V$	0		12	MHz
		$V_{CC} = 2.7 - 3.6V$	0		32	
t_{CK}	Clock Period	$V_{CC} = 1.6 - 1.8V$	83.3			ns
		$V_{CC} = 2.7 - 3.6V$	31.5			
t_{CH}	Clock High Time	$V_{CC} = 1.6 - 1.8V$	30.0			ns
		$V_{CC} = 2.7 - 3.6V$	12.5			
t_{CL}	Clock Low Time	$V_{CC} = 1.6 - 1.8V$	30.0			ns
		$V_{CC} = 2.7 - 3.6V$	12.5			
t_{CR}	Rise Time (for maximum frequency)	$V_{CC} = 1.6 - 1.8V$			10	ns
		$V_{CC} = 2.7 - 3.6V$			3	
t_{CF}	Fall Time (for maximum frequency)	$V_{CC} = 1.6 - 1.8V$			10	ns
		$V_{CC} = 2.7 - 3.6V$			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

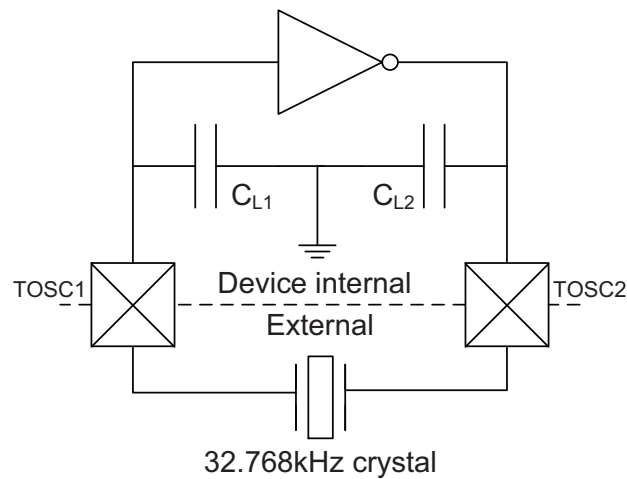
36.4.14.8 External 32.768kHz crystal oscillator and TOSC characteristics

Table 36-126. External 32.768kHz crystal oscillator and TOSC characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
ESR/R1	Recommended crystal equivalent series resistance (ESR)	Crystal load capacitance 6.5pF			60	kΩ
		Crystal load capacitance 9.0pF			35	
C _{TOSC1}	Parasitic capacitance TOSC1 pin			5.4		pF
		Alternate TOSC location		4.0		
C _{TOSC2}	Parasitic capacitance TOSC2 pin			7.1		pF
		Alternate TOSC location		4.0		
	Recommended safety factor	capacitance load matched to crystal specification	3			

Note: 1. See Figure 36-25 for definition.

Figure 36-25. TOSC input capacitance.



The parasitic capacitance between the TOSC pins is $C_{L1} + C_{L2}$ in series as seen from the crystal when oscillating without external capacitors.

37. Typical Characteristics

37.1 ATxmega16A4U

37.1.1 Current consumption

37.1.1.1 Active mode supply current

Figure 37-1. Active supply current vs. frequency.

$f_{\text{SYS}} = 0 - 1\text{MHz}$ external clock, $T = 25^{\circ}\text{C}$.

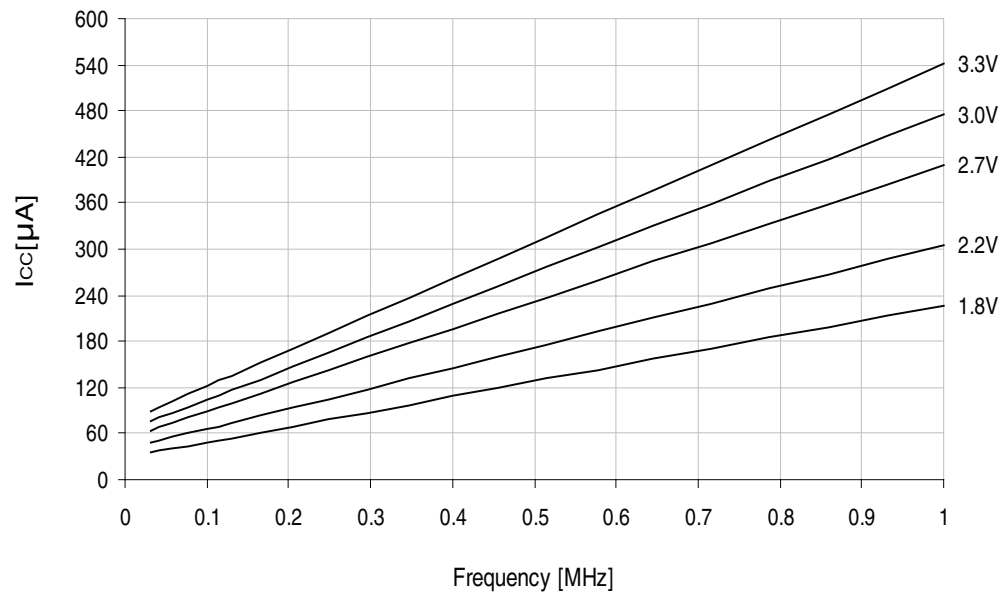


Figure 37-2. Active supply current vs. frequency.

$f_{\text{SYS}} = 1 - 32\text{MHz}$ external clock, $T = 25^{\circ}\text{C}$.

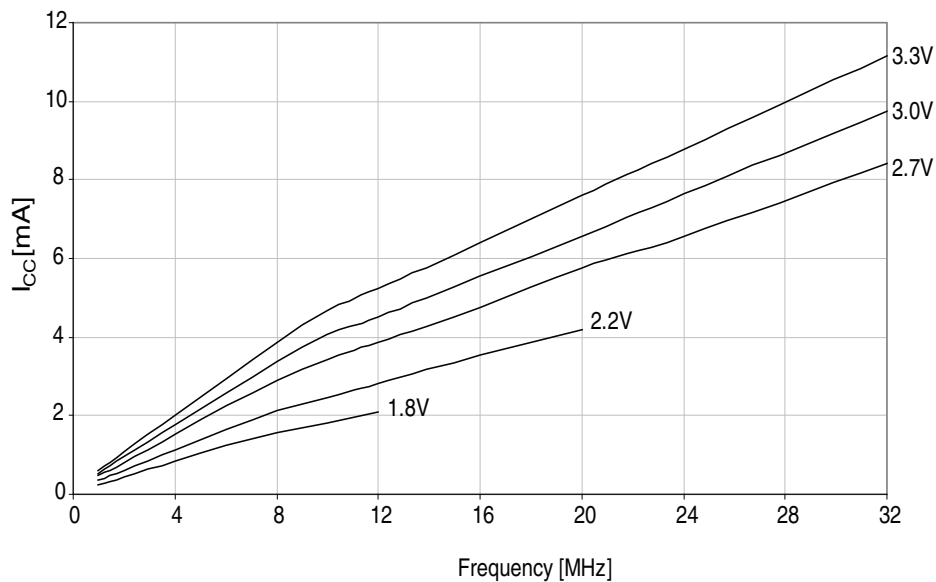


Figure 37-11. Idle mode supply current vs. V_{CC} .

$f_{SYS} = 1\text{MHz}$ external clock.

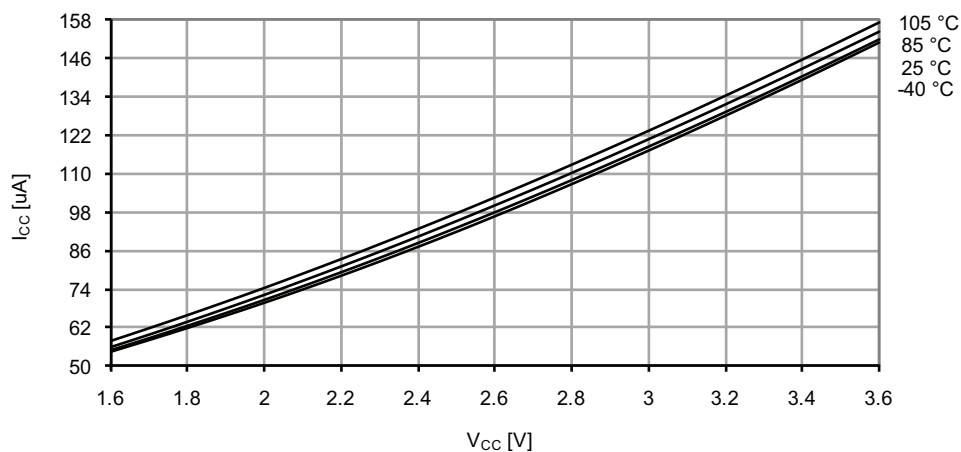


Figure 37-12. Idle mode supply current vs. V_{CC} .

$f_{SYS} = 2\text{MHz}$ internal oscillator.

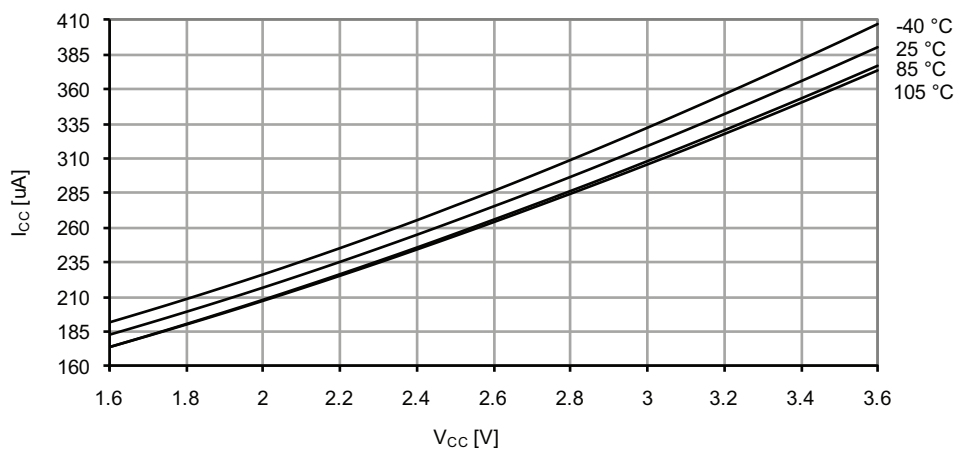


Figure 37-25. I/O pin output voltage vs. source current.

$V_{CC} = 3.0V$.

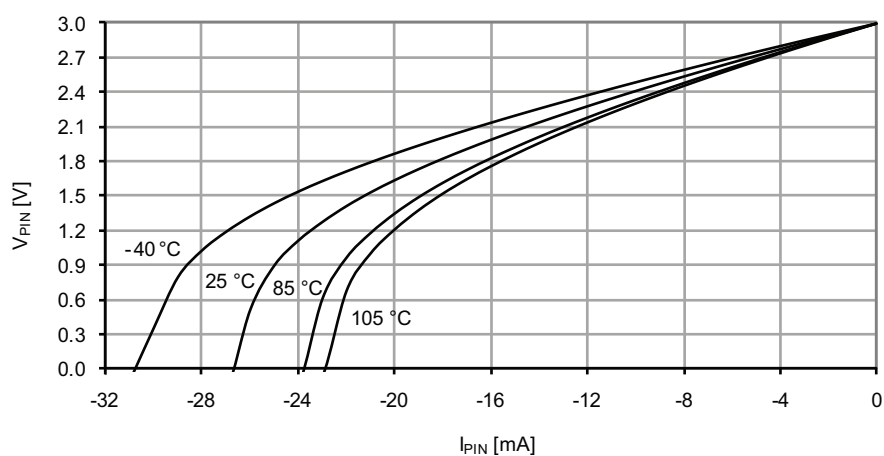


Figure 37-26. I/O pin output voltage vs. source current.

$V_{CC} = 3.3V$.

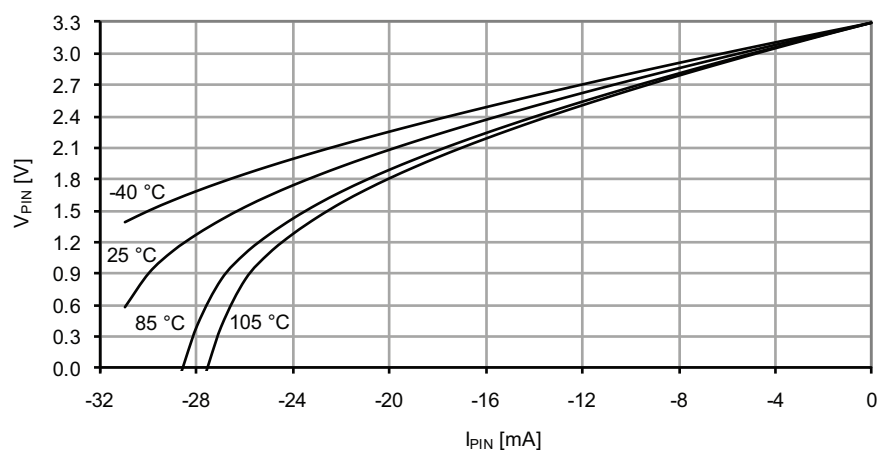


Figure 37-29. I/O pin output voltage vs. sink current.

$V_{CC} = 3.0V$.

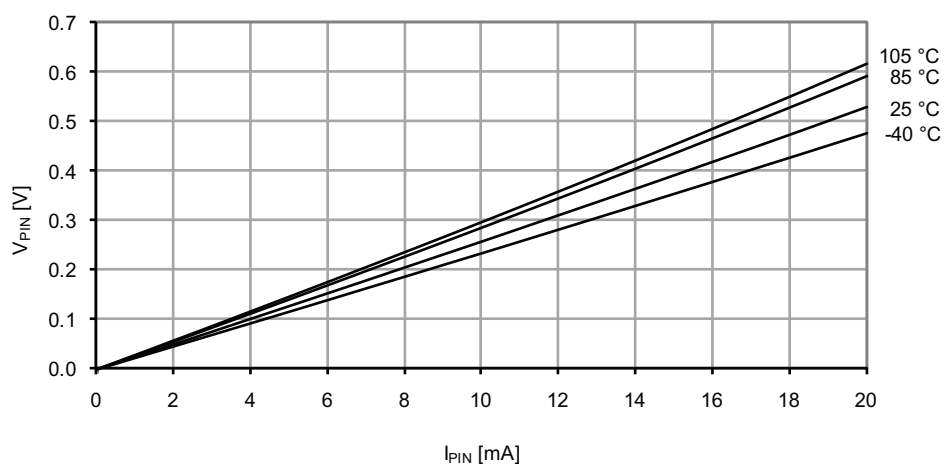


Figure 37-30. I/O pin output voltage vs. sink current.

$V_{CC} = 3.3V$.

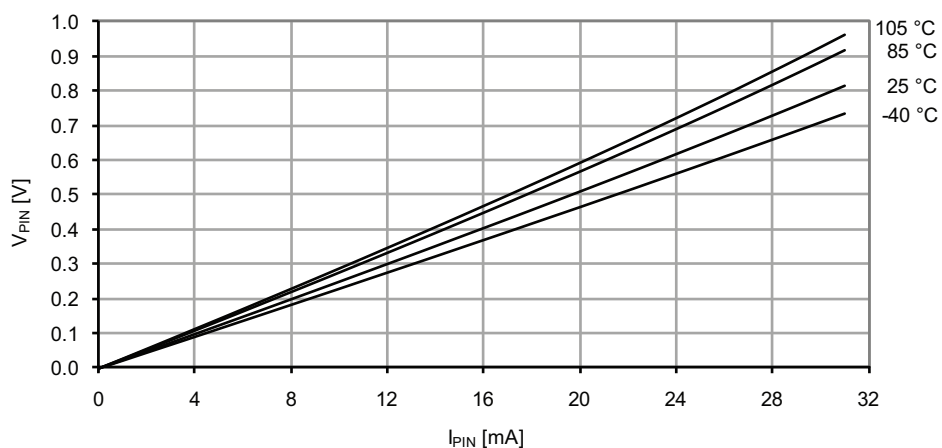


Figure 37-31. I/O pin output voltage vs. sink current.

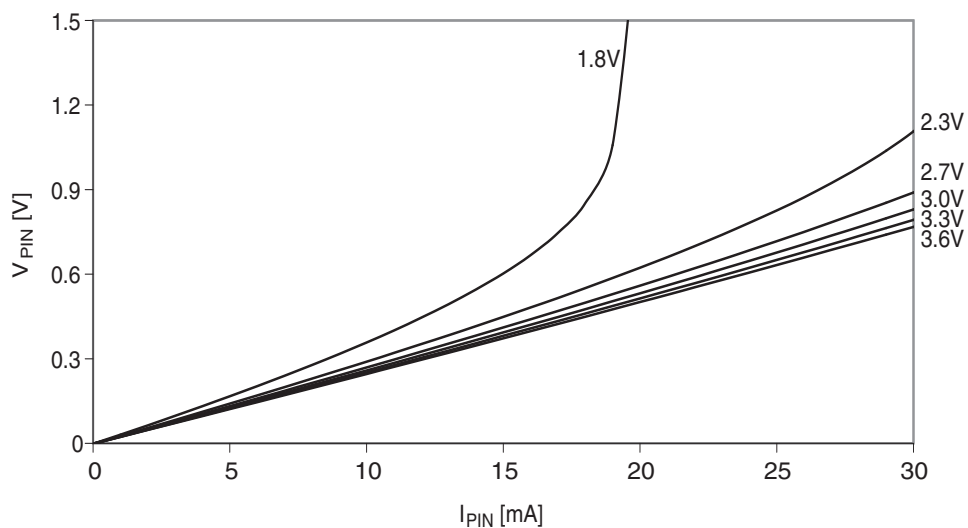


Figure 37-56. Analog comparator current source vs. calibration value.

Temperature = 25°C.

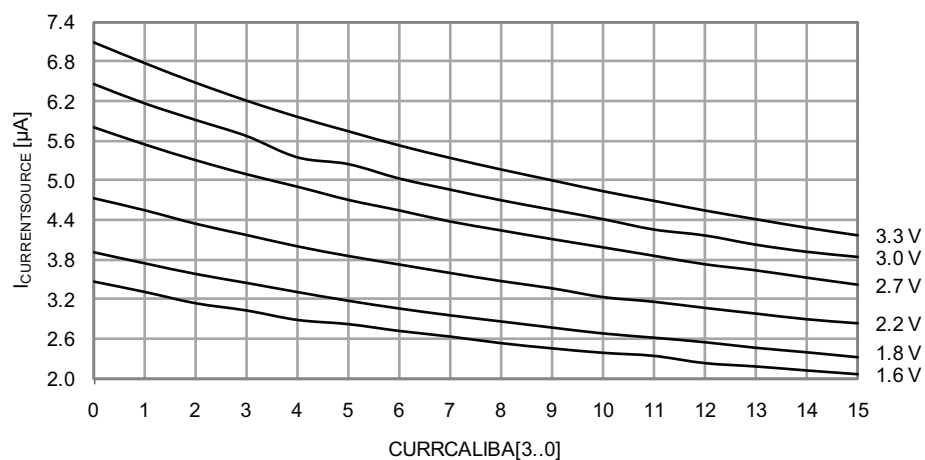


Figure 37-57. Analog comparator current source vs. calibration value.

V_{CC} = 3.0V.

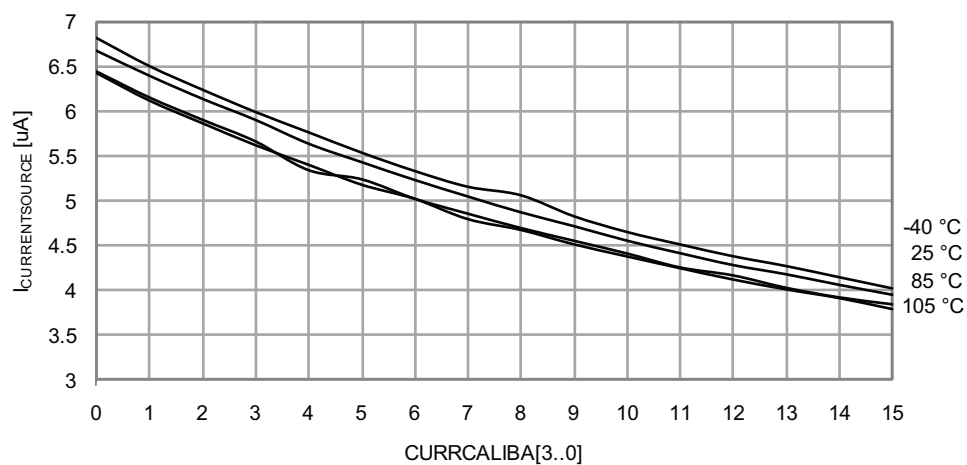


Figure 37-177. Idle mode supply current vs. frequency.

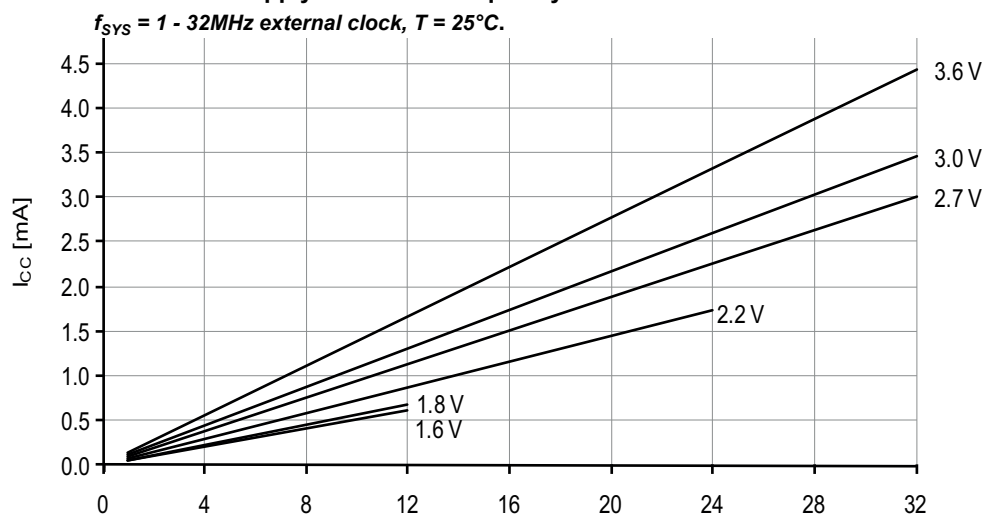


Figure 37-178. Idle mode supply current vs. V_{CC} .

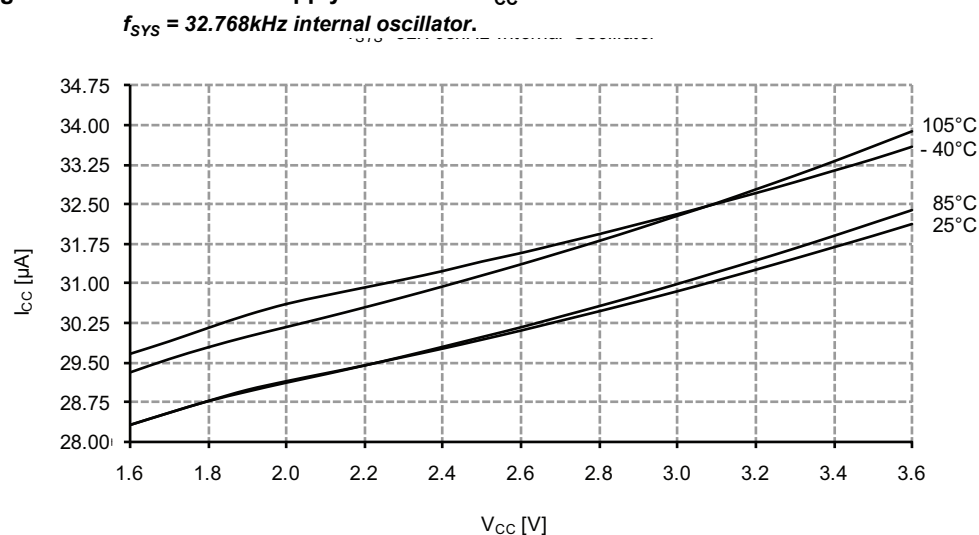


Figure 37-231. Reset pin pull-up resistor current vs. reset pin voltage.

$V_{CC} = 1.8V$.

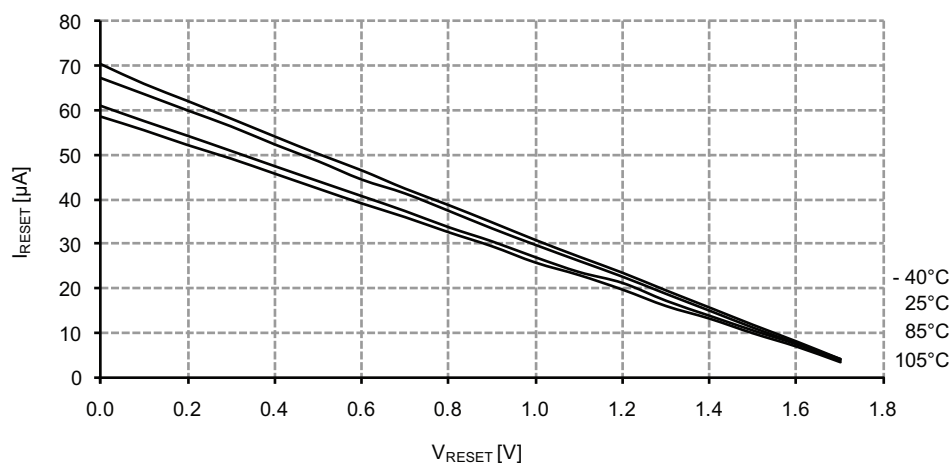


Figure 37-232. Reset pin pull-up resistor current vs. reset pin voltage.

$V_{CC} = 3.0V$.

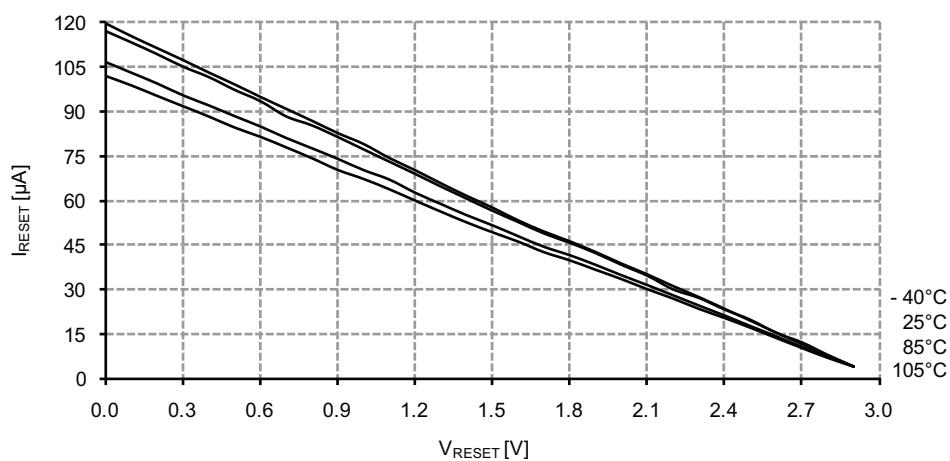


Figure 37-233. Reset pin pull-up resistor current vs. reset pin voltage.

$V_{CC} = 3.3V$.

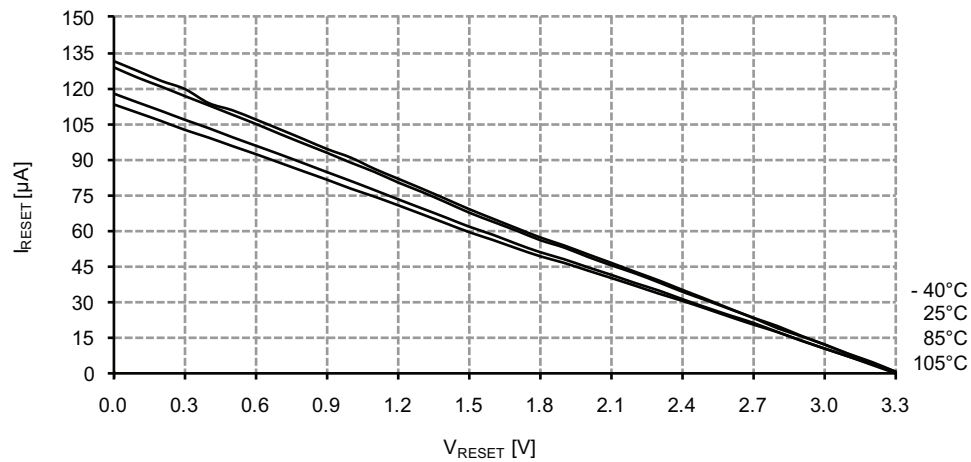


Figure 37-234. Reset pin input threshold voltage vs. V_{CC} .

V_{IH} - Reset pin read as "1".

