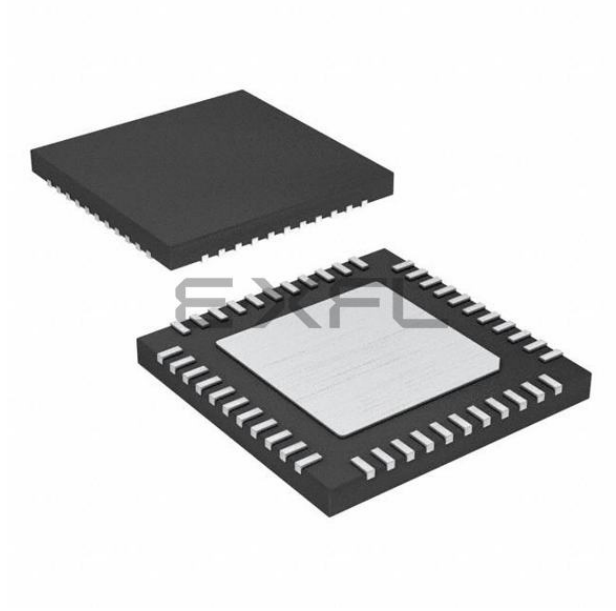

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What is "Embedded - Microcontrollers"?

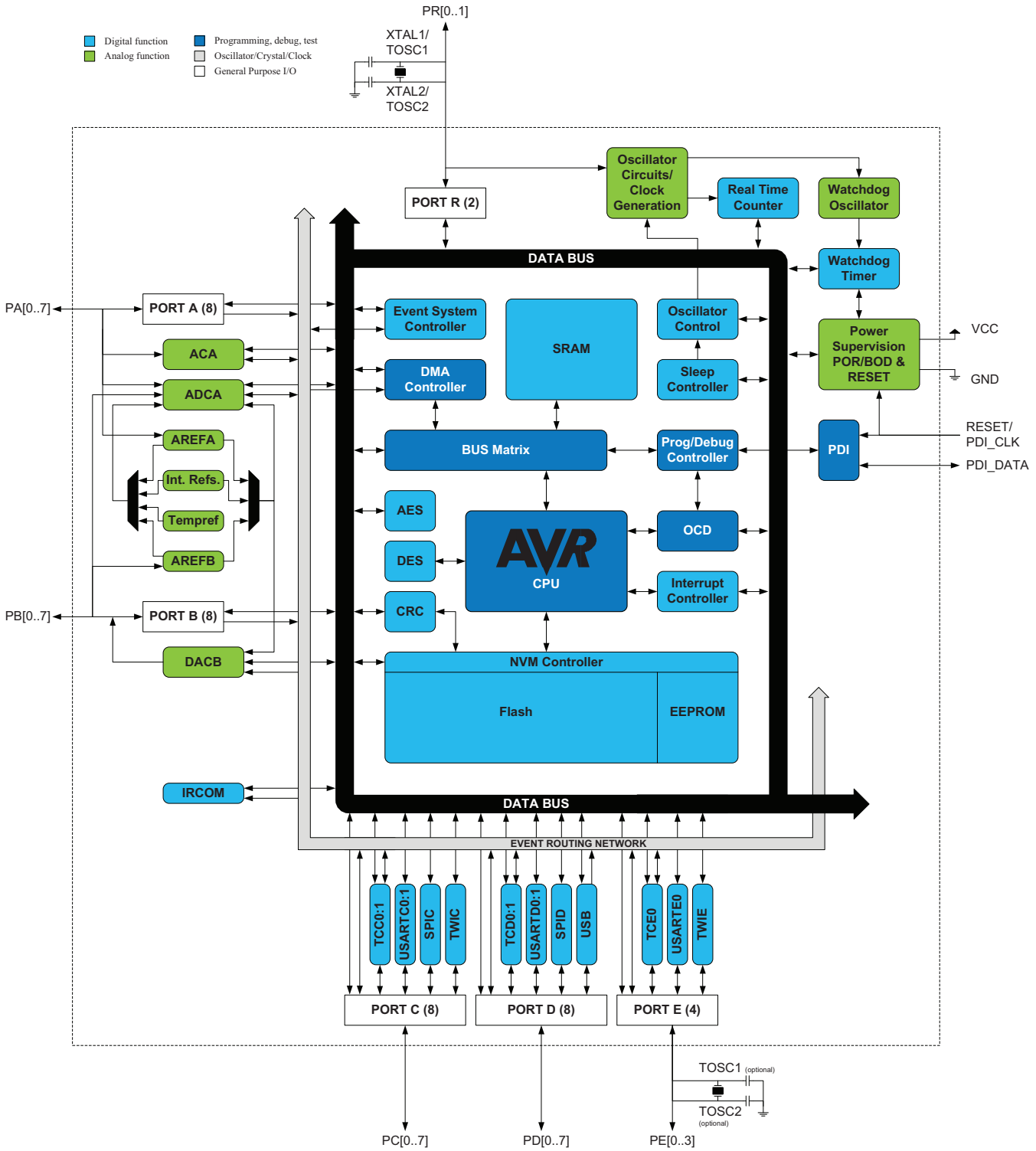
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32a4u-mn

3.1 Block Diagram

Figure 3-1. XMEGA A4U Block Diagram



13. WDT – Watchdog Timer

13.1 Features

- Issues a device reset if the timer is not reset before its timeout period
- Asynchronous operation from dedicated oscillator
- 1kHz output of the 32kHz ultra low power oscillator
- 11 selectable timeout periods, from 8ms to 8s
- Two operation modes:
  - Normal mode
  - Window mode
- Configuration lock to prevent unwanted changes

13.2 Overview

The watchdog timer (WDT) is a system function for monitoring correct program operation. It makes it possible to recover from error situations such as runaway or deadlocked code. The WDT is a timer, configured to a predefined timeout period, and is constantly running when enabled. If the WDT is not reset within the timeout period, it will issue a microcontroller reset. The WDT is reset by executing the WDR (watchdog timer reset) instruction from the application code.

The window mode makes it possible to define a time slot or window inside the total timeout period during which WDT must be reset. If the WDT is reset outside this window, either too early or too late, a system reset will be issued. Compared to the normal mode, this can also catch situations where a code error causes constant WDR execution.

The WDT will run in active mode and all sleep modes, if enabled. It is asynchronous, runs from a CPU-independent clock source, and will continue to operate to issue a system reset even if the main clocks fail.

The configuration change protection mechanism ensures that the WDT settings cannot be changed by accident. For increased safety, a fuse for locking the WDT settings is also available.

26. AES and DES Crypto Engine

26.1 Features

- Data Encryption Standard (DES) CPU instruction
- Advanced Encryption Standard (AES) crypto module
- DES Instruction
  - Encryption and decryption
  - DES supported
  - Encryption/decryption in 16 CPU clock cycles per 8-byte block
- AES crypto module
  - Encryption and decryption
  - Supports 128-bit keys
  - Supports XOR data load mode to the state memory
  - Encryption/decryption in 375 clock cycles per 16-byte block

26.2 Overview

The Advanced Encryption Standard (AES) and Data Encryption Standard (DES) are two commonly used standards for cryptography. These are supported through an AES peripheral module and a DES CPU instruction, and the communication interfaces and the CPU can use these for fast, encrypted communication and secure data storage.

DES is supported by an instruction in the AVR CPU. The 8-byte key and 8-byte data blocks must be loaded into the register file, and then the DES instruction must be executed 16 times to encrypt/decrypt the data block.

The AES crypto module encrypts and decrypts 128-bit data blocks with the use of a 128-bit key. The key and data must be loaded into the key and state memory in the module before encryption/decryption is started. It takes 375 peripheral clock cycles before the encryption/decryption is done. The encrypted/encrypted data can then be read out, and an optional interrupt can be generated. The AES crypto module also has DMA support with transfer triggers when encryption/decryption is done and optional auto-start of encryption/decryption when the state memory is fully loaded.

29. DAC – 12-bit Digital to Analog Converter

29.1 Features

- One Digital to Analog Converter (DAC)
- 12-bit resolution
- Two independent, continuous-drive output channels
- Up to one million samples per second conversion rate per DAC channel
- Built-in calibration that removes:
  - Offset error
  - Gain error
- Multiple conversion trigger sources
  - On new available data
  - Events from the event system
- High drive capabilities and support for
  - Resistive loads
  - Capacitive loads
  - Combined resistive and capacitive loads
- Internal and external reference options
- DAC output available as input to analog comparator and ADC
- Low-power mode, with reduced drive strength
- Optional DMA transfer of data

29.2 Overview

The digital-to-analog converter (DAC) converts digital values to voltages. The DAC has two channels, each with 12-bit resolution, and is capable of converting up to one million samples per second (msps) on each channel. The built-in calibration system can remove offset and gain error when loaded with calibration values from software.

Figure 29-1. DAC overview.

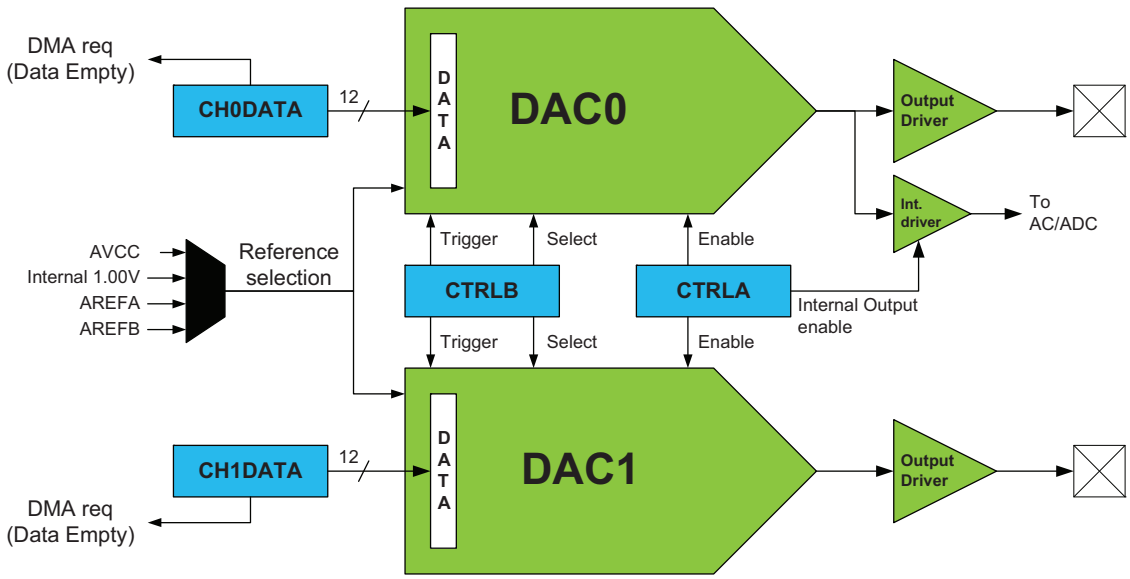


Table 36-10. Accuracy characteristics.

Symbol	Parameter	Condition [2]		Min.	Typ.	Max.	Units
RES	Resolution	Programmable to 8 or 12 bit		8	12	12	Bits
INL [1]	Integral non-linearity	500ksps	V_{CC}-1.0V < V_{REF}< V_{CC}-0.6V		±1.2	±2.0	lsb
			All V_{REF}		±1.5	±3.0	
		2000ksps	V_{CC}-1.0V < V_{REF}< V_{CC}-0.6V		±1.0	±2.0	
			All V_{REF}		±1.5	±3.0	
DNL [1]	Differential non-linearity	guaranteed monotonic			<±0.8	<±1.0	lsb
	Offset error				-1.0		mV
		Temperature drift			<0.01		mV/K
		Operating voltage drift			<0.6		mV/V
	Gain error	Differential mode	External reference		-1.0		mV
			AV_{CC}/1.6		10		
			AV_{CC}/2.0		8.0		
			Bandgap		±5.0		
		Temperature drift			<0.02		mV/K
		Operating voltage drift			<0.5		mV/V
	Noise	Differential mode, shorted input 2msps, V_{CC} = 3.6V, Clk_{PER} = 16MHz			0.4		mV rms

Notes:
1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external V_{REF} is used.

Table 36-11. Gain stage characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_{in}	Input resistance	Switched in normal mode			4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode			4.4		pF
	Signal range	Gain stage output		0		V_{CC}- 0.6	V
	Propagation delay	ADC conversion rate			1.0		Clk_{ADC} cycles
	Sample rate	Same as ADC		100		1000	kHz
INL [1]	Integral non-linearity	500ksps	All gain settings		±1.5	±4	lsb
	Gain error	1x gain, normal mode			-0.8		%
		8x gain, normal mode			-2.5		
		64x gain, normal mode			-3.5		

Table 36-78. Accuracy characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
RES	Input resolution					12	Bits
INL [1]	Integral non-linearity	V_{REF}= Ext 1.0V	V_{CC} = 1.6V		±2.0	±3.0	lsb
			V_{CC} = 3.6V		±1.5	±2.5	
		V_{REF}=AV_{CC}	V_{CC} = 1.6V		±2.0	±4.0	
			V_{CC} = 3.6V		±1.5	±4.0	
		V_{REF}=INT1V	V_{CC} = 1.6V		±5.0		
			V_{CC} = 3.6V		±5.0		
DNL [1]	Differential non-linearity	V_{REF}=Ext 1.0V	V_{CC} = 1.6V		±1.5	3.0	lsb
			V_{CC} = 3.6V		±0.6	1.5	
		V_{REF}=AV_{CC}	V_{CC} = 1.6V		±1.0	3.5	
			V_{CC} = 3.6V		±0.6	1.5	
		V_{REF}=INT1V	V_{CC} = 1.6V		±4.5		
			V_{CC} = 3.6V		±4.5		
	Gain error	After calibration			<4.0		lsb
	Gain calibration step size				4.0		lsb
	Gain calibration drift	V_{REF}= Ext 1.0V			<0.2		mV/K
	Offset error	After calibration			<1.0		lsb
	Offset calibration step size				1.0		

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% output voltage range.

36.4.16 Two-Wire Interface Characteristics

Table 36-128 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 36-28.

Figure 36-28. Two-wire interface bus timing.

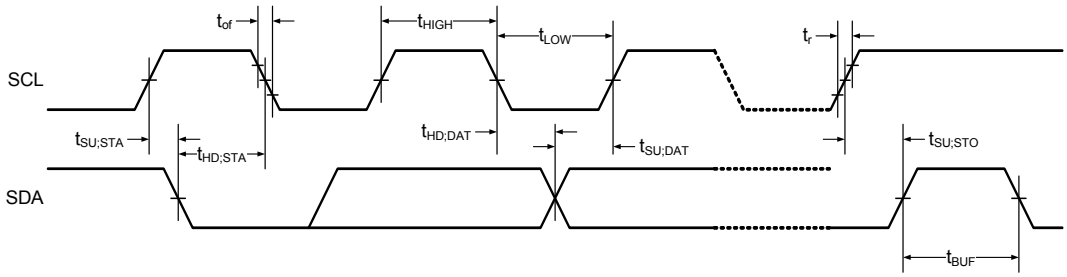


Table 36-128. Two-wire interface characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage		$0.7V_{CC}$		V_{CC}+0.5	V
V_{IL}	Input Low Voltage		0.5		$0.3\times V_{CC}$	V
V_{hys}	Hysteresis of Schmitt Trigger Inputs		$0.05V_{CC}$ (1)			V
V_{OL}	Output Low Voltage	3mA, sink current	0		0.4	V
t_r	Rise Time for both SDA and SCL		$20+0.1C_b$ (1)(2)		300	ns
t_{of}	Output Fall Time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF$ (2)	$20+0.1C_b$ (1)(2)		250	ns
t_{SP}	Spikes Suppressed by Input Filter		0		50	ns
I_I	Input Current for each I/O Pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	µA
C_I	Capacitance for each I/O Pin				10	pF
f_{SCL}	SCL Clock Frequency	f_{PER} (3)>max($10f_{SCL}$, 250kHz)	0		400	kHz
R_P	Value of Pull-up resistor	$f_{SCL} \le 100kHz$	$\frac{V_{CC}-0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		$f_{SCL} > 100kHz$			$\frac{300ns}{C_b}$	
$t_{HD;STA}$	Hold Time (repeated) START condition	$f_{SCL} \le 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
t_{LOW}	Low Period of SCL Clock	$f_{SCL} \le 100kHz$	4.7			µs
		$f_{SCL} > 100kHz$	1.3			
t_{HIGH}	High Period of SCL Clock	$f_{SCL} \le 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \le 100kHz$	4.7			µs
		$f_{SCL} > 100kHz$	0.6			

Figure 37-66. Reset pin input threshold voltage vs. V_{CC}.

V_{IH} - Reset pin read as "1".

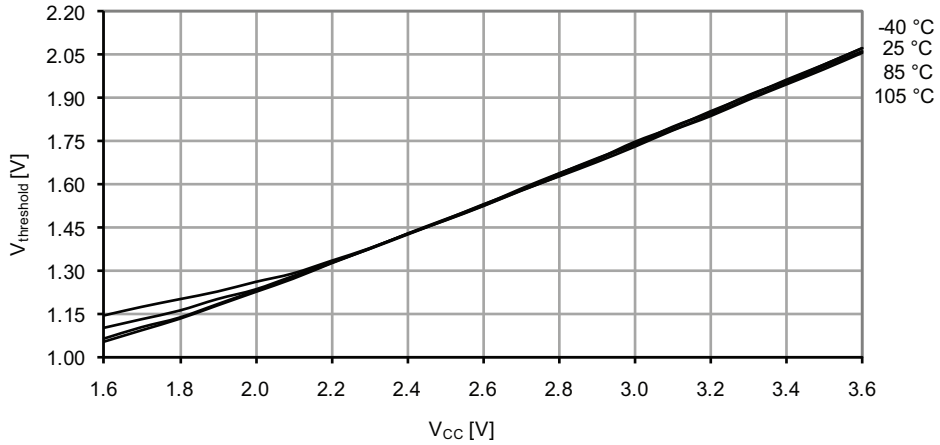


Figure 37-67. Reset pin input threshold voltage vs. V_{CC}.

V_{IL} - Reset pin read as "0".

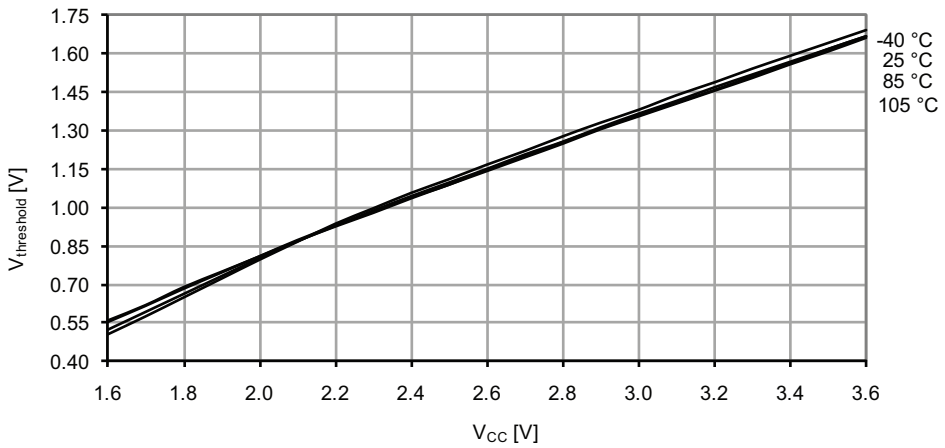


Figure 37-78. 32MHz internal oscillator CALA calibration step size.

V_{CC} = 3.0V.

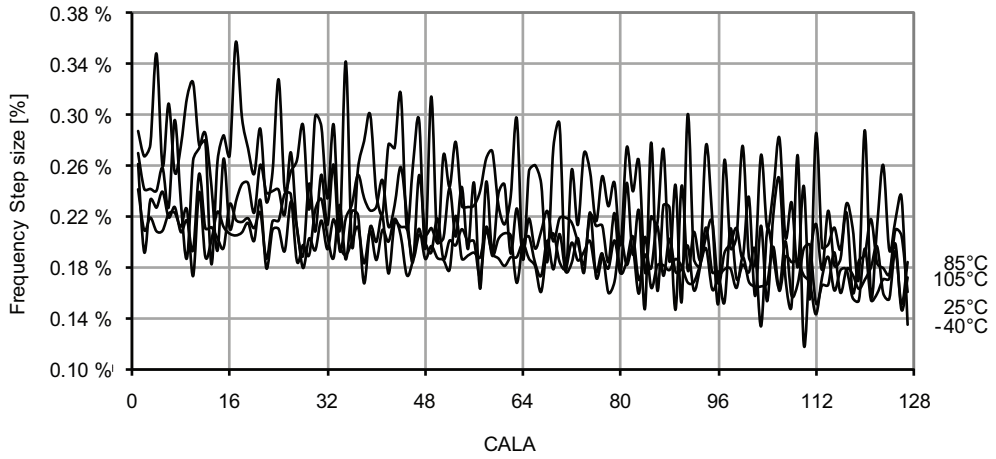
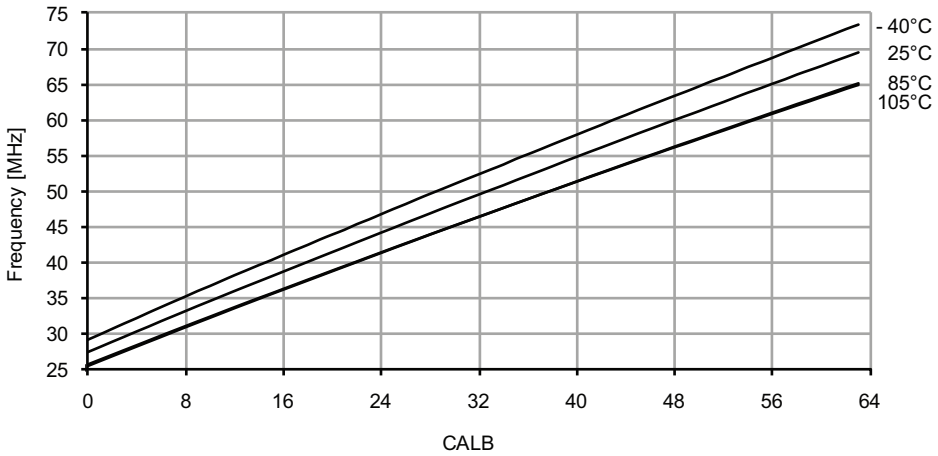


Figure 37-79. 32MHz internal oscillator frequency vs. CALB calibration value.

V_{CC} = 3.0V.



37.1.10.5 32MHz internal oscillator calibrated to 48MHz

Figure 37-80. 48MHz internal oscillator frequency vs. temperature.

DFLL disabled.

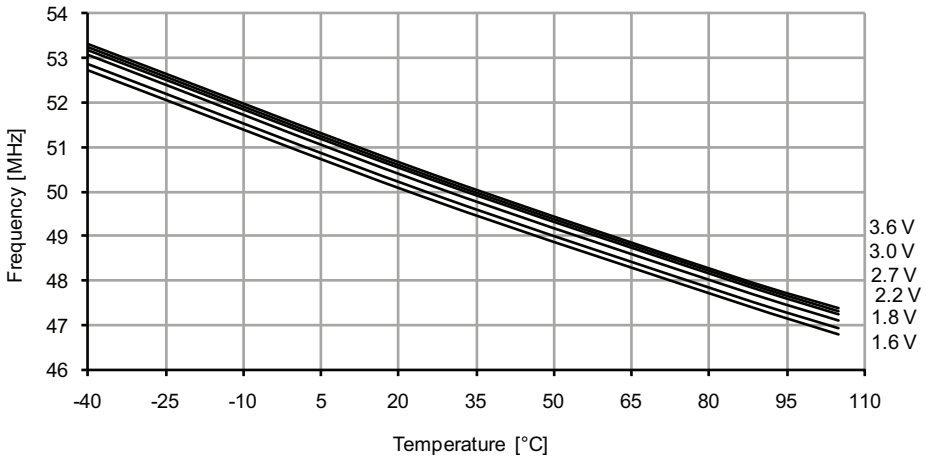
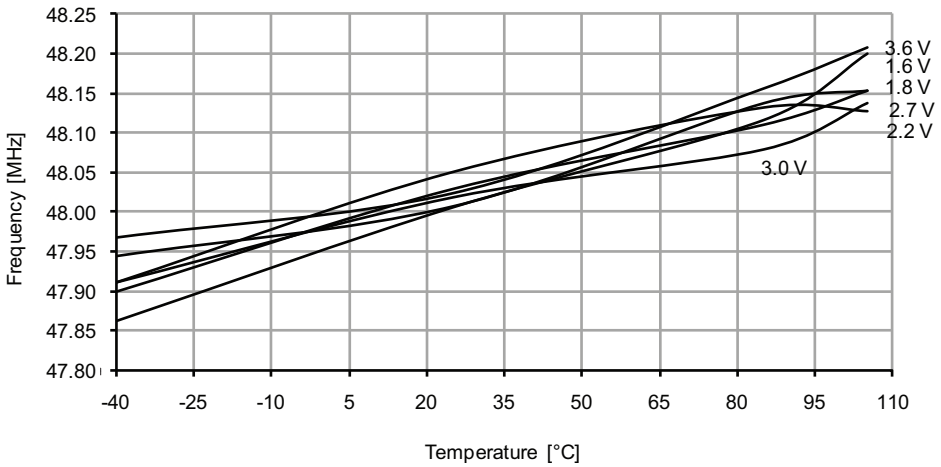


Figure 37-81. 48MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator.



37.2.9 Power-on Reset Characteristics

Figure 37-152. Power-on reset current consumption vs. V_{CC}.

BOD level = 3.0V, enabled in continuous mode.

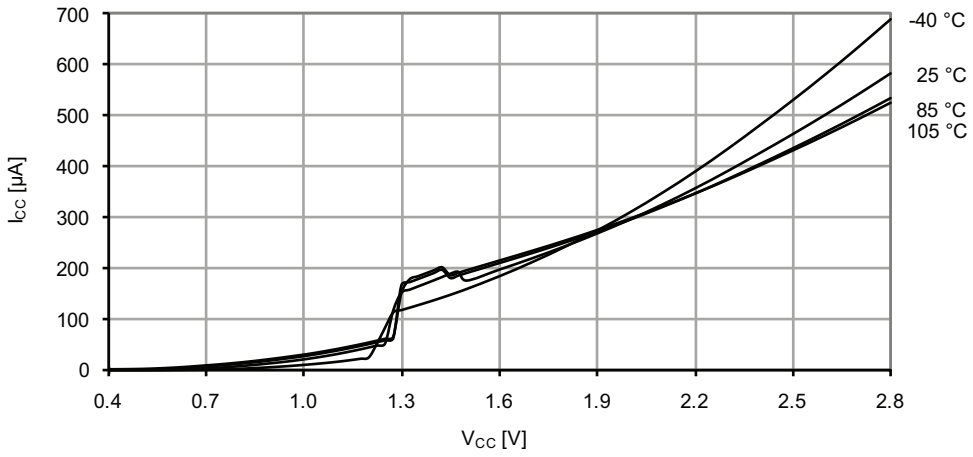


Figure 37-153. Power-on reset current consumption vs. V_{CC}.

BOD level = 3.0V, enabled in sampled mode.

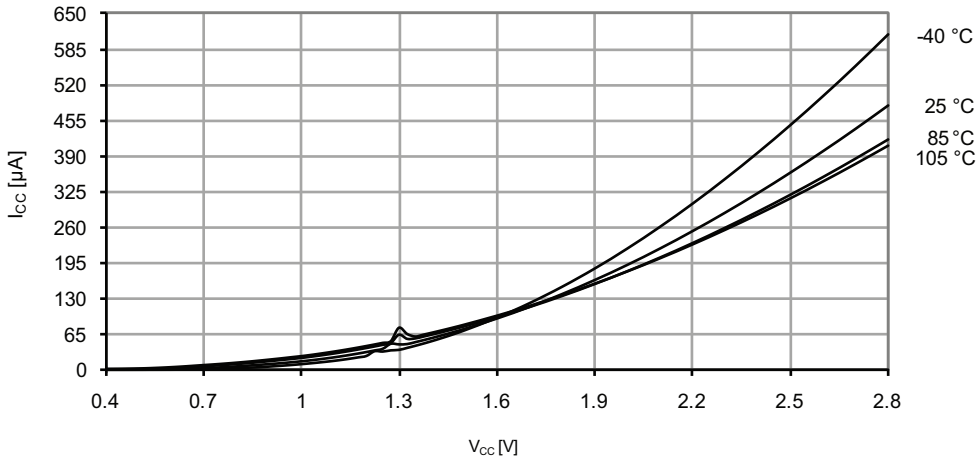


Figure 37-158. 2MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator .

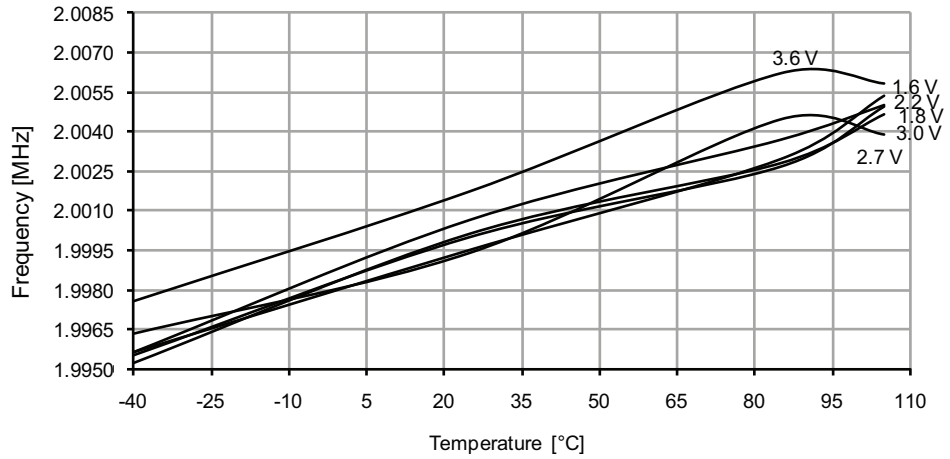


Figure 37-159. 2MHz internal oscillator CALA calibration step size.

V_{CC} = 3V.

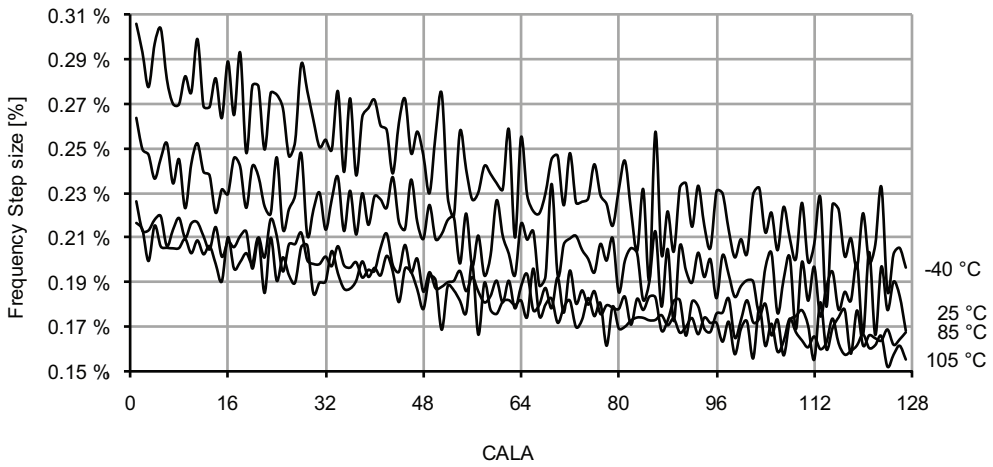


Figure 37-225. Analog comparator current source vs. calibration value.

V_{CC} = 3.0V.

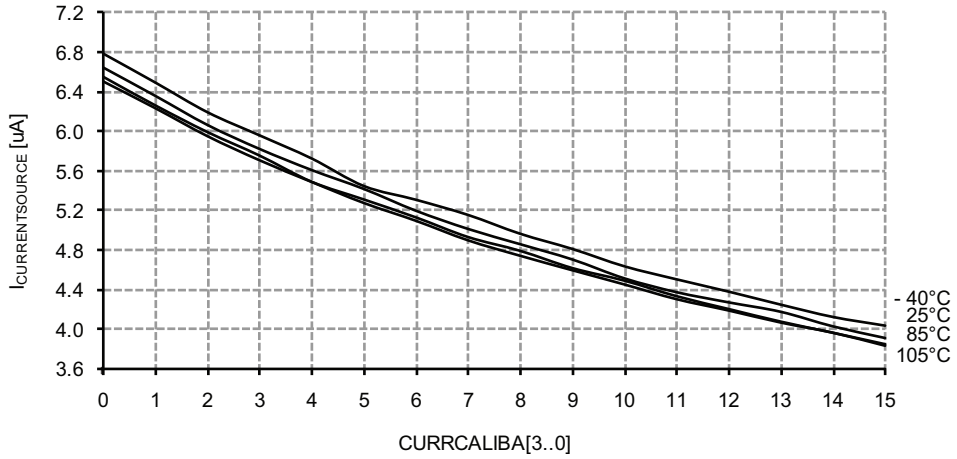


Figure 37-226. Voltage scaler INL vs. SCALEFAC.

T = 25°C, V_{CC} = 3.0V.

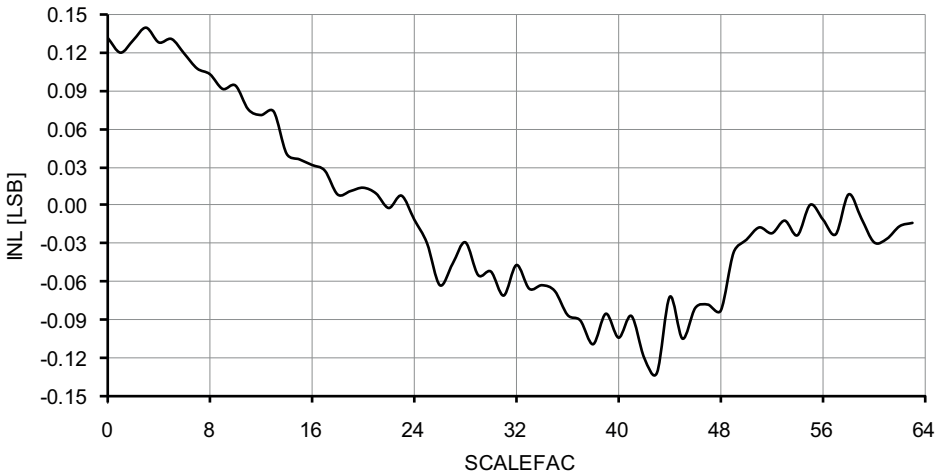
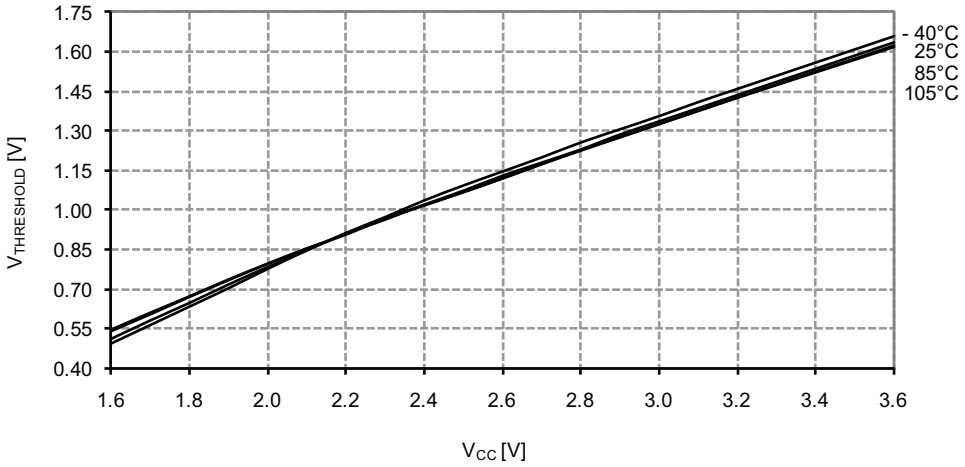


Figure 37-235. Reset pin input threshold voltage vs. V_{CC}.

V_{IL} - Reset pin read as "0".



37.3.9 Power-on Reset Characteristics

Figure 37-236. Power-on reset current consumption vs. V_{CC}.

BOD level = 3.0V, enabled in continuous mode.

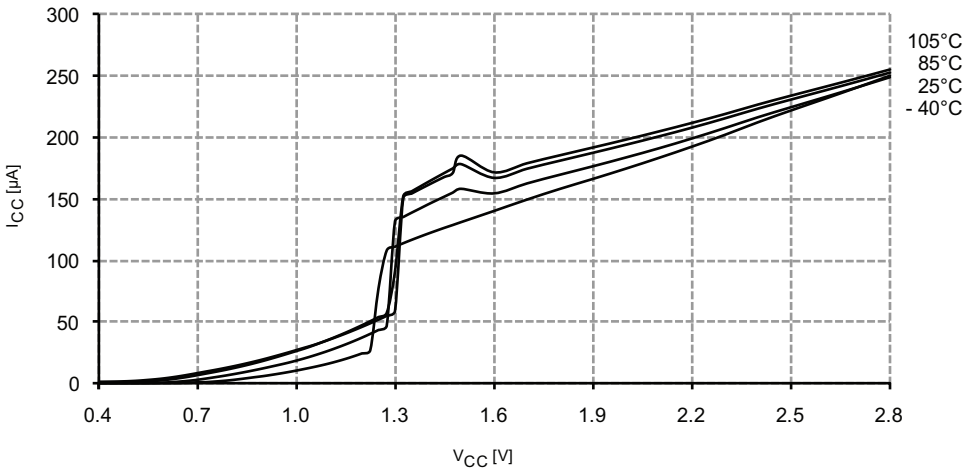


Figure 37-245. 32MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator.

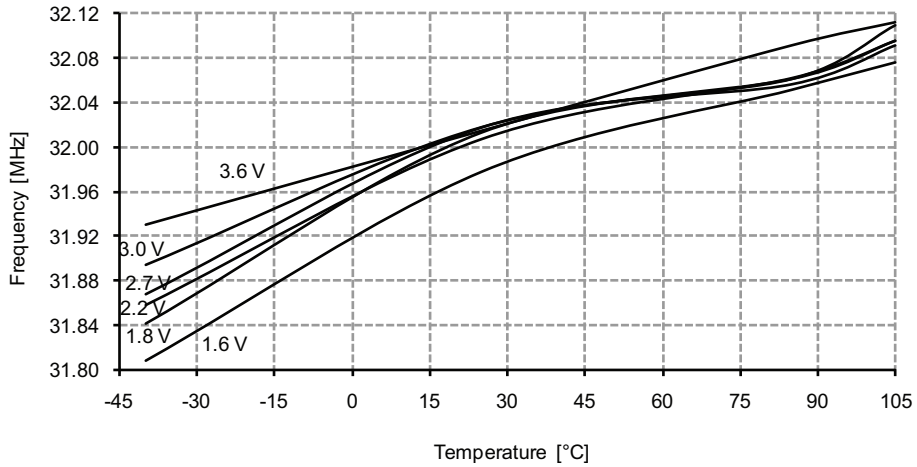
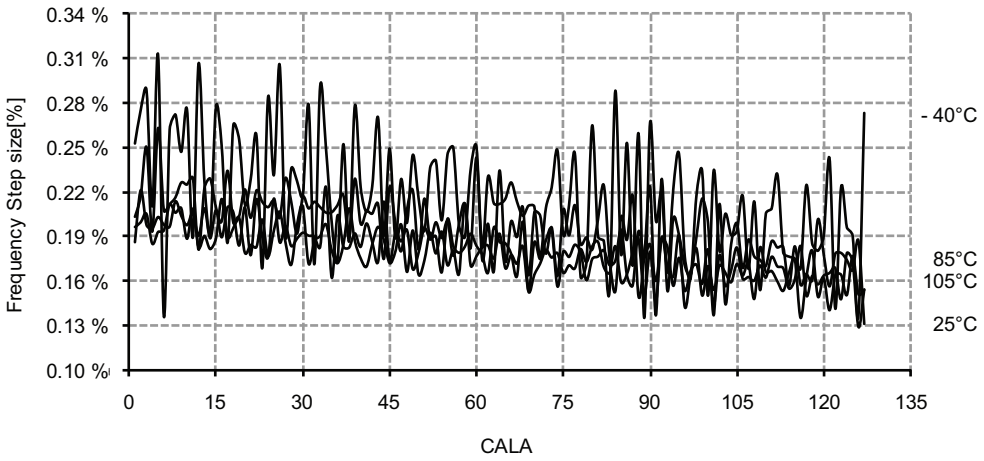


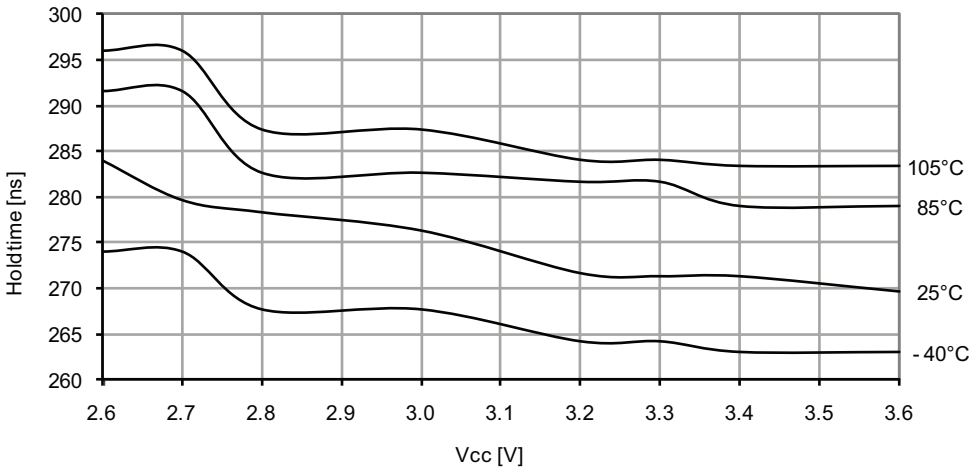
Figure 37-246. 32MHz internal oscillator CALA calibration step size.

V_{CC} = 3.0V.



37.3.11 Two-Wire Interface characteristics

Figure 37-251. SDA hold time vs. supply voltage.



37.3.12 PDI characteristics

Figure 37-252. Maximum PDI frequency vs. V_{CC}.

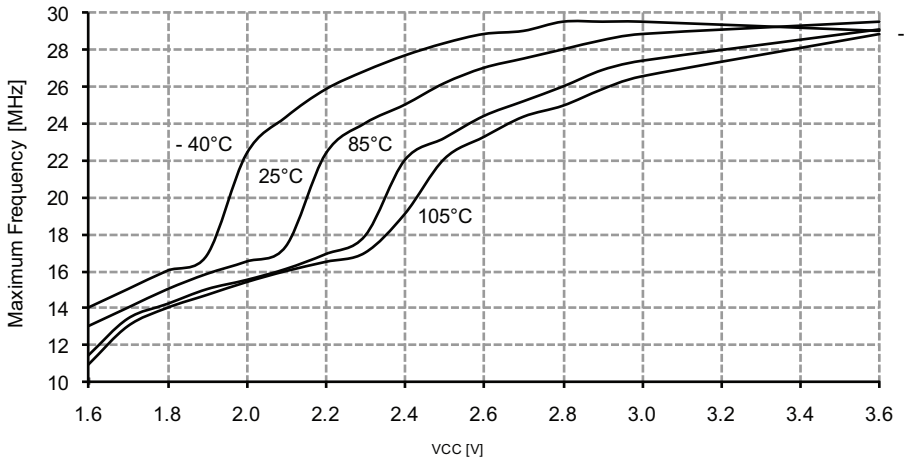


Figure 37-255. Active mode supply current vs. V_{CC}.

f_{SYS} = 32.768kHz internal oscillator

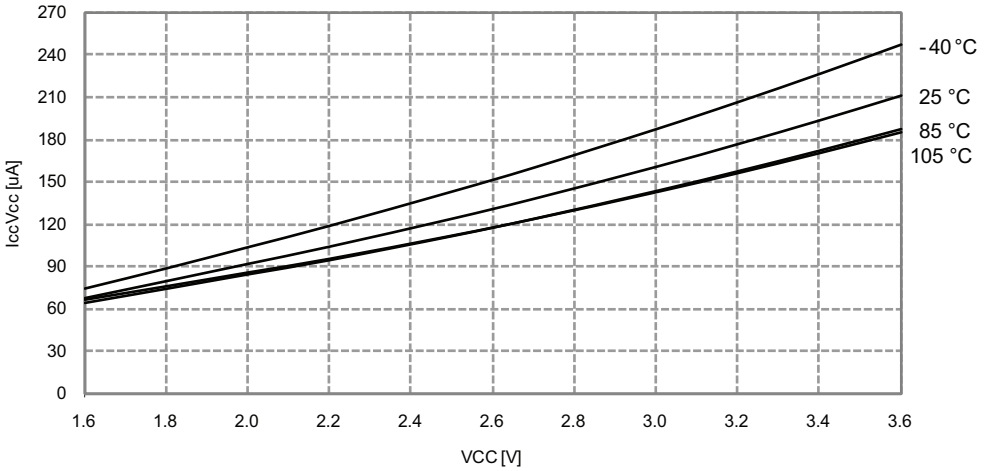


Figure 37-256. Active mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

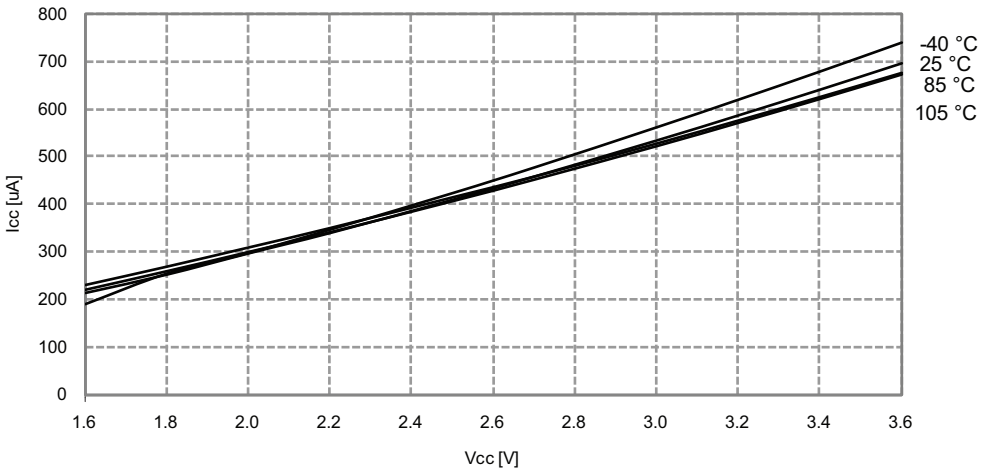


Figure 37-281. I/O pin output voltage vs. sink current.

V_{CC} = 3.0V

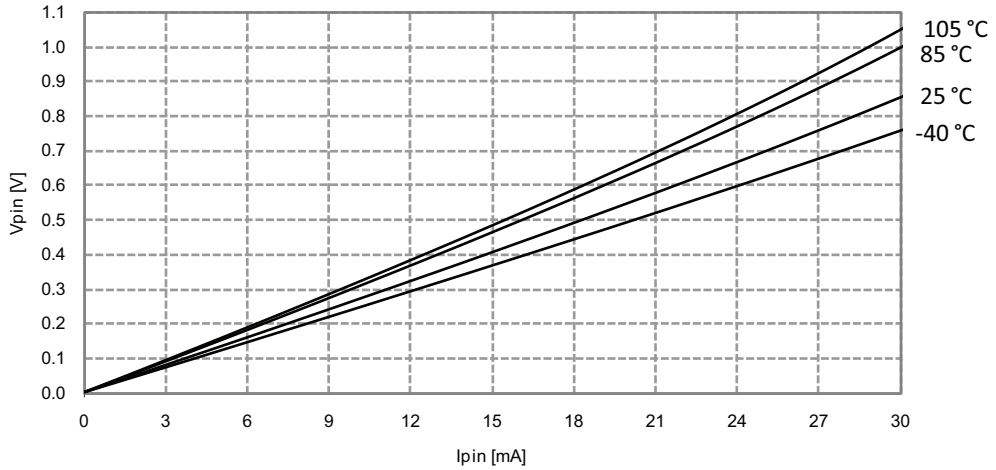


Figure 37-282. I/O pin output voltage vs. sink current.

V_{CC} = 3.3V

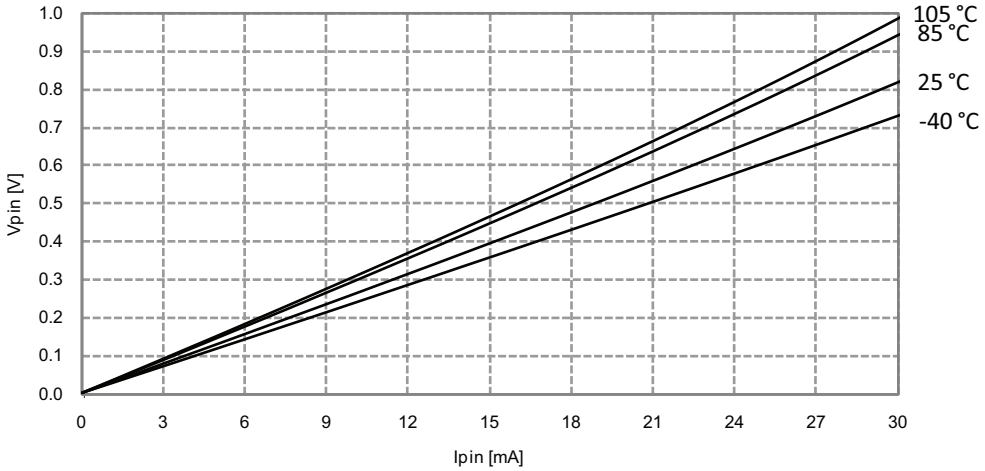


Figure 37-297. Gain error vs. temperature

V_{CC} = 3.0V, V_{REF} = external 2.0V

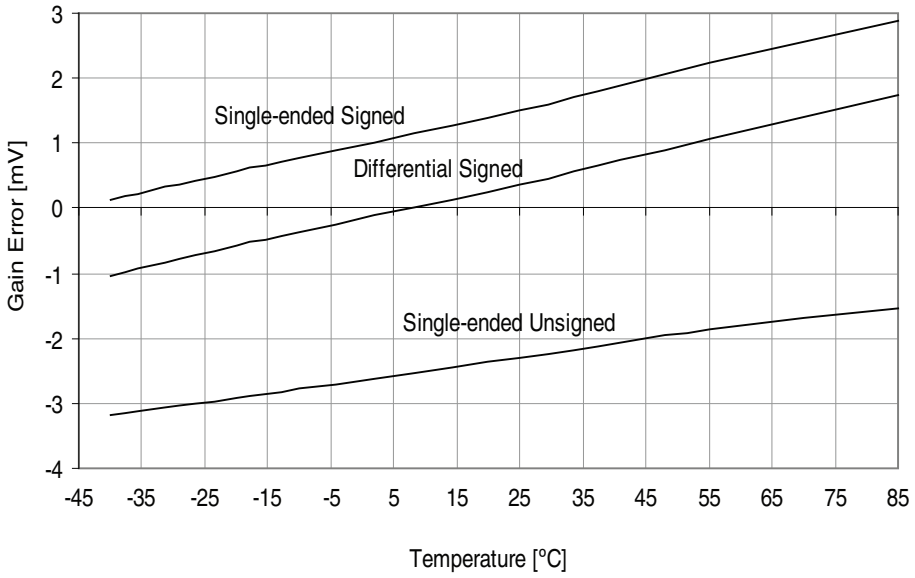
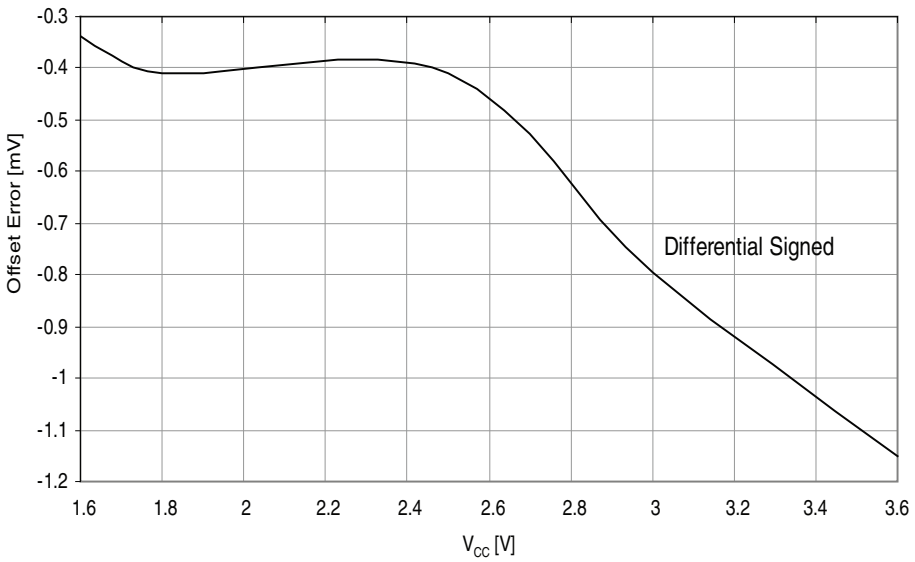


Figure 37-298. Offset error vs. V_{CC}

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps



5.	Updated all typical characteristics in “Power-down mode supply current” on page 166.
6.	Added electrical characteristics for “ATxmega32A4U” on page 93.
7.	Added electrical characteristics for “ATxmega64A4U” on page 115.
8.	Added electrical characteristics for “ATxmega128A4U” on page 137.
9.	Added typical characteristics for “ATxmega64A4U” on page 243
10.	Added typical characteristics for “ATxmega64A4U” on page 243.
12.	Added typical characteristics for “ATxmega128A4U” on page 285.
13.	Updated “Errata” on page 327.
14.	Used Atmel new datasheet template that includes Atmel new addresses on the last page.

39.7 8387B – 12/2011

1.	Updated Figure 2-1 on page 4: “Block Diagram and QFN/TQFP pinout”
2.	Updated Figure 3-1 on page 7: “XMEGA A4U Block Diagram”
3.	Updated “Overview” on page 13.
4.	Updated “ADC – 12-bit Analog to Digital Converter” on page 49.
5.	Updated Figure 28-1 on page 50: “ADC overview.”
6.	Updated “Instruction Set Summary” on page 63.
7.	Updated “Electrical Characteristics” on page 72.
8.	Updated “Typical Characteristics” on page 159.
9.	The order of several figures in the chapter “Typical Characteristics” has been changed
10.	Several new figures have been added to and some figures have been removed from chapter “Typical Characteristics”
11.	Several minor changes/corrections in text and figures have been performed
12.	Table 32-2 on page 59 has been corrected
13.	Table 32-4 on page 60 has been corrected
14.	Table 36-29 on page 85 has been corrected
15.	Table 36-30 on page 86 has been corrected
16.	The heading ”I/O Pin Characteristics” on page 164 has been corrected (the text “and Reset” has been removed)

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1.	Initial revision.