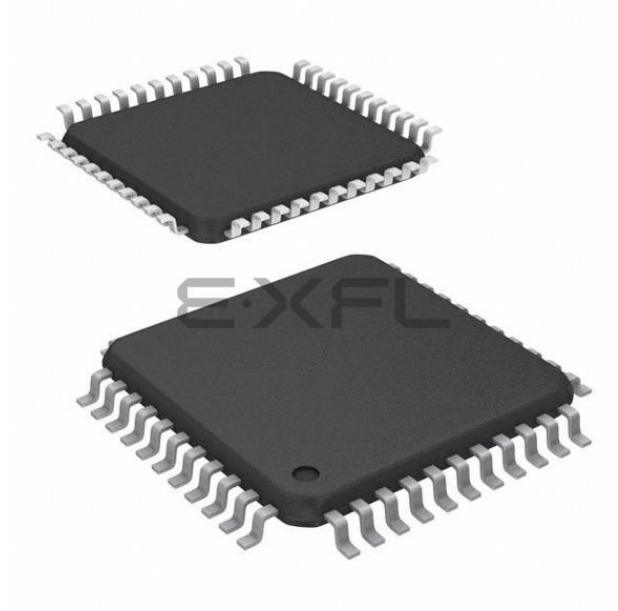

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64a4u-an

Ordering code	Flash (bytes)	EEPROM (bytes)	SRAM (bytes)	Speed (MHz)	Power supply	Package [1][2][3]	Temp.
ATxmega128A4U-AN	128K + 8K	2K	8K	32	1.6 - 3.6V	44A	0°C - 105°C
ATxmega128A4U-ANR[4]	128K + 8K	2K	8K				
ATxmega64A4U-AN	64K + 4K	2K	4K				
ATxmega64A4U-ANR[4]	64K + 4K	2K	4K				
ATxmega32A4U-AN	32K + 4K	1K	4K				
ATxmega32A4U-ANR[4]	32K + 4K	1K	4K				
ATxmega16A4U-AN	16K + 4K	1K	2K				
ATxmega16A4U-ANR[4]	16K + 4K	1K	2K				
ATxmega128A4U-M7	128K + 8K	2K	8K			PW	
ATxmega128A4U-M7R[4]	128K + 8K	2K	8K				
ATxmega64A4U-M7	64K + 4K	2K	4K				
ATxmega64A4U-M7R[4]	64K + 4K	2K	4K				
ATxmega32A4U-M7	32K + 4K	1K	4K			44M1	
ATxmega32A4U-M7R[4]	32K + 4K	1K	4K				
ATxmega16A4U-M7	16K + 4K	1K	2K				
ATxmega16A4U-M7R[4]	16K + 4K	1K	2K				

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For packaging information, see "Instruction Set Summary" on page 63.
4. Tape and Reel

Package Type	
44A	44-Lead, 10 x 10mm body size, 1.0mm body thickness, 0.8mm lead pitch, thin profile plastic quad flat package (TQFP)
44M1	44-Pad, 7x7x1mm body, lead pitch 0.50mm, 5.20mm exposed pad, thermally enhanced plastic very thin quad no lead package (VQFN)
PW	44-Pad, 7x7x1mm body, lead pitch 0.50mm, 5.20mm exposed pad, thermally enhanced plastic very thin quad no lead package (VQFN)
49C2	49-Ball (7 x 7 Array), 0.65mm Pitch, 5.0 x 5.0 x 1.0mm, very thin, fine-pitch ball grid array package (VFBGA)

Typical Applications

Industrial control	Climate control	Low power battery applications
Factory automation	RF and ZigBee®	Power tools
Building control	USB connectivity	HVAC
Board control	Sensor control	Utility metering
White goods	Optical	Medical applications

a 1kHz output. The oscillator is automatically enabled/disabled when it is used as clock source for any part of the device. This oscillator can be selected as the clock source for the RTC.

10.3.2 32.768kHz Calibrated Internal Oscillator

This oscillator provides an approximate 32.768kHz clock. It is calibrated during production to provide a default frequency close to its nominal frequency. The calibration register can also be written from software for run-time calibration of the oscillator frequency. The oscillator employs a built-in prescaler, which provides both a 32.768kHz output and a 1.024kHz output.

10.3.3 32.768kHz Crystal Oscillator

A 32.768kHz crystal oscillator can be connected between the TOSC1 and TOSC2 pins and enables a dedicated low frequency oscillator input circuit. A low power mode with reduced voltage swing on TOSC2 is available. This oscillator can be used as a clock source for the system clock and RTC, and as the DFLL reference clock.

10.3.4 0.4 - 16MHz Crystal Oscillator

This oscillator can operate in four different modes optimized for different frequency ranges, all within 0.4 - 16MHz.

10.3.5 2MHz Run-time Calibrated Internal Oscillator

The 2MHz run-time calibrated internal oscillator is the default system clock source after reset. It is calibrated during production to provide a default frequency close to its nominal frequency. A DFLL can be enabled for automatic run-time calibration of the oscillator to compensate for temperature and voltage drift and optimize the oscillator accuracy.

10.3.6 32MHz Run-time Calibrated Internal Oscillator

The 32MHz run-time calibrated internal oscillator is a high-frequency oscillator. It is calibrated during production to provide a default frequency close to its nominal frequency. A digital frequency looked loop (DFLL) can be enabled for automatic run-time calibration of the oscillator to compensate for temperature and voltage drift and optimize the oscillator accuracy. This oscillator can also be adjusted and calibrated to any frequency between 30MHz and 55MHz. The production signature row contains 48MHz calibration values intended used when the oscillator is used a full-speed USB clock source.

10.3.7 External Clock Sources

The XTAL1 and XTAL2 pins can be used to drive an external oscillator, either a quartz crystal or a ceramic resonator. XTAL1 can be used as input for an external clock signal. The TOSC1 and TOSC2 pins is dedicated to driving a 32.768kHz crystal oscillator.

10.3.8 PLL with 1x-31x Multiplication Factor

The built-in phase locked loop (PLL) can be used to generate a high-frequency system clock. The PLL has a user-selectable multiplication factor of from 1 to 31. In combination with the prescalers, this gives a wide range of output frequencies from all clock sources.

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ELPM	Rd, Z+	Extended Load Program Memory and Post-Increment	Rd ← (RAMPZ:Z), Z ← Z + 1	None	3
SPM		Store Program Memory	(RAMPZ:Z) ← R1:R0	None	-
SPM	Z+	Store Program Memory and Post-Increment by 2	(RAMPZ:Z) ← R1:R0, Z ← Z + 2	None	-
IN	Rd, A	In From I/O Location	Rd ← I/O(A)	None	1
OUT	A, Rr	Out To I/O Location	I/O(A) ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	1 (1)
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2 (1)
XCH	Z, Rd	Exchange RAM location	Temp ← Rd, Rd ← (Z), (Z) ← Temp	None	2
LAS	Z, Rd	Load and Set RAM location	Temp ← Rd, Rd ← (Z), (Z) ← Temp v (Z)	None	2
LAC	Z, Rd	Load and Clear RAM location	Temp ← Rd, Rd ← (Z), (Z) ← ($FFh – Rd) • (Z)	None	2
LAT	Z, Rd	Load and Toggle RAM location	Temp ← Rd, Rd ← (Z), (Z) ← Temp ⊕ (Z)	None	2
Bit and bit-test instructions					
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0, C ← Rd(7)	Z,C,N,V,H	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0, C ← Rd(0)	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0) ← C, Rd(n+1) ← Rd(n), C ← Rd(7)	Z,C,N,V,H	1
ROR	Rd	Rotate Right Through Carry	Rd(7) ← C, Rd(n) ← Rd(n+1), C ← Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0) ↔ Rd(7..4)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
SBI	A, b	Set Bit in I/O Register	I/O(A, b) ← 1	None	1
CBI	A, b	Clear Bit in I/O Register	I/O(A, b) ← 0	None	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1

Table 36-32. Two-wire interface characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		$0.7*V_{CC}$		$V_{CC}+0.5$	V
V_{IL}	Input low voltage		0.5		$0.3*V_{CC}$	V
V_{hys}	Hysteresis of Schmitt trigger inputs		$0.05*V_{CC}$ (1)			V
V_{OL}	Output low voltage	3mA, sink current	0		0.4	V
t_r	Rise time for both SDA and SCL		$20+0.1C_b$ (1)(2)		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF$ (2)	$20+0.1C_b$ (1)(2)		250	ns
t_{SP}	Spikes suppressed by input filter		0		50	ns
I_I	Input current for each I/O Pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	µA
C_I	Capacitance for each I/O Pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER} (3)>max($10f_{SCL}$, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq 100kHz$	$\frac{V_{CC}-0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		$f_{SCL} > 100kHz$			$\frac{300ns}{C_b}$	
$t_{HD;STA}$	Hold time (repeated) START condition	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
t_{LOW}	Low period of SCL clock	$f_{SCL} \leq 100kHz$	4.7			µs
		$f_{SCL} > 100kHz$	1.3			
t_{HIGH}	High period of SCL clock	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq 100kHz$	4.7			µs
		$f_{SCL} > 100kHz$	0.6			
$t_{HD;DAT}$	Data hold time	$f_{SCL} \leq 100kHz$	0		3.45	µs
		$f_{SCL} > 100kHz$	0		0.9	
$t_{SU;DAT}$	Data setup time	$f_{SCL} \leq 100kHz$	250			ns
		$f_{SCL} > 100kHz$	100			
$t_{SU;STO}$	Setup time for STOP condition	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
t_{BUF}	Bus free time between a STOP and START condition	$f_{SCL} \leq 100kHz$	4.7			µs
		$f_{SCL} > 100kHz$	1.3			

Notes:
1. Required only for $f_{SCL} > 100kHz$.
2. C_b = Capacitance of one bus line in pF.
3. f_{PER} = Peripheral clock frequency.

36.2.16 Two-Wire Interface Characteristics

Table 36-64 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 36-14.

Figure 36-14. Two-wire interface bus timing.

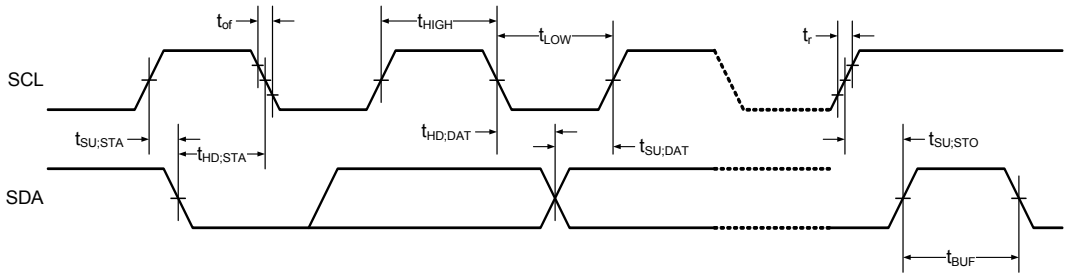


Table 36-64. Two-wire interface characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		$0.7V_{CC}$		$V_{CC}+0.5$	V
V_{IL}	Input low voltage		0.5		$0.3\times V_{CC}$	V
V_{hys}	Hysteresis of Schmitt trigger inputs		$0.05V_{CC}$ (1)			V
V_{OL}	Output low voltage	3mA, sink current	0		0.4	V
t_r	Rise time for both SDA and SCL		$20+0.1C_b$ (1)(2)		300	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF$ (2)	$20+0.1C_b$ (1)(2)		250	ns
t_{SP}	Spikes suppressed by Input filter		0		50	ns
I_I	Input current for each I/O Pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	µA
C_I	Capacitance for each I/O Pin				10	pF
f_{SCL}	SCL clock frequency	f_{PER} (3)>max($10f_{SCL}$, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq 100kHz$	$\frac{V_{CC}-0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		$f_{SCL} > 100kHz$			$\frac{300ns}{C_b}$	
$t_{HD;STA}$	Hold time (repeated) START condition	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
t_{LOW}	Low period of SCL Clock	$f_{SCL} \leq 100kHz$	4.7			µs
		$f_{SCL} > 100kHz$	1.3			
t_{HIGH}	High period of SCL Clock	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq 100kHz$	4.7			µs
		$f_{SCL} > 100kHz$	0.6			

Table 36-69. Current consumption for modules and peripherals.

Symbol	Parameter	Condition [1]		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				1.0		µA
	32.768kHz int. oscillator				29		µA
	2MHz int. oscillator				85		µA
		DFLL enabled with 32.768kHz int. osc. as reference			120		
	32MHz int. oscillator				300		µA
		DFLL enabled with 32.768kHz int. osc. as reference			465		
	PLL	20x multiplication factor, 32MHz int. osc. DIV4 as reference			320		µA
	Watchdog timer				1.0		µA
	BOD	Continuous mode			138		µA
		Sampled mode, includes ULP oscillator			1.0		
	Internal 1.0V reference				103		µA
	Temperature sensor				100		µA
	ADC	250ksps V_{REF} = Ext ref			3.0		mA
			CURRLIMIT = LOW		2.6		
			CURRLIMIT = MEDIUM		2.1		
			CURRLIMIT = HIGH		1.6		
	DAC	250ksps V_{REF} = Ext ref No load	Normal mode		1.9		mA
			Low power mode		1.1		
	AC	High speed mode			330		µA
		Low pPower mode			130		
	DMA	615KBps between I/O registers and SRAM			108		µA
	Timer/counter				16		µA
	USART	Rx and Tx enabled, 9600 BAUD			2.5		µA
	Flash memory and EEPROM programming				8.0		mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

36.3.14.4 32kHz Internal ULP Oscillator characteristics

Table 36-89. 32kHz internal ULP oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Factory calibrated frequency			32		kHz
	Factory calibrated accuracy	T = 85°C, V_{CC} = 3.0V	-12		12	%
	Accuracy		-30		30	%

36.3.14.5 Internal Phase Locked Loop (PLL) characteristics

Table 36-90. Internal PLL characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency (1)	V_{CC}= 1.6 - 1.8V	20		48	MHz
		V_{CC}= 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		µs

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

36.3.14.6 External clock characteristics

Figure 36-17. External clock drive waveform

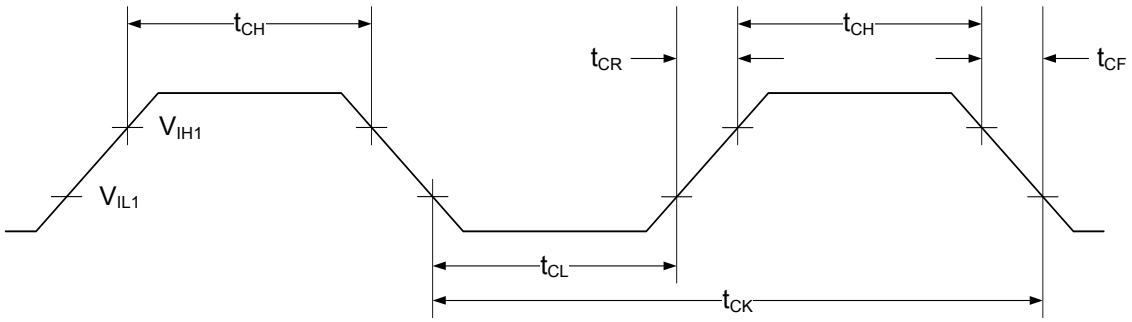


Table 36-91. External clock used as system clock without prescaling.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (1)	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			

36.4.14 Clock and Oscillator Characteristics

36.4.14.1 Calibrated 32.768kHz Internal Oscillator characteristics

Table 36-118. 32.768kHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency			32.768		kHz
	Factory calibration accuracy	T = 85°C, V_{CC} = 3.0V	-0.5		0.5	%
	User calibration accuracy		-0.5		0.5	%

36.4.14.2 Calibrated 2MHz RC Internal Oscillator characteristics

Table 36-119. 2MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	1.8		2.2	MHz
	Factory calibrated frequency			2.0		MHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	%
	DFLL calibration stepsize			0.21		%

36.4.14.3 Calibrated and tunable 32MHz internal oscillator characteristics

Table 36-120. 32MHz internal oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Frequency range	DFLL can tune to this frequency over voltage and temperature	30		55	MHz
	Factory calibrated frequency			32		MHz
	Factory calibration accuracy	T = 85°C, V_{CC}= 3.0V	-1.5		1.5	%
	User calibration accuracy		-0.2		0.2	%
	DFLL calibration step size			0.22		%

36.4.14.4 32kHz Internal ULP Oscillator characteristics

Table 36-121. 32kHz internal ULP oscillator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Output frequency			32		kHz
	Accuracy		-30		30	%

36.4.14.5 Internal Phase Locked Loop (PLL) characteristics

Table 36-122. Internal PLL characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency (1)	V_{CC}= 1.6 - 1.8V	20		48	MHz
		V_{CC}= 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		µs

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

36.4.14.6 External clock characteristics

Figure 36-24. External clock drive waveform

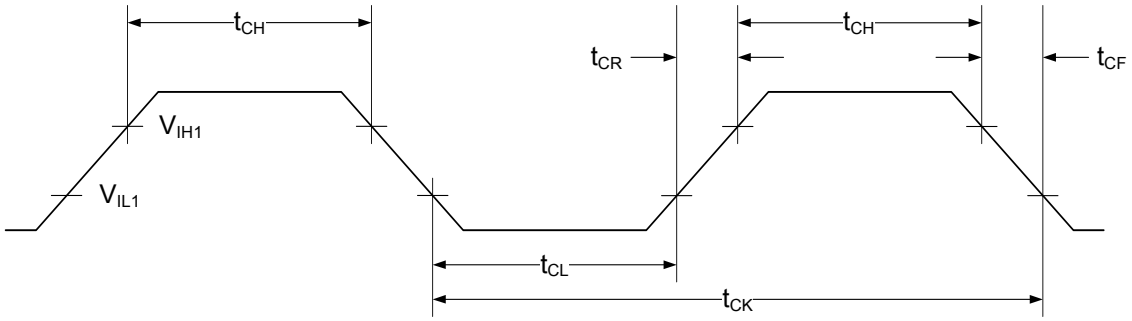


Table 36-123.External clock used as system clock without prescaling.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (1)	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

Table 36-124. External clock with prescaler [1] for system clock.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency [2]	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes:
1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

36.4.14.7 External 16MHz crystal oscillator and XOSC characteristic

Table 36-125. External 16MHz crystal oscillator and XOSC characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0		<10		ns
			FRQRANGE=1, 2, or 3		<1		
		XOSCPWR=1			<1		
	Long term jitter	XOSCPWR=0	FRQRANGE=0		<6		ns
			FRQRANGE=1, 2, or 3		<0.5		
		XOSCPWR=1			<0.5		
	Frequency error	XOSCPWR=0	FRQRANGE=0		<0.1		%
			FRQRANGE=1		<0.05		
			FRQRANGE=2 or 3		<0.005		
		XOSCPWR=1			<0.005		

Figure 37-118. I/O pin input threshold voltage vs. V_{CC}.

V_{IL} I/O pin read as "0".

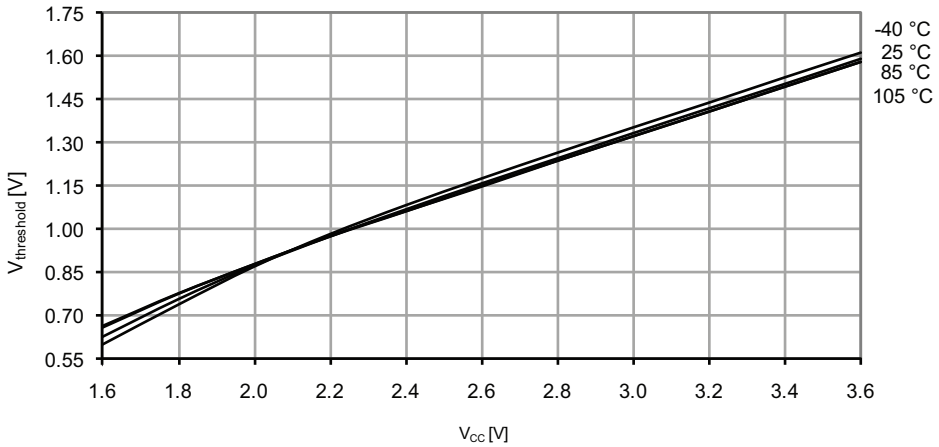


Figure 37-119. I/O pin input hysteresis vs. V_{CC}.

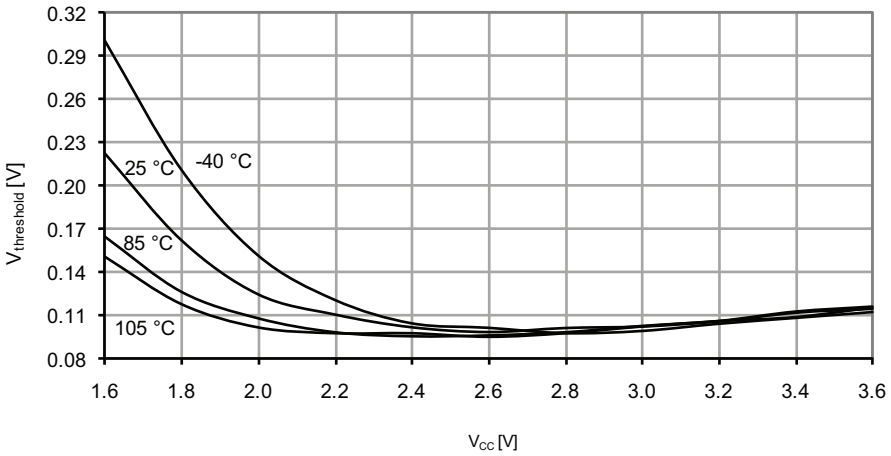


Figure 37-128. Offset error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps.

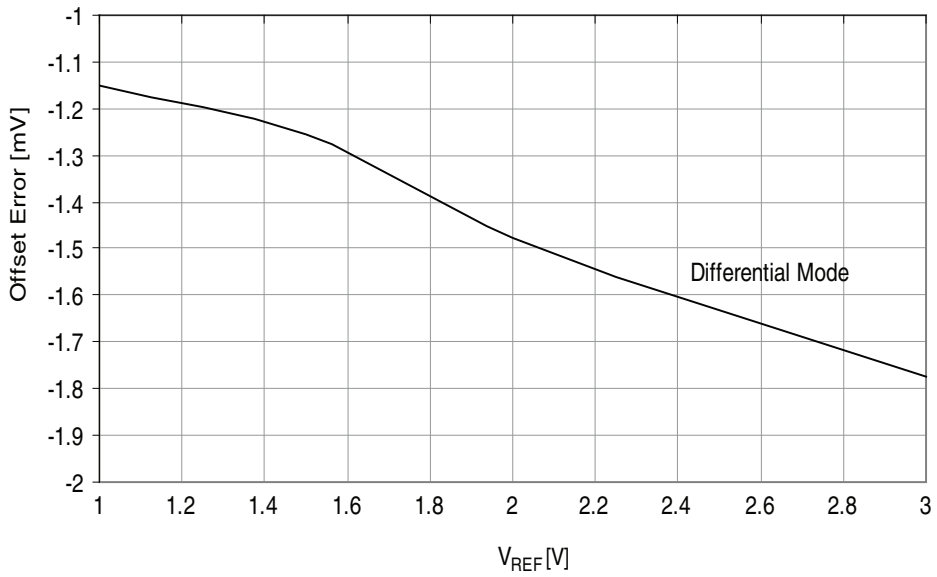


Figure 37-129. Gain error vs. temperature.

V_{CC} = 3.0V, V_{REF} = external 2.0V.

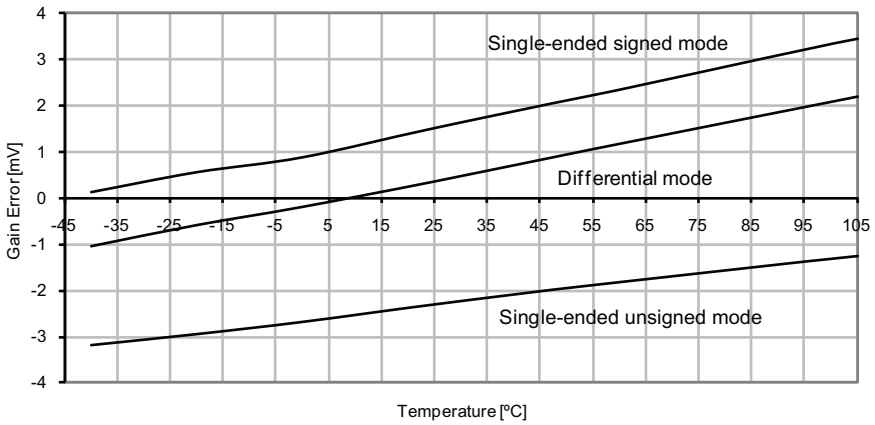
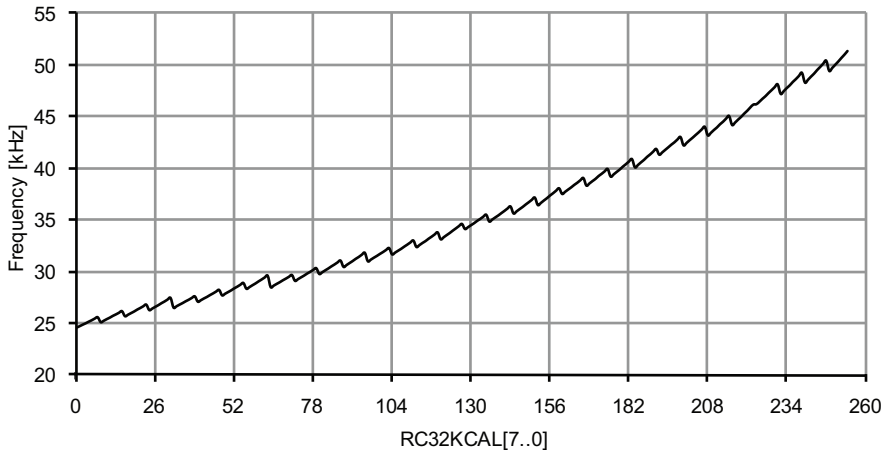


Figure 37-156. 32.768kHz internal oscillator frequency vs. calibration value.

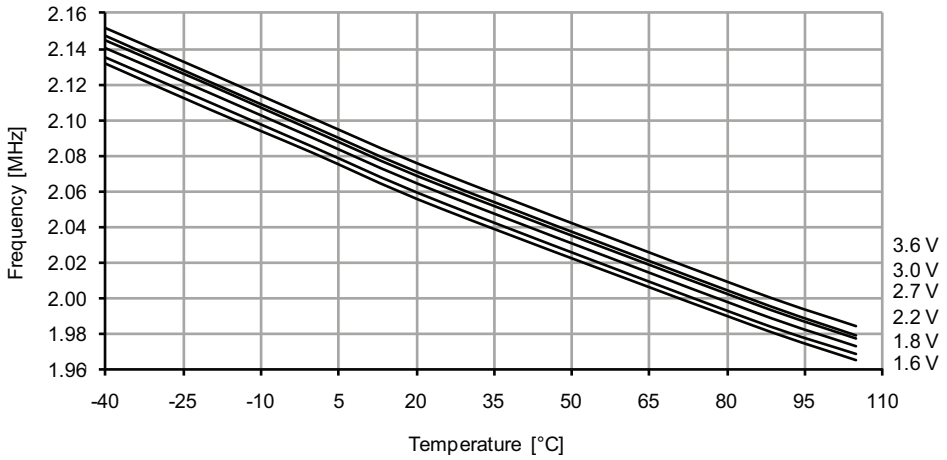
V_{CC} = 3.0V, T = 25°C.



37.2.10.3 2MHz Internal Oscillator

Figure 37-157. 2MHz internal oscillator frequency vs. temperature.

DFLL disabled.



37.3 ATxmega64A4U

37.3.1 Current consumption

37.3.1.1 Active mode supply current

Figure 37-169. Active supply current vs. frequency.
f_{SYS} = 0 - 1MHz external clock, T = 25°C.

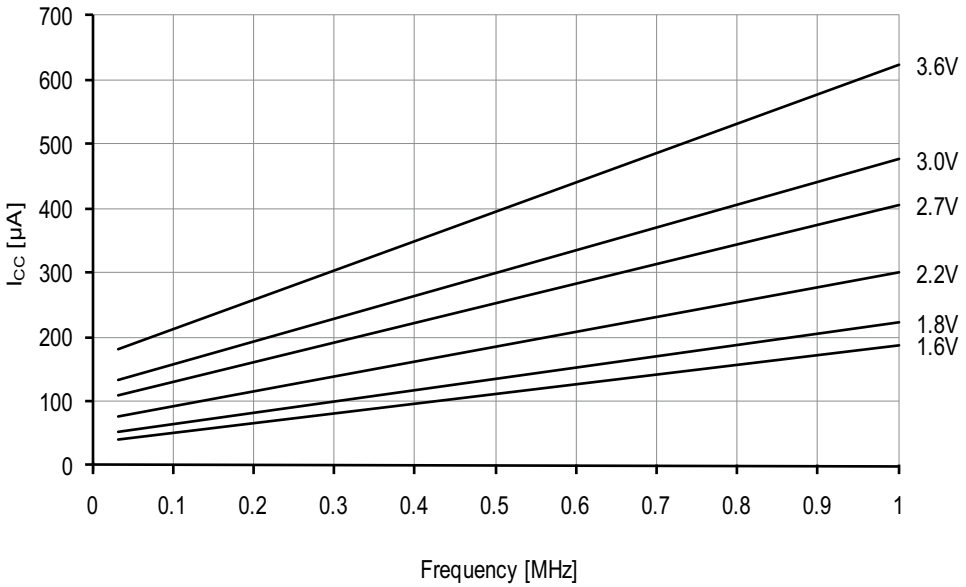


Figure 37-170. Active supply current vs. frequency.
f_{SYS} = 1 - 32MHz external clock, T = 25°C.

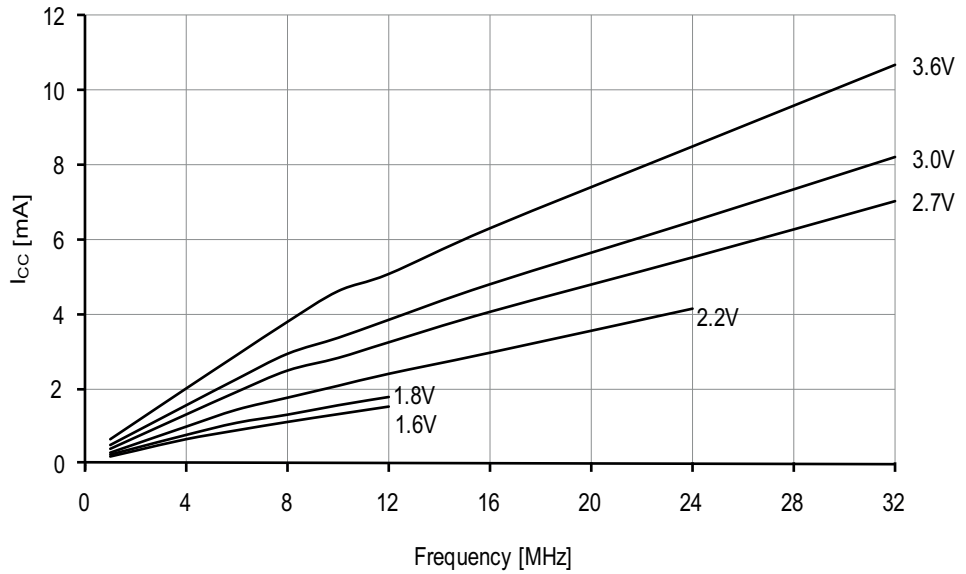


Figure 37-197. I/O pin output voltage vs. sink current.

V_{CC} = 3.0V.

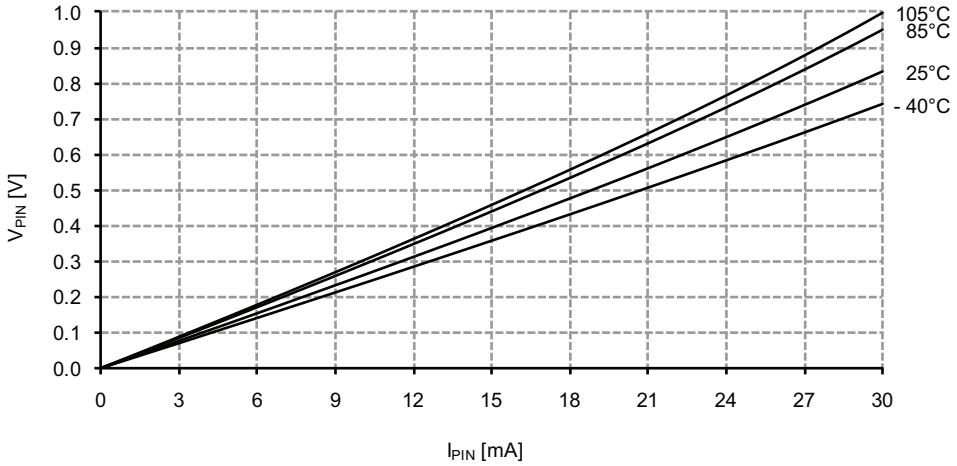


Figure 37-198. I/O pin output voltage vs. sink current.

V_{CC} = 3.3V.

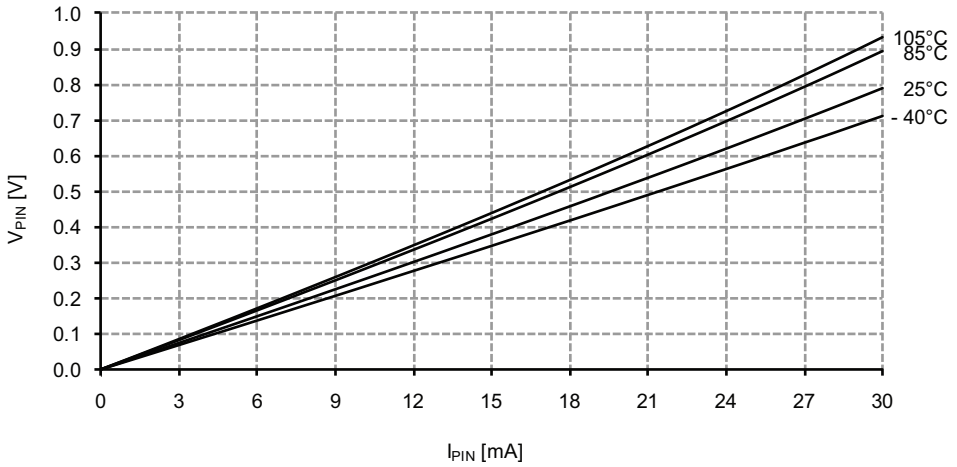


Figure 37-211. Gain error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.

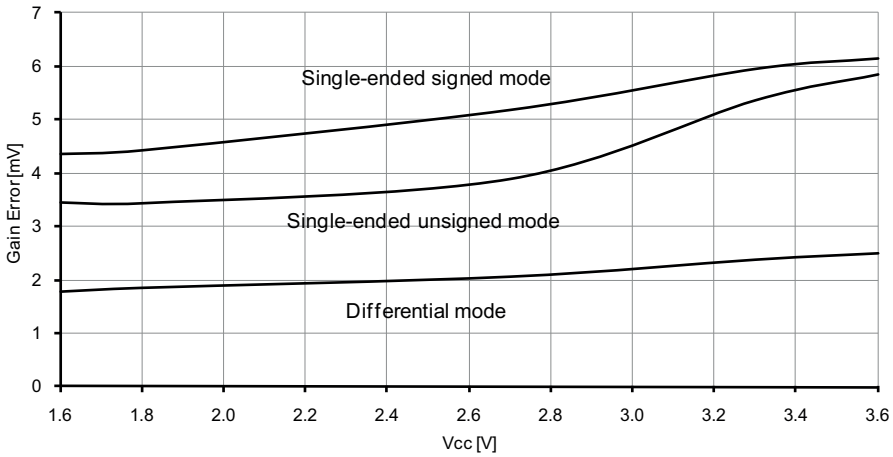


Figure 37-212. Offset error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps.

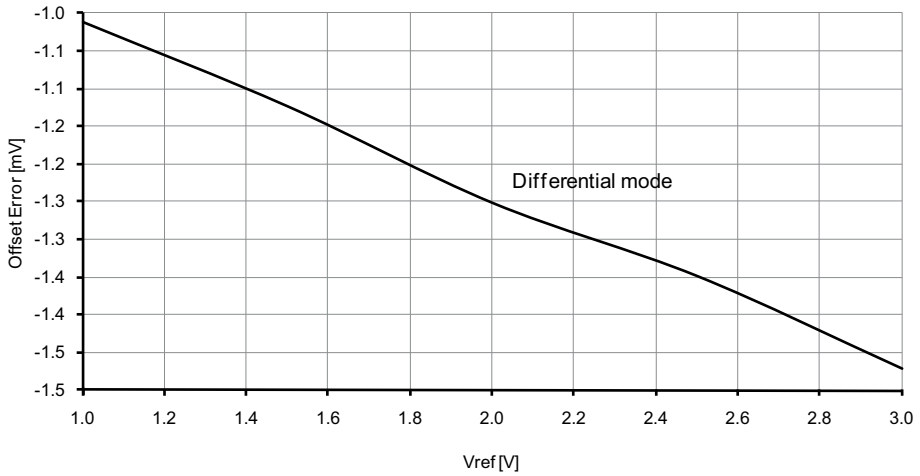
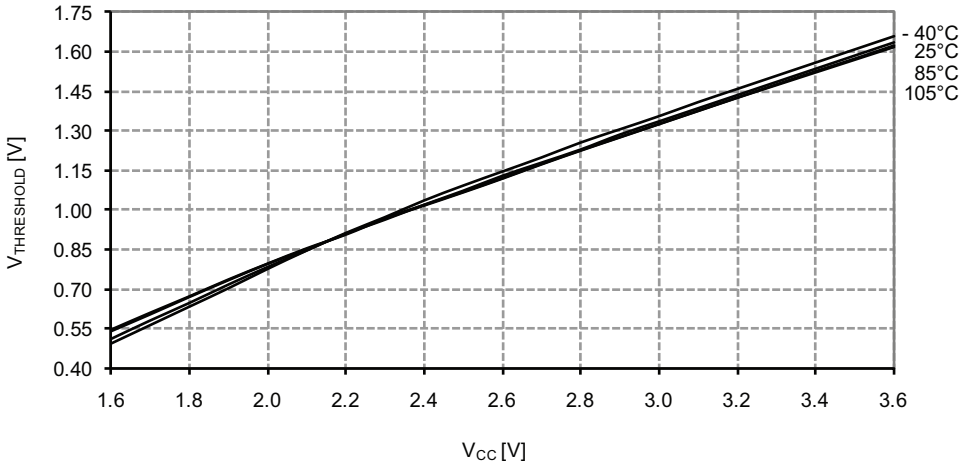


Figure 37-235. Reset pin input threshold voltage vs. V_{CC}.

V_{IL} - Reset pin read as "0".



37.3.9 Power-on Reset Characteristics

Figure 37-236. Power-on reset current consumption vs. V_{CC}.

BOD level = 3.0V, enabled in continuous mode.

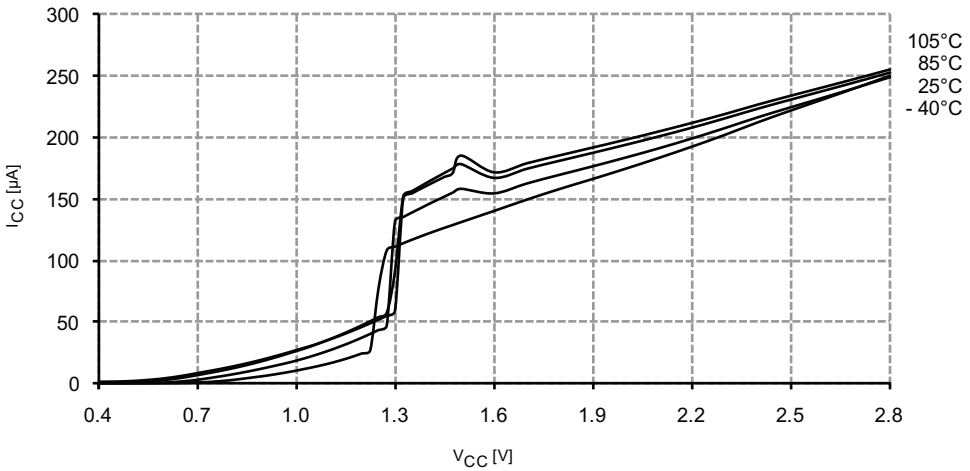
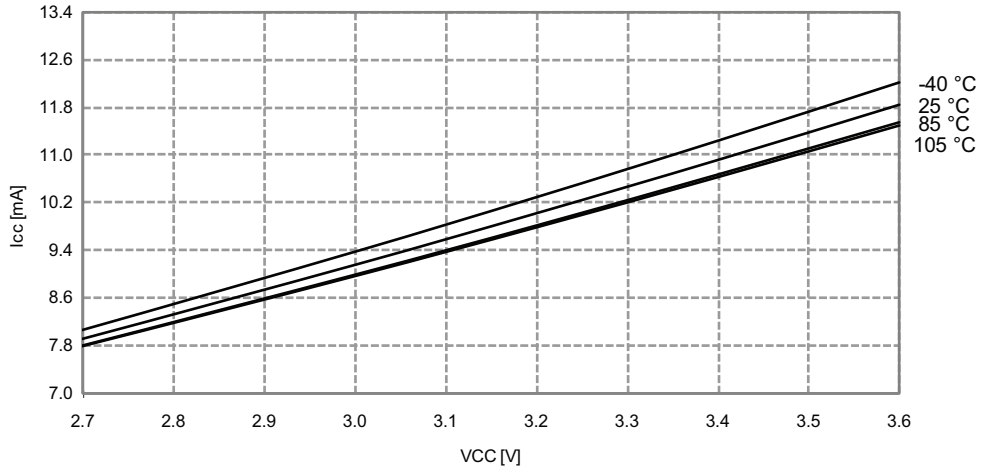


Figure 37-259. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator.



37.4.1.2 Idle mode supply current

Figure 37-260. Idle mode supply current vs. frequency.

f_{SYS} = 0 - 1MHz external clock, T = 25°C

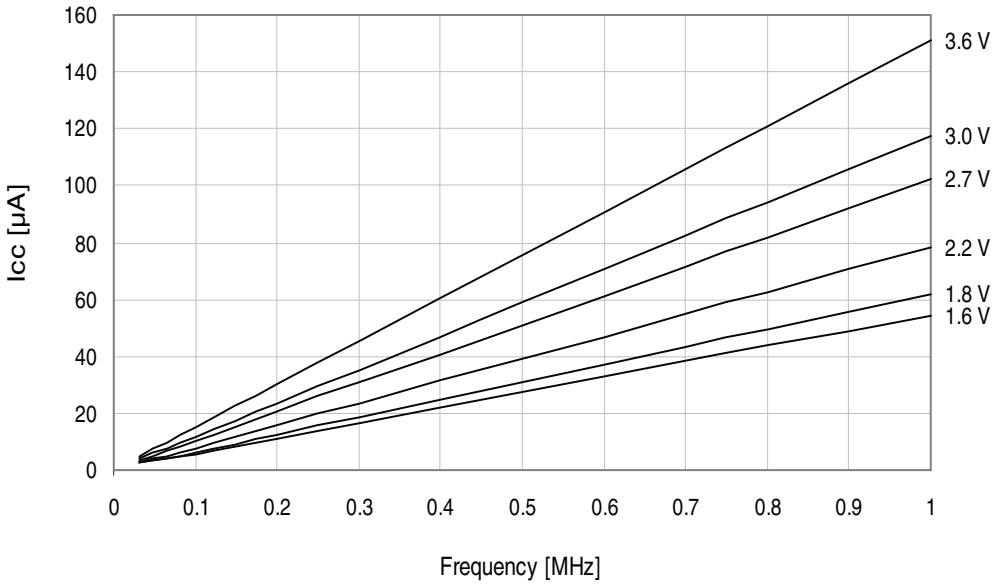
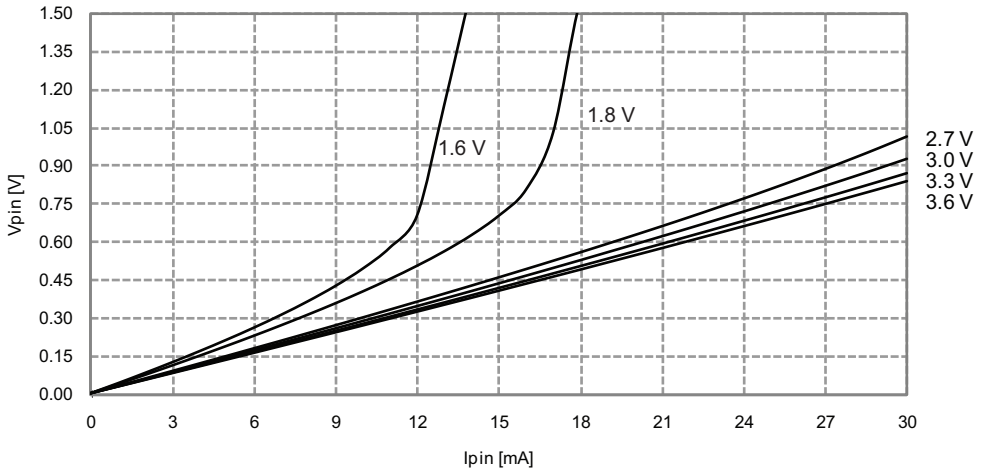


Figure 37-283. I/O pin output voltage vs. sink current



37.4.2.3 Thresholds and Hysteresis

Figure 37-284. I/O pin input threshold voltage vs. V_{CC}.

T = 25°C

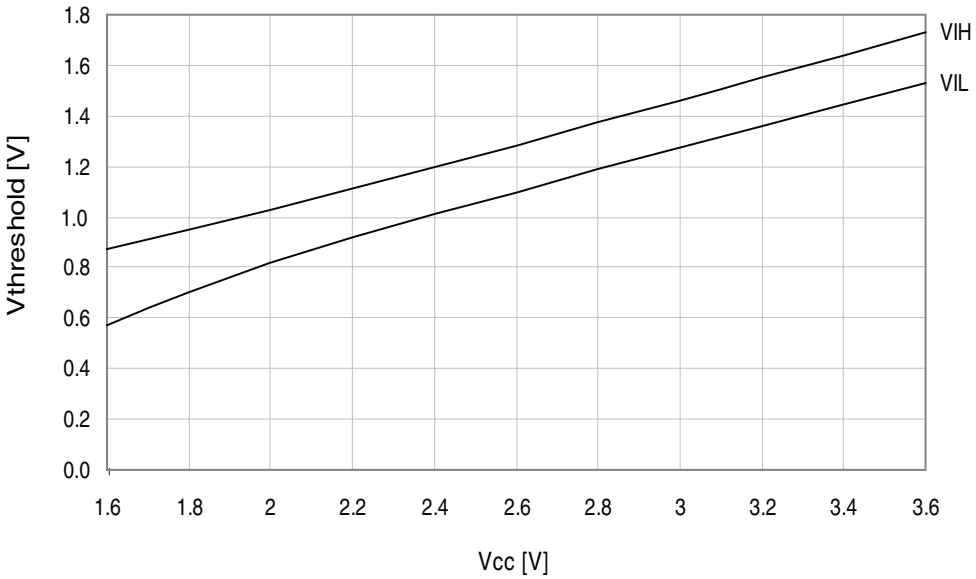


Figure 37-307. Analog comparator hysteresis vs. V_{CC}.

Low power, large hysteresis

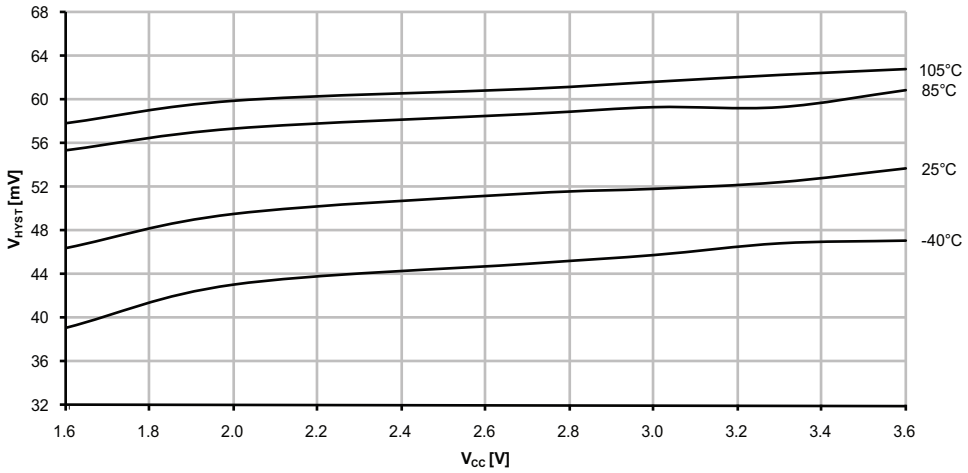


Figure 37-308. Analog comparator current source vs. calibration value.

Temperature = 25°C