Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64a4u-auk

14. Interrupts and Programmable Multilevel Interrupt Controller

14.1 Features

- Short and predictable interrupt response time
- Separate interrupt configuration and vector address for each interrupt
- Programmable multilevel interrupt controller
  - Interrupt prioritizing according to level and vector address
  - Three selectable interrupt levels for all interrupts: low, medium and high
  - Selectable, round-robin priority scheme within low-level interrupts
  - Non-maskable interrupts for critical functions
- Interrupt vectors optionally placed in the application section or the boot loader section

14.2 Overview

Interrupts signal a change of state in peripherals, and this can be used to alter program execution. Peripherals can have one or more interrupts, and all are individually enabled and configured. When an interrupt is enabled and configured, it will generate an interrupt request when the interrupt condition is present. The programmable multilevel interrupt controller (PMIC) controls the handling and prioritizing of interrupt requests. When an interrupt request is acknowledged by the PMIC, the program counter is set to point to the interrupt vector, and the interrupt handler can be executed.

All peripherals can select between three different priority levels for their interrupts: low, medium, and high. Interrupts are prioritized according to their level and their interrupt vector address. Medium-level interrupts will interrupt low-level interrupt handlers. High-level interrupts will interrupt both medium- and low-level interrupt handlers. Within each level, the interrupt priority is decided from the interrupt vector address, where the lowest interrupt vector address has the highest interrupt priority. Low-level interrupts have an optional round-robin scheduling scheme to ensure that all interrupts are serviced within a certain amount of time.

Non-maskable interrupts (NMI) are also supported, and can be used for system critical functions.

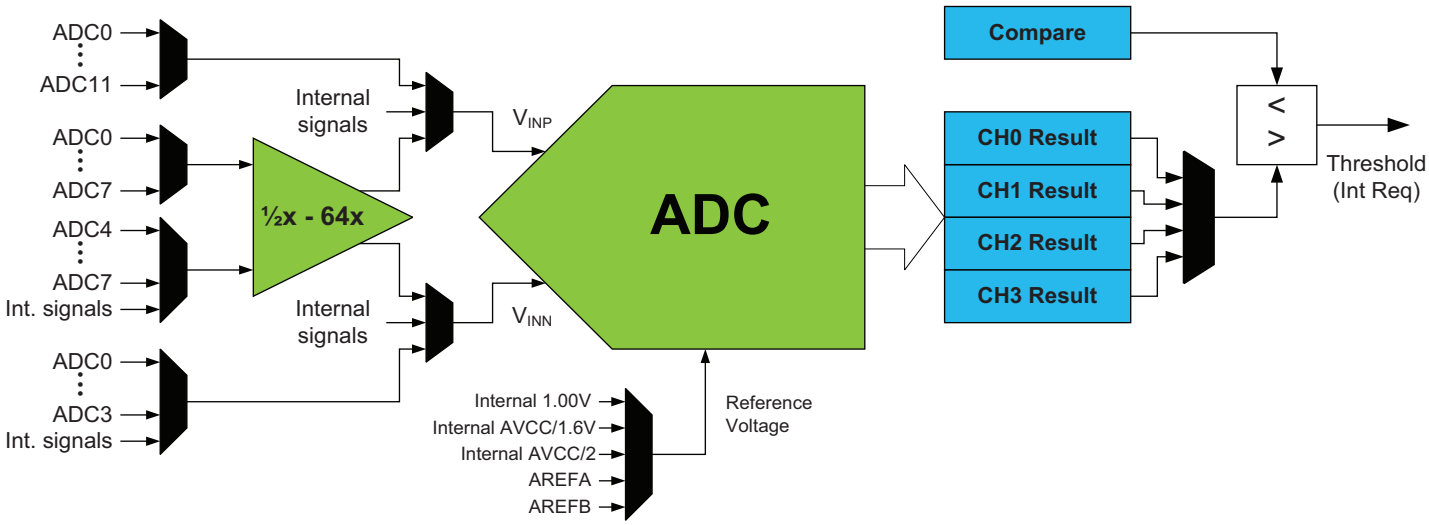
14.3 Interrupt vectors

The interrupt vector is the sum of the peripheral's base interrupt address and the offset address for specific interrupts in each peripheral. The base addresses for the Atmel AVR XMEGA A4U devices are shown in Table 14-1 on page 30. Offset addresses for each interrupt available in the peripheral are described for each peripheral in the XMEGA AU manual. For peripherals or modules that have only one interrupt, the interrupt vector is shown in Table 14-1 on page 30. The program address is the word address.

Table 14-1. Reset and interrupt vectors

Program address (base address)	Source	Interrupt description
0x000	RESET	
0x002	OSCF_INT_vect	Crystal oscillator failure interrupt vector (NMI)
0x004	PORTC_INT_base	Port C interrupt base
0x008	PORTR_INT_base	Port R interrupt base
0x00C	DMA_INT_base	DMA controller interrupt base
0x014	RTC_INT_base	Real time counter interrupt base
0x018	TWIC_INT_base	Two-Wire Interface on Port C interrupt base
0x01C	TCC0_INT_base	Timer/counter 0 on port C interrupt base
0x028	TCC1_INT_base	Timer/counter 1 on port C interrupt base
0x030	SPIC_INT_vect	SPI on port C interrupt vector
0x032	USARTC0_INT_base	USART 0 on port C interrupt base
0x038	USARTC1_INT_base	USART 1 on port C interrupt base
0x03E	AES_INT_vect	AES interrupt vector
0x040	NVM_INT_base	Nonvolatile Memory interrupt base
0x044	PORTB_INT_base	Port B interrupt base
0x056	PORTE_INT_base	Port E interrupt base
0x05A	TWIE_INT_base	Two-wire Interface on Port E interrupt base
0x05E	TCE0_INT_base	Timer/counter 0 on port E interrupt base
0x06A	TCE1_INT_base	Timer/counter 1 on port E interrupt base
0x074	USARTE0_INT_base	USART 0 on port E interrupt base
0x080	PORTD_INT_base	Port D interrupt base
0x084	PORTA_INT_base	Port A interrupt base
0x088	ACA_INT_base	Analog Comparator on Port A interrupt base
0x08E	ADCA_INT_base	Analog to Digital Converter on Port A interrupt base
0x09A	TCD0_INT_base	Timer/counter 0 on port D interrupt base
0x0A6	TCD1_INT_base	Timer/counter 1 on port D interrupt base
0x0AE	SPID_INT_vector	SPI on port D interrupt vector
0x0B0	USARTD0_INT_base	USART 0 on port D interrupt base
0x0B6	USARTD1_INT_base	USART 1 on port D interrupt base
0x0FA	USB_INT_base	USB on port D interrupt base

Figure 28-1. ADC overview.



Two inputs can be sampled simultaneously as both the ADC and the gain stage include sample and hold circuits, and the gain stage has 1x gain setting. Four inputs can be sampled within 1.5µs without any intervention by the application.

The ADC may be configured for 8- or 12-bit result, reducing the minimum conversion time (propagation delay) from 3.5µs for 12-bit to 2.5µs for 8-bit result.

ADC conversion results are provided left- or right adjusted with optional ‘1’ or ‘0’ padding. This eases calculation when the result is represented as a signed integer (signed 16-bit number).

PORTA has one ADC. Notation of this peripheral is ADCA.

Mnemonics	Operands	Description	Operation	Flags	#Clocks
MOVW	Rd, Rr	Copy Register Pair	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LDS	Rd, k	Load Direct from data space	Rd ← (k)	None	2 (1)(2)
LD	Rd, X	Load Indirect	Rd ← (X)	None	1 (1)(2)
LD	Rd, X+	Load Indirect and Post-Increment	Rd ← (X) X ← X + 1	None	1 (1)(2)
LD	Rd, -X	Load Indirect and Pre-Decrement	X ← X - 1, ← X - 1 Rd ← (X) ← (X)	None	2 (1)(2)
LD	Rd, Y	Load Indirect	Rd ← (Y) ← (Y)	None	1 (1)(2)
LD	Rd, Y+	Load Indirect and Post-Increment	Rd ← (Y) Y ← Y + 1	None	1 (1)(2)
LD	Rd, -Y	Load Indirect and Pre-Decrement	Y ← Y - 1 Rd ← (Y)	None	2 (1)(2)
LDD	Rd, Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2 (1)(2)
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	1 (1)(2)
LD	Rd, Z+	Load Indirect and Post-Increment	Rd ← (Z), Z ← Z+1	None	1 (1)(2)
LD	Rd, -Z	Load Indirect and Pre-Decrement	Z ← Z - 1, Rd ← (Z)	None	2 (1)(2)
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2 (1)(2)
STS	k, Rr	Store Direct to Data Space	(k) ← Rd	None	2 (1)
ST	X, Rr	Store Indirect	(X) ← Rr	None	1 (1)
ST	X+, Rr	Store Indirect and Post-Increment	(X) ← Rr, X ← X + 1	None	1 (1)
ST	-X, Rr	Store Indirect and Pre-Decrement	X ← X - 1, (X) ← Rr	None	2 (1)
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	1 (1)
ST	Y+, Rr	Store Indirect and Post-Increment	(Y) ← Rr, Y ← Y + 1	None	1 (1)
ST	-Y, Rr	Store Indirect and Pre-Decrement	Y ← Y - 1, (Y) ← Rr	None	2 (1)
STD	Y+q, Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2 (1)
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	1 (1)
ST	Z+, Rr	Store Indirect and Post-Increment	(Z) ← Rr Z ← Z + 1	None	1 (1)
ST	-Z, Rr	Store Indirect and Pre-Decrement	Z ← Z - 1	None	2 (1)
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2 (1)
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Increment	Rd ← (Z), Z ← Z + 1	None	3
ELPM		Extended Load Program Memory	R0 ← (RAMPZ:Z)	None	3
ELPM	Rd, Z	Extended Load Program Memory	Rd ← (RAMPZ:Z)	None	3

36.2.3 Current consumption

Table 36-36. Current consumption for Active mode and sleep modes.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption[1]	32kHz, Ext. Clk	V_{CC} = 1.8V		40		µA
			V_{CC} = 3.0V		80		
		1MHz, Ext. Clk	V_{CC} = 1.8V		230		
			V_{CC} = 3.0V		480		
		2MHz, Ext. Clk	V_{CC} = 1.8V		430	600	
			V_{CC} = 3.0V		0.9	1.4	mA
		32MHz, Ext. Clk			9.6	12	
	Idle power consumption[1]	32kHz, Ext. Clk	V_{CC} = 1.8V		2.4		µA
			V_{CC} = 3.0V		3.9		
		1MHz, Ext. Clk	V_{CC} = 1.8V		62		
			V_{CC} = 3.0V		118		
		2MHz, Ext. Clk	V_{CC} = 1.8V		125	225	
			V_{CC} = 3.0V		240	350	
		32MHz, Ext. Clk			3.8	5.5	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			1.2	4.5	
		T = 105°C			3.5	6.0	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.3	3.0	
		WDT and sampled BOD enabled, T = 85°C			2.4	6.0	
		WDT and sampled BOD enabled, T = 105°C			4.5	8.0	
	Power-save power consumption[2]	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.2		µA
			V_{CC} = 3.0V		1.3		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.6	2.0	
			V_{CC} = 3.0V		0.7	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.8	3.0	
			V_{CC} = 3.0V		1.0	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		320		

Notes:
1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

Table 36-60. External clock with prescaler [1] for system clock.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency [2]	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

36.2.14.7 External 16MHz crystal oscillator and XOSC characteristic

Table 36-61. External 16MHz crystal oscillator and XOSC characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0		<10		ns
			FRQRANGE=1, 2, or 3		<1		
		XOSCPWR=1			<1		
	Long term jitter	XOSCPWR=0	FRQRANGE=0		<6		ns
			FRQRANGE=1, 2, or 3		<0.5		
		XOSCPWR=1			<0.5		
	Frequency error	XOSCPWR=0	FRQRANGE=0		<0.1		%
			FRQRANGE=1		<0.05		
			FRQRANGE=2 or 3		<0.005		
		XOSCPWR=1			<0.005		
	Duty cycle	XOSCPWR=0	FRQRANGE=0		40		%
			FRQRANGE=1		42		
			FRQRANGE=2 or 3		45		
		XOSCPWR=1			48		

36.3.10 Brownout Detection Characteristics

Table 36-81. Brownout detection characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{BOT}	BOD level 0 falling V_{CC}		1.50	1.62	1.72	V
	BOD level 1 falling V_{CC}			1.8		
	BOD level 2 falling V_{CC}			2.0		
	BOD level 3 falling V_{CC}			2.2		
	BOD level 4 falling V_{CC}			2.4		
	BOD level 5 falling V_{CC}			2.6		
	BOD level 6 falling V_{CC}			2.8		
	BOD level 7 falling V_{CC}			3.0		
t_{BOD}	Detection time	Continuous mode		0.4		µs
		Sampled mode		1000		
V_{HYST}	Hysteresis			1.2		%

36.3.11 External Reset Characteristics

Table 36-82. External reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width		1000	95		ns
V_{RST}	Reset threshold voltage (V_{IH})	V_{CC} = 2.7 - 3.6V		0.60×V_{CC}		V
		V_{CC} = 1.6 - 2.7V		0.60×V_{CC}		
	Reset threshold voltage (V_{IL})	V_{CC} = 2.7 - 3.6V		0.50×V_{CC}		
		V_{CC} = 1.6 - 2.7V		0.40×V_{CC}		
R_{RST}	Reset pin Pull-up Resistor			25		kΩ

36.3.12 Power-on Reset Characteristics

Table 36-83. Power-on reset characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{POT-} (1)	POR threshold voltage falling V_{CC}	V_{CC} falls faster than 1V/ms	0.4	1.0		V
		V_{CC} falls at 1V/ms or slower	0.8	1.0		
V_{POT+}	POR threshold voltage rising V_{CC}			1.3	1.59	

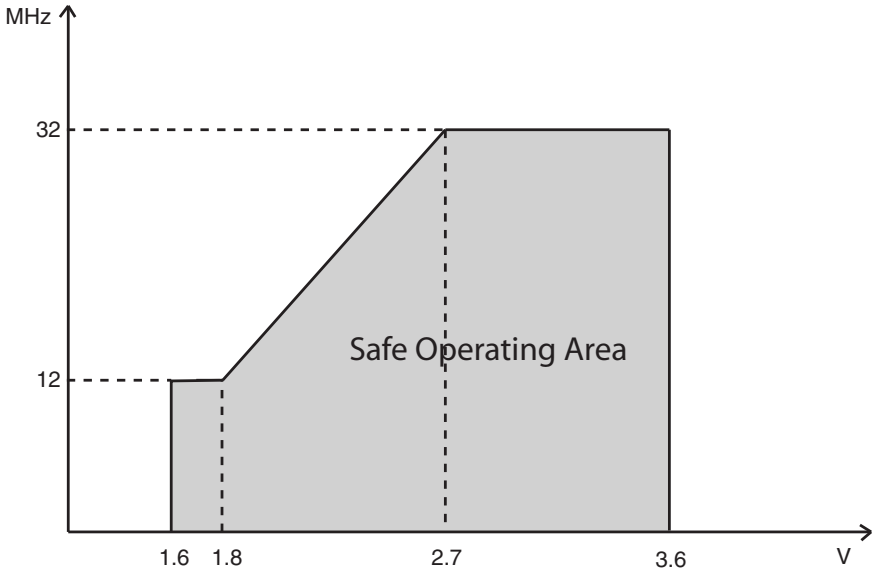
Note: 1. V_{POT-} values are only valid when BOD is disabled. When BOD is enabled V_{POT-} = V_{POT+}.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Long term jitter	XOSCPWR=0	FRQRANGE=0		<6		ns
			FRQRANGE=1, 2, or 3		<0.5		
		XOSCPWR=1			<0.5		
	Frequency error	XOSCPWR=0	FRQRANGE=0		<0.1		%
			FRQRANGE=1		<0.05		
			FRQRANGE=2 or 3		<0.005		
		XOSCPWR=1			<0.005		
	Duty cycle	XOSCPWR=0	FRQRANGE=0		40		%
			FRQRANGE=1		42		
			FRQRANGE=2 or 3		45		
		XOSCPWR=1			48		
R_Q	Negative impedance [1]	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF	2.4k			Ω
			1MHz crystal, CL=20pF	8.7k			
			2MHz crystal, CL=20pF	2.1k			
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal	4.2k			
			8MHz crystal	250			
			9MHz crystal	195			
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal	360			
			9MHz crystal	285			
			12MHz crystal	155			
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal	365			
			12MHz crystal	200			
			16MHz crystal	105			
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal	435			
			12MHz crystal	235			
			16MHz crystal	125			
		XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal	495			
			12MHz crystal	270			
			16MHz crystal	145			
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal	305			
			16MHz crystal	160			
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal	380			
			16MHz crystal	205			

Table 36-95. SPI timing characteristics and requirements.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{SCK}	SCK period	Master		(See Table 21-4 in XMEGA AU Manual)		ns
t_{SCKW}	SCK high/low width	Master		0.5*SCK		
t_{SCKR}	SCK rise time	Master		2.7		
t_{SCKF}	SCK fall time	Master		2.7		
t_{MIS}	MISO setup to SCK	Master		11		
t_{MIH}	MISO hold after SCK	Master		0		
t_{MOS}	MOSI setup SCK	Master		0.5*SCK		
t_{MOH}	MOSI hold after SCK	Master		1.0		
t_{SSCK}	Slave SCK Period	Slave	4*t Clk_{PER}			
t_{SSCKW}	SCK high/low width	Slave	2*t Clk_{PER}			
t_{SSCKR}	SCK rise time	Slave			1600	
t_{SSCKF}	SCK fall time	Slave			1600	
t_{SIS}	MOSI setup to SCK	Slave	3.0			
t_{SIH}	MOSI hold after SCK	Slave	t_{PER}			
t_{SSS}	$\overline{SS}$ setup to SCK	Slave	20			
t_{SSH}	$\overline{SS}$ hold after SCK	Slave	20			
t_{SOS}	MISO setup SCK	Slave		8.0		
t_{SOH}	MISO hold after SCK	Slave		13.0		
t_{SOSS}	MISO setup after $\overline{SS}$ low	Slave		11.0		
t_{SOSH}	MISO hold after $\overline{SS}$ high	Slave		8.0		

Figure 36-22.Maximum Frequency vs. V_{CC}.



36.4.8 Analog Comparator Characteristics

Table 36-111. Analog Comparator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage			<±10		mV
I_{lk}	Input leakage current			<1		nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			100		µs
V_{hys1}	Hysteresis, none			0		mV
V_{hys2}	Hysteresis, small	mode = High Speed (HS)		13		mV
		mode = Low Power (LP)		30		
V_{hys3}	Hysteresis, large	mode = HS		30		mV
		mode = LP		60		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T= 85°C mode = HS		30	90	ns
		mode = HS		30		
		V_{CC} = 3.0V, T= 85°C mode = LP		130	500	
		mode = LP		130		
	64-level voltage scaler	Integral non-linearity (INL)		0.3	0.5	lsb

36.4.9 Bandgap and Internal 1.0V Reference Characteristics

Table 36-112. Bandgap and Internal 1.0V reference characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC or DAC	1 Clk_{PER} + 2.5µs			µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T= 85°C, after calibration	0.99	1.0	1.01	V
	Variation over voltage and temperature	Relative to T= 85°C, V_{CC} = 3.0V		±1.5		%

Figure 37-34. I/O pin input threshold voltage vs. V_{CC}.

V_{IL} I/O pin read as "0".

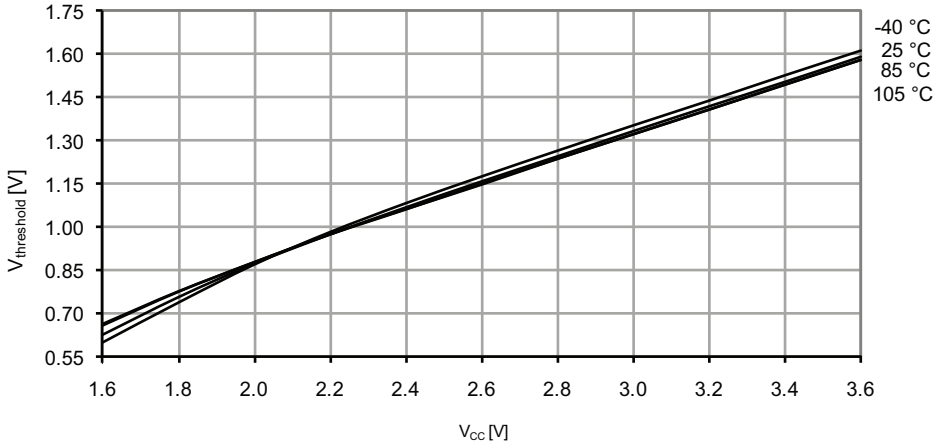


Figure 37-35. I/O pin input hysteresis vs. V_{CC}.

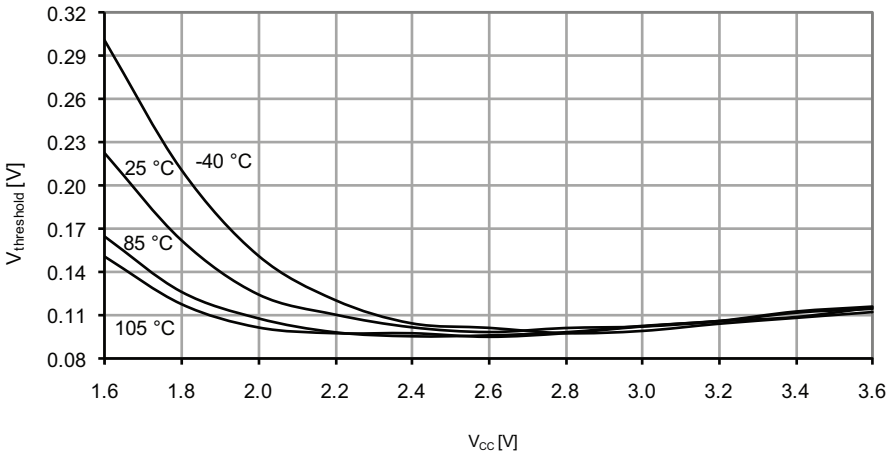
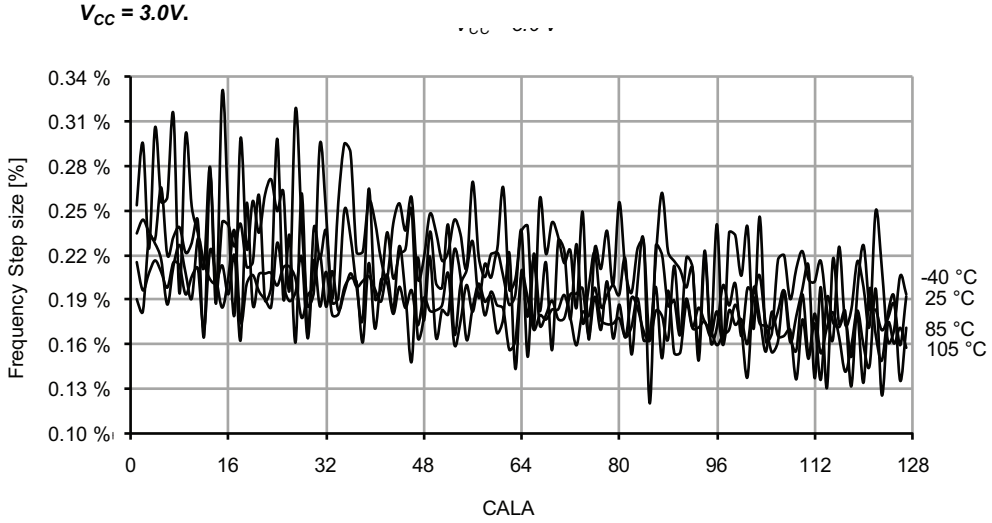


Figure 37-82. 48MHz internal oscillator CALA calibration step size.

V_{CC} = 3.0V.



37.1.11 Two-Wire Interface characteristics

Figure 37-83. SDA hold time vs. supply voltage.

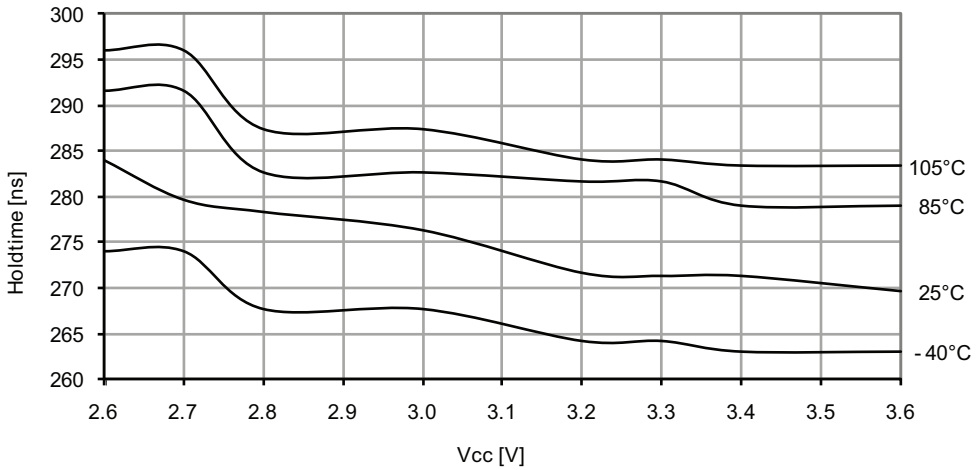


Figure 37-89.Active mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.

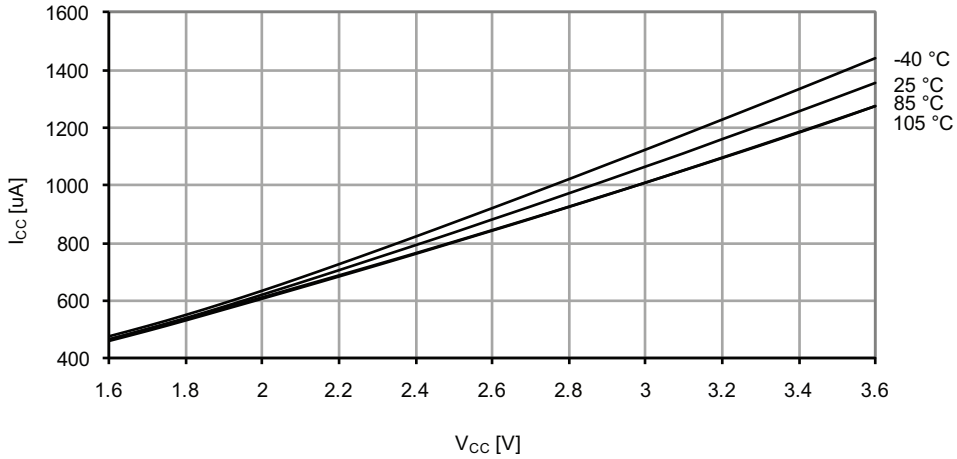


Figure 37-90.Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

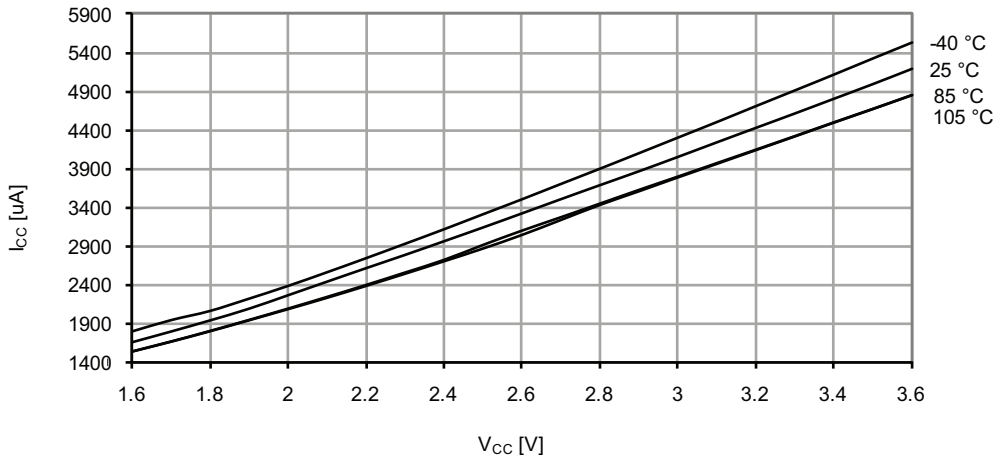


Figure 37-97. Idle mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

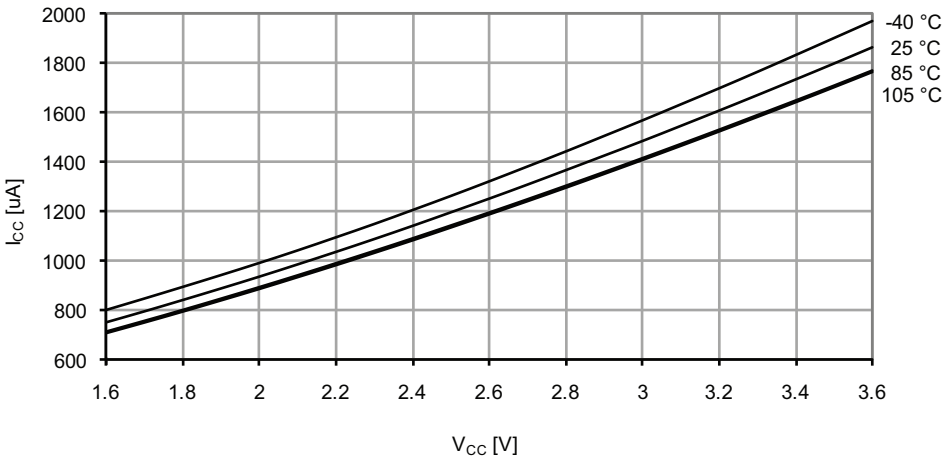


Figure 37-98. Idle mode current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator.

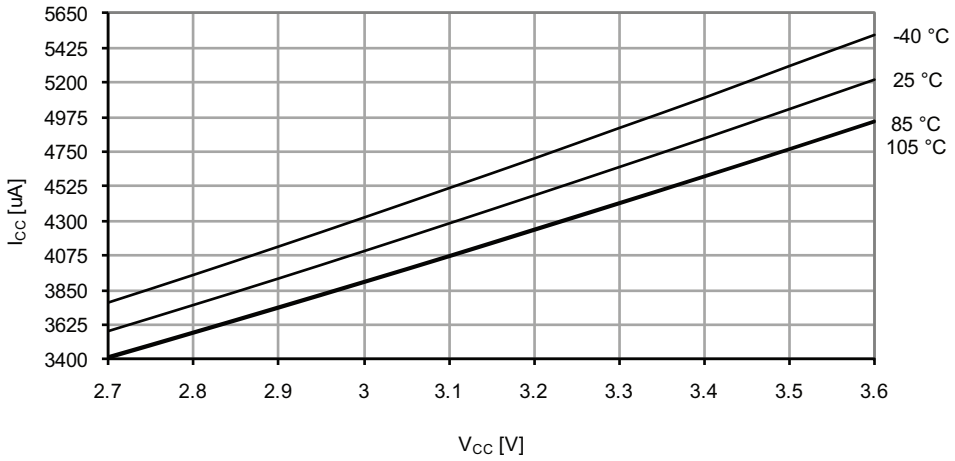


Figure 37-205. INL error vs. sample rate.

T = 25°C, V_{CC} = 2.7V, V_{REF} = 1.0V external.

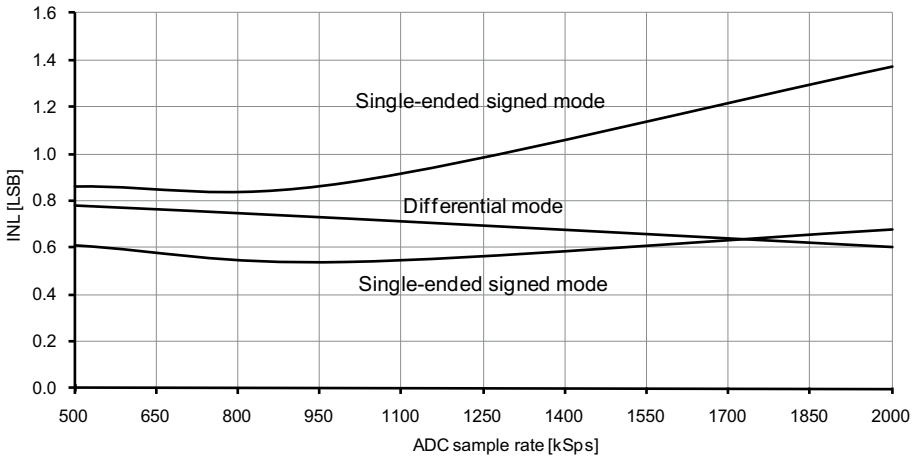
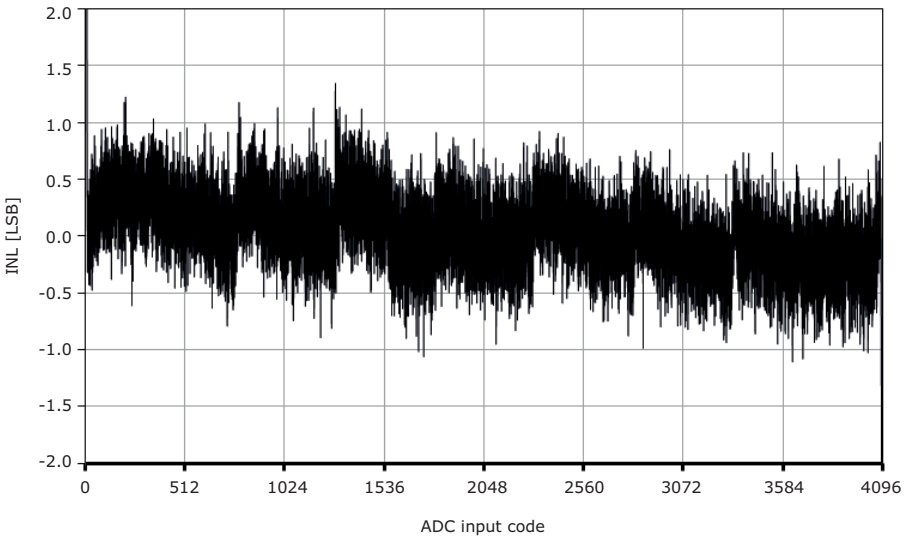


Figure 37-206. INL error vs. input code



37.3.10.3 2MHz Internal Oscillator

Figure 37-241. 2MHz internal oscillator frequency vs. temperature.

DFLL disabled.

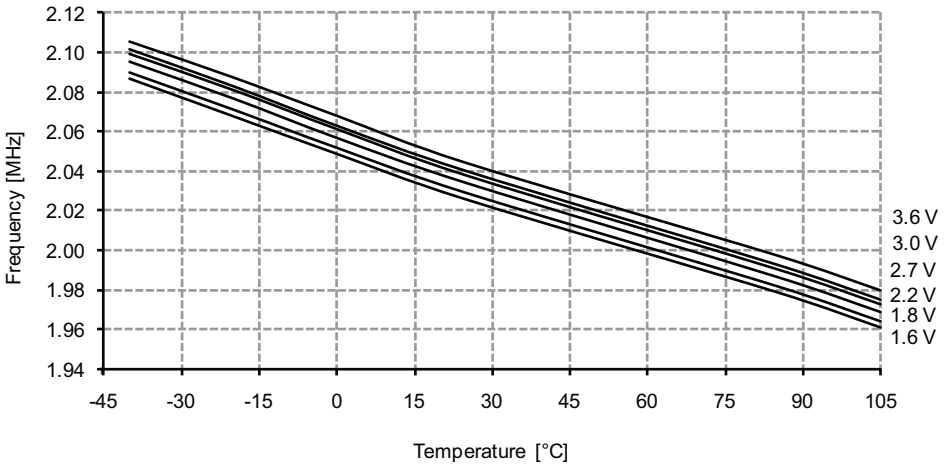


Figure 37-242. 2MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator .

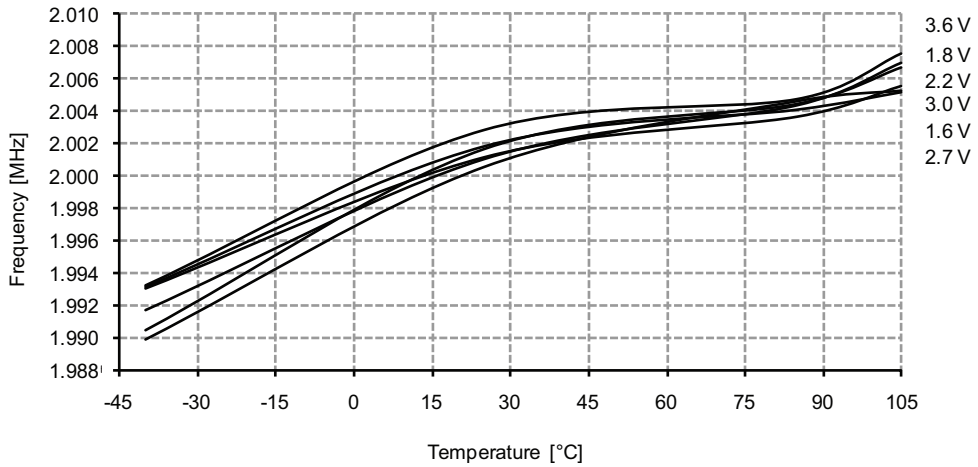
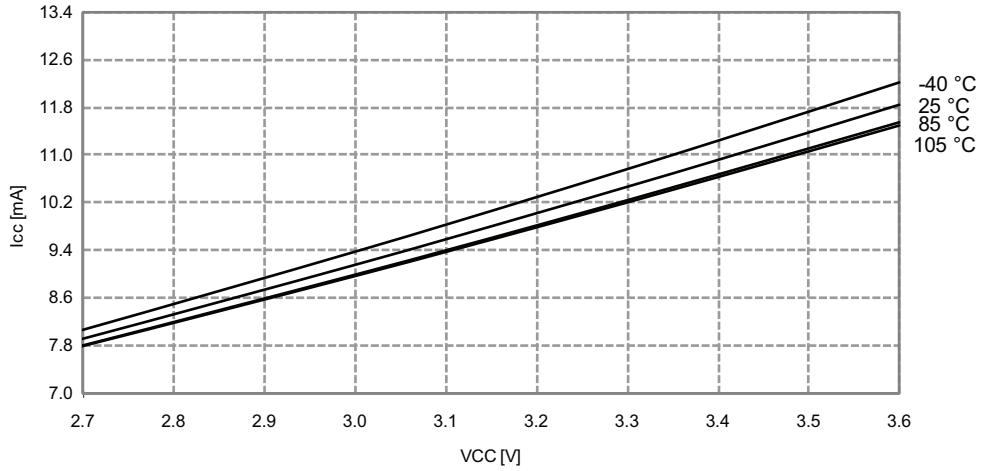


Figure 37-259. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator.



37.4.1.2 Idle mode supply current

Figure 37-260. Idle mode supply current vs. frequency.

f_{SYS} = 0 - 1MHz external clock, T = 25°C

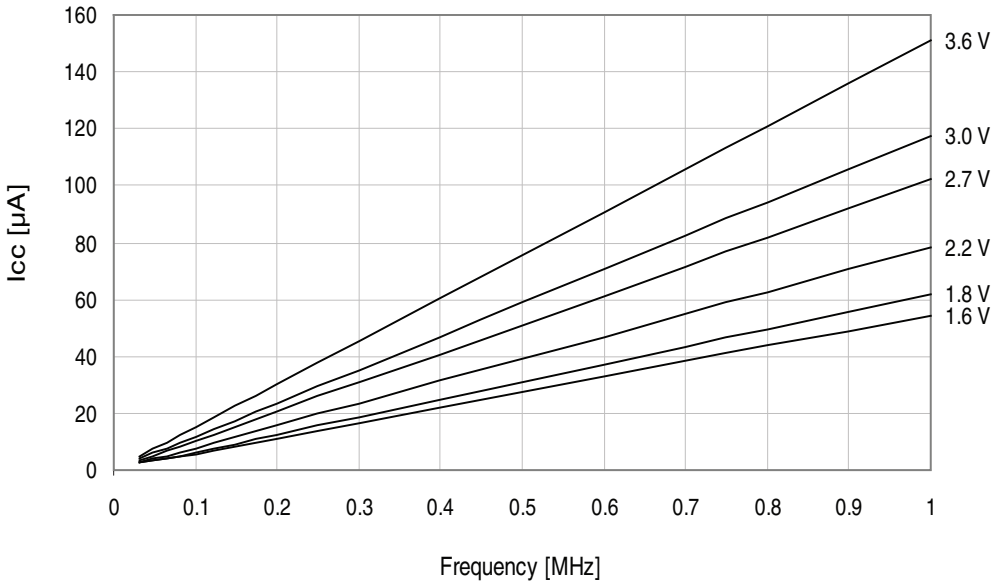


Figure 37-281. I/O pin output voltage vs. sink current.

V_{CC} = 3.0V

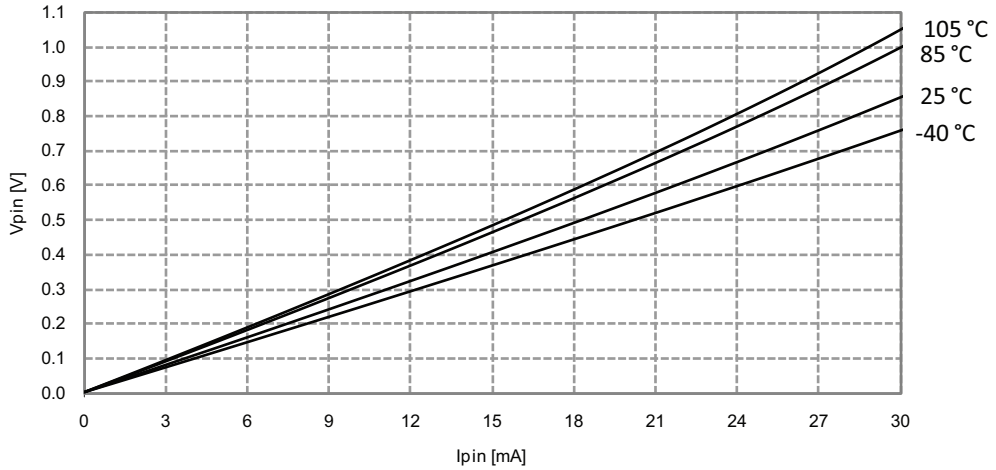
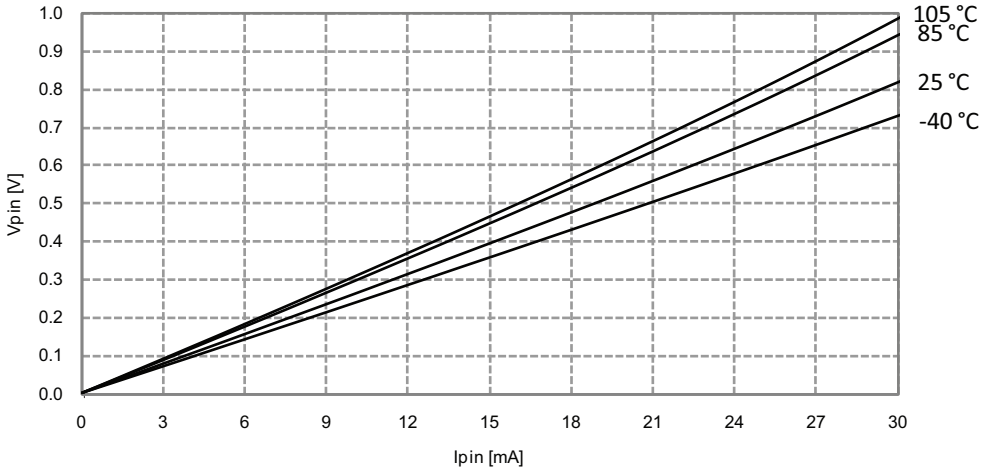


Figure 37-282. I/O pin output voltage vs. sink current.

V_{CC} = 3.3V



37.4.4 DAC Characteristics

Figure 37-301. DAC INL error vs. V_{REF}

V_{CC} = 3.6V

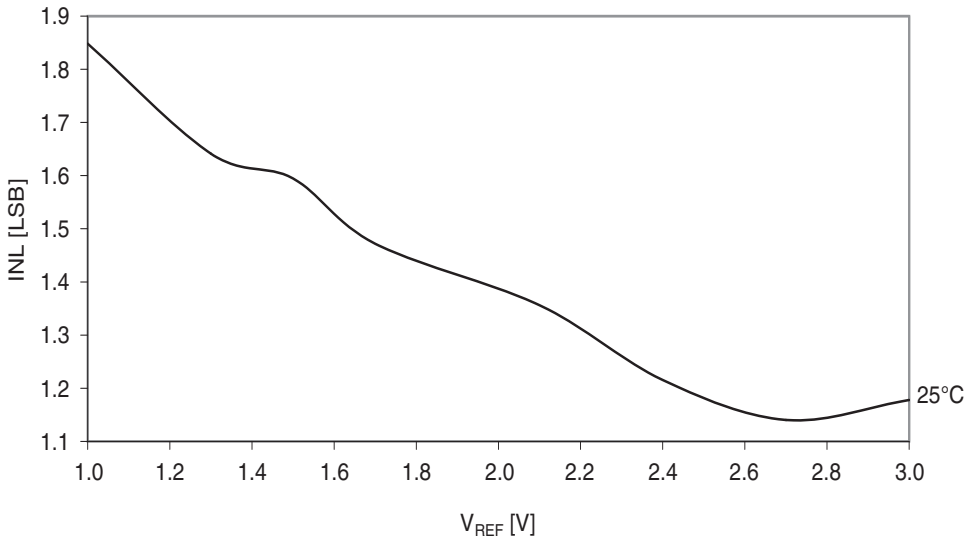


Figure 37-302. DNL error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V.