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What is "Embedded - Microcontrollers"?

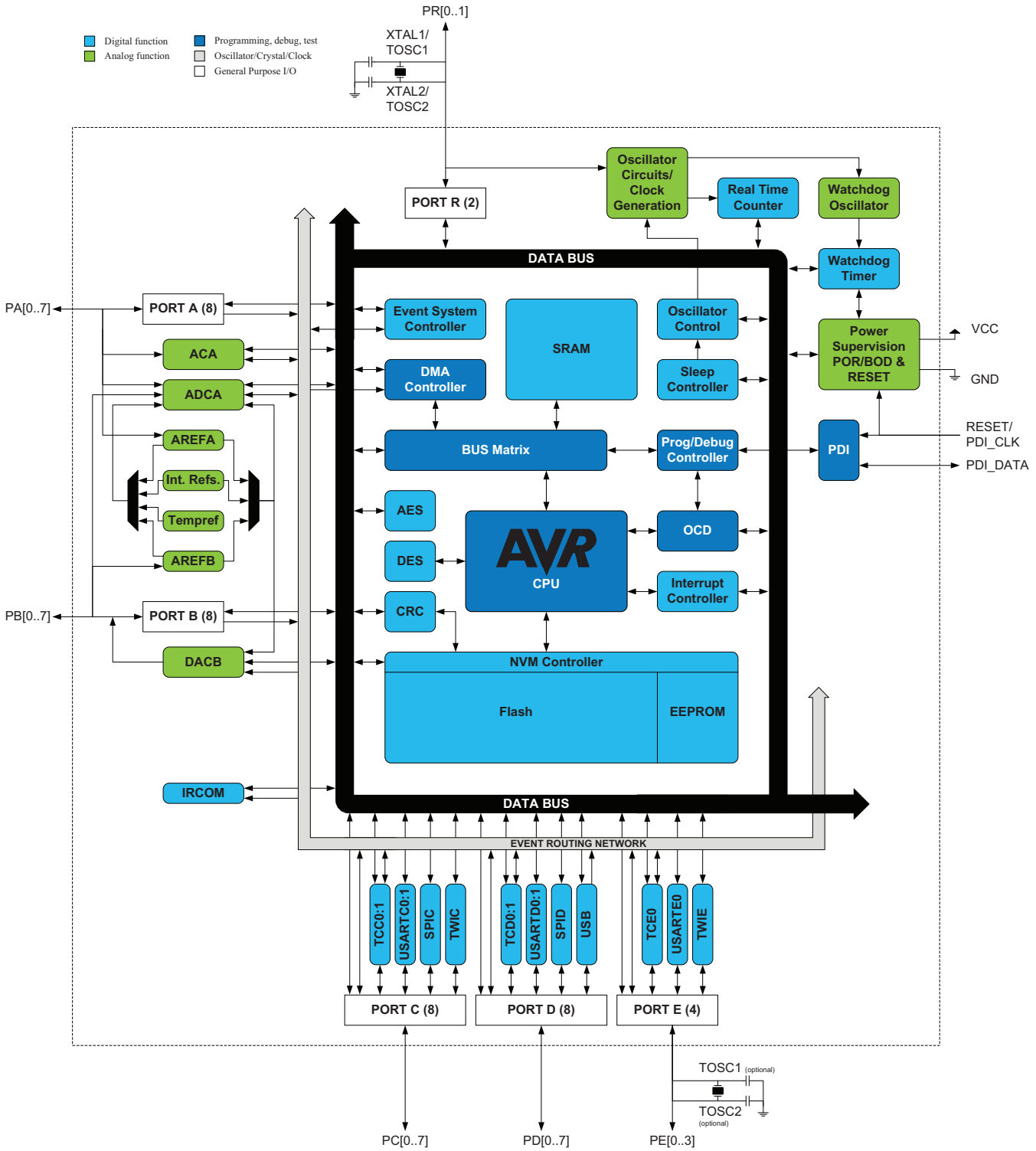
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64a4u-aur

3.1 Block Diagram

Figure 3-1. XMEGA A4U Block Diagram



7.3 Flash Program Memory

The Atmel AVR XMEGA devices contain on-chip, in-system reprogrammable flash memory for program storage. The flash memory can be accessed for read and write from an external programmer through the PDI or from application software running in the device.

All AVR CPU instructions are 16 or 32 bits wide, and each flash location is 16 bits wide. The flash memory is organized in two main sections, the application section and the boot loader section. The sizes of the different sections are fixed, but device-dependent. These two sections have separate lock bits, and can have different levels of protection. The store program memory (SPM) instruction, which is used to write to the flash from the application software, will only operate when executed from the boot loader section.

The application section contains an application table section with separate lock settings. This enables safe storage of nonvolatile data in the program memory.

Table 7-1. Flash Program Memory (Hexadecimal address).

Word Address				
ATxmega128A4U	ATxmega64A4U	ATxmega32A4U	ATxmega16A4U	
0	0	0	0	Application Section (128K/64K/32K/16K)
				...
EFFF /	77FF /	37FF /	17FF	
F000 /	7800 /	3800 /	1800	Application Table Section (8K/4K/4K/4K)
FFFF /	7FFF /	3FFF /	1FFF	
10000 /	8000 /	4000 /	2000	Boot Section (8K/4K/4K/4K)
10FFF /	87FF /	47FF /	27FF	

7.3.1 Application Section

The Application section is the section of the flash that is used for storing the executable application code. The protection level for the application section can be selected by the boot lock bits for this section. The application section can not store any boot loader code since the SPM instruction cannot be executed from the application section.

7.3.2 Application Table Section

The application table section is a part of the application section of the flash memory that can be used for storing data. The size is identical to the boot loader section. The protection level for the application table section can be selected by the boot lock bits for this section. The possibilities for different protection levels on the application section and the application table section enable safe parameter storage in the program memory. If this section is not used for data, application code can reside here.

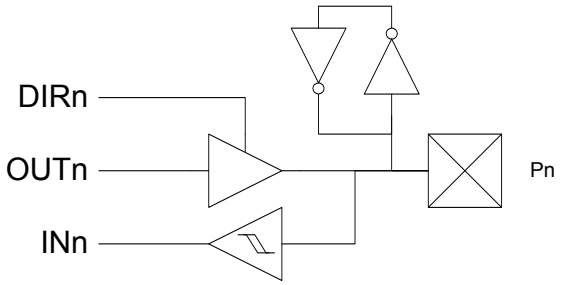
7.3.3 Boot Loader Section

While the application section is used for storing the application code, the boot loader software must be located in the boot loader section because the SPM instruction can only initiate programming when executing from this section. The SPM instruction can access the entire flash, including the boot loader section itself. The protection level for the boot loader section can be selected by the boot loader lock bits. If this section is not used for boot loader software, application code can be stored here.

Table 7-4. Number of bytes and pages in the EEPROM.

Devices	EEPROM	Page Size	E2BYTE	E2PAGE	No of Pages
	Size	bytes			
ATxmega16A4U	1K	32	ADDR[4:0]	ADDR[10:5]	32
ATxmega32A4U	1K	32	ADDR[4:0]	ADDR[10:5]	32
ATxmega64A4U	2K	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega128A4U	2K	32	ADDR[4:0]	ADDR[10:5]	64

Figure 15-4. I/O configuration - Totem-pole with bus-keeper.



15.3.5 Others

Figure 15-5. Output configuration - Wired-OR with optional pull-down.

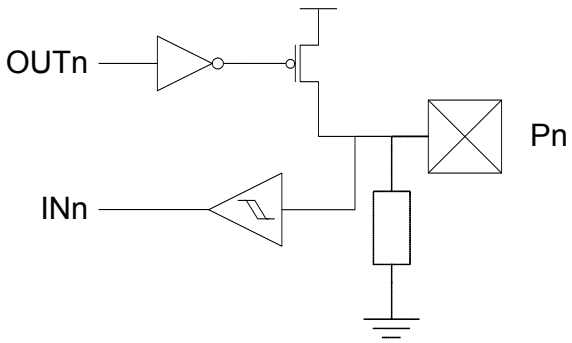
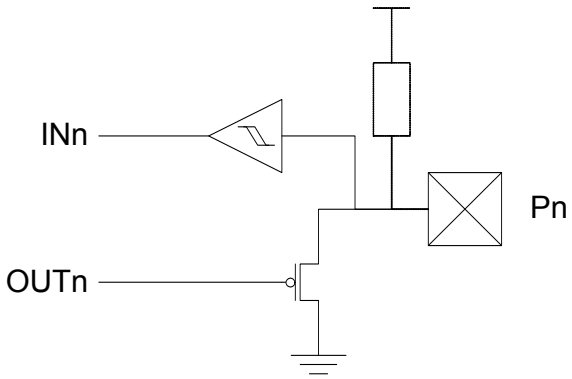


Figure 15-6. I/O configuration - Wired-AND with optional pull-up.



27. CRC – Cyclic Redundancy Check Generator

27.1 Features

- Cyclic redundancy check (CRC) generation and checking for
  - Communication data
  - Program or data in flash memory
  - Data in SRAM and I/O memory space
- Integrated with flash memory, DMA controller and CPU
  - Continuous CRC on data going through a DMA channel
  - Automatic CRC of the complete or a selectable range of the flash memory
  - CPU can load data to the CRC generator through the I/O interface
- CRC polynomial software selectable to
  - CRC-16 (CRC-CCITT)
  - CRC-32 (IEEE 802.3)
- Zero remainder detection

27.2 Overview

A cyclic redundancy check (CRC) is an error detection technique test algorithm used to find accidental errors in data, and it is commonly used to determine the correctness of a data transmission, and data present in the data and program memories. A CRC takes a data stream or a block of data as input and generates a 16- or 32-bit output that can be appended to the data and used as a checksum. When the same data are later received or read, the device or application repeats the calculation. If the new CRC result does not match the one calculated earlier, the block contains a data error. The application will then detect this and may take a corrective action, such as requesting the data to be sent again or simply not using the incorrect data.

Typically, an n-bit CRC applied to a data block of arbitrary length will detect any single error burst not longer than n bits (any single alteration that spans no more than n bits of the data), and will detect the fraction $1-2^{-n}$ of all longer error bursts. The CRC module in Atmel AVR XMEGA devices supports two commonly used CRC polynomials; CRC-16 (CRC-CCITT) and CRC-32 (IEEE 802.3).

- **CRC-16:**

Polynomial:	$x^{16}+x^{12}+x^5+1$
Hex value:	0x1021

- **CRC-32:**

Polynomial:	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$
Hex value:	0x04C11DB7

32.1.5 Communication functions

SCL	Serial Clock for TWI
SDA	Serial Data for TWI
SCLIN	Serial Clock In for TWI when external driver interface is enabled
SCLOUT	Serial Clock Out for TWI when external driver interface is enabled
SDAIN	Serial Data In for TWI when external driver interface is enabled
SDAOUT	Serial Data Out for TWI when external driver interface is enabled
XCKn	Transfer Clock for USART n
RXDn	Receiver Data for USART n
TXDn	Transmitter Data for USART n
SS	Slave Select for SPI
MOSI	Master Out Slave In for SPI
MISO	Master In Slave Out for SPI
SCK	Serial Clock for SPI
D-	Data- for USB
D+	Data+ for USB

32.1.6 Oscillators, Clock and Event

TOSCn	Timer Oscillator pin n
XTALn	Input/Output for Oscillator pin n
CLKOUT	Peripheral Clock Output
EVOUT	Event Channel Output
RTCOUT	RTC Clock Source Output

32.1.7 Debug/System functions

RESET	Reset pin
PDI_CLK	Program and Debug Interface Clock pin
PDI_DATA	Program and Debug Interface Data pin

32.2 Alternate Pin Functions

The tables below show the primary/default function for each pin on a port in the first column, the pin number in the second column, and then all alternate pin functions in the remaining columns. The head row shows what peripheral that enable and use the alternate pin functions.

For better flexibility, some alternate functions also have selectable pin locations for their functions, this is noted under the first table where this apply.

Table 32-1. Port A - alternate functions.

PORT A	PIN #	INTERRUPT	ADCA POS/ GAINPOS	ADCA NEG	ADCA GAINNEG	ACA POS	ACA NEG	ACAOUT	REFA
GND	38								
AVCC	39								
PA0	40	SYNC	ADC0	ADC0		AC0	AC0		AREF
PA1	41	SYNC	ADC1	ADC1		AC1	AC1		
PA2	42	SYNC/ASYNC	ADC2	ADC2		AC2			
PA3	43	SYNC	ADC3	ADC3		AC3	AC3		
PA4	44	SYNC	ADC4		ADC4	AC4			
PA5	1	SYNC	ADC5		ADC5	AC5	AC5		
PA6	2	SYNC	ADC6		ADC6	AC6		AC1OUT	
PA7	3	SYNC	ADC7		ADC7		AC7	AC0OUT	

Table 32-2. Port B - alternate functions.

PORT B	PIN #	INTERRUPT	ADCA POS	DACB	REFB
PB0	4	SYNC	ADC8		AREF
PB1	5	SYNC	ADC9		
PB2	6	SYNC/ASYNC	ADC10	DAC0	
PB3	7	SYNC	ADC11	DAC1	

Table 36-28. External clock with prescaler [1] for system clock.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency [2]	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes:
1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

36.1.14.7 External 16MHz crystal oscillator and XOSC characteristic

Table 36-29. External 16MHz crystal oscillator and XOSC characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0		<10		ns
			FRQRANGE=1, 2, or 3		<1.0		
		XOSCPWR=1			<1.0		
	Long term jitter	XOSCPWR=0	FRQRANGE=0		<6.0		ns
			FRQRANGE=1, 2, or 3		<0.5		
		XOSCPWR=1			<0.5		
	Frequency error	XOSCPWR=0	FRQRANGE=0		<0.1		%
			FRQRANGE=1		<0.05		
			FRQRANGE=2 or 3		<0.005		
		XOSCPWR=1			<0.005		

36.4.13 Flash and EEPROM Memory Characteristics

Table 36-116. Endurance and data retention.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/Erase cycles	25°C	10K			Cycle
			85°C	10K			
			105°C	2K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			
	EEPROM	Write/Erase cycles	25°C	100K			Cycle
			85°C	100K			
			105°C	30K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			

Table 36-117. Programming time.

Symbol	Parameter	Condition	Min.	Typ.(1)	Max.	Units
	Chip Erase	128KB Flash, EEPROM(2) and SRAM Erase		75		ms
	Application Erase	Section erase		6		ms
	Flash	Page erase		4		ms
		Page write		4		
		Atomic page erase and write		8		
	EEPROM	Page erase		4		ms
		Page write		4		
		Atomic page erase and write		8		

Notes: 1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

Figure 37-5. Active mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.

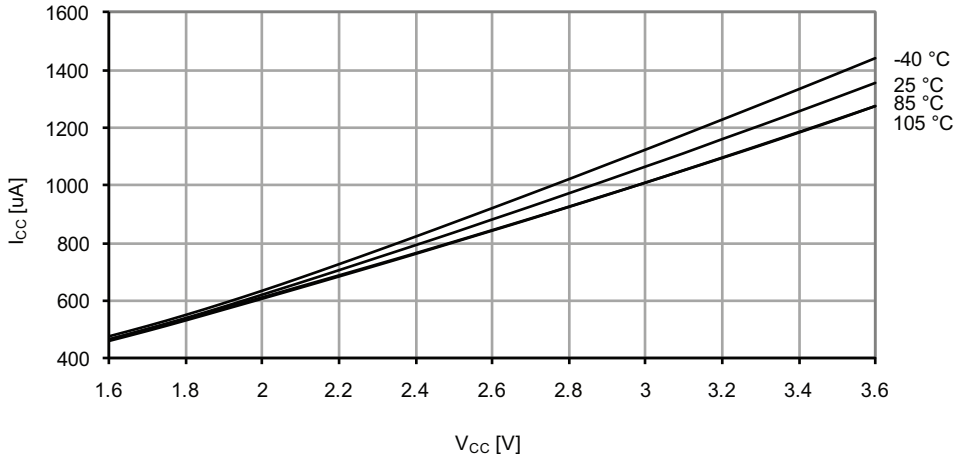


Figure 37-6. Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

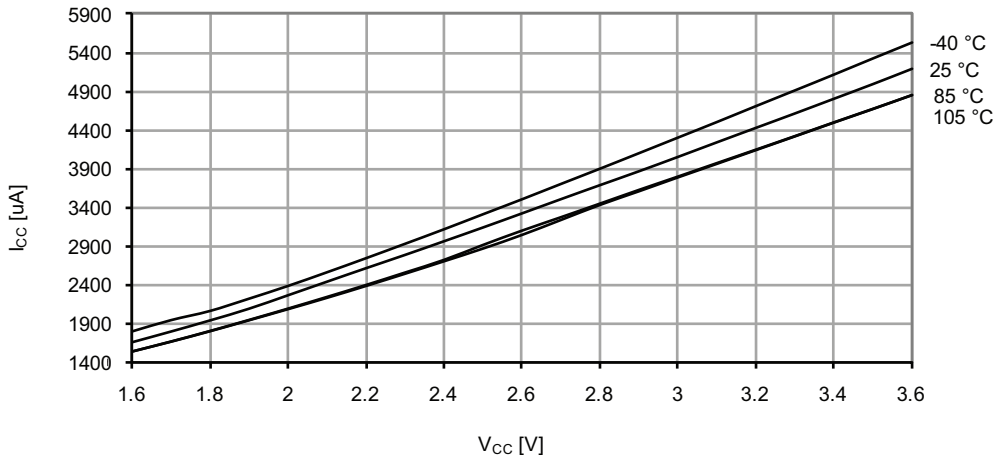


Figure 37-11. Idle mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

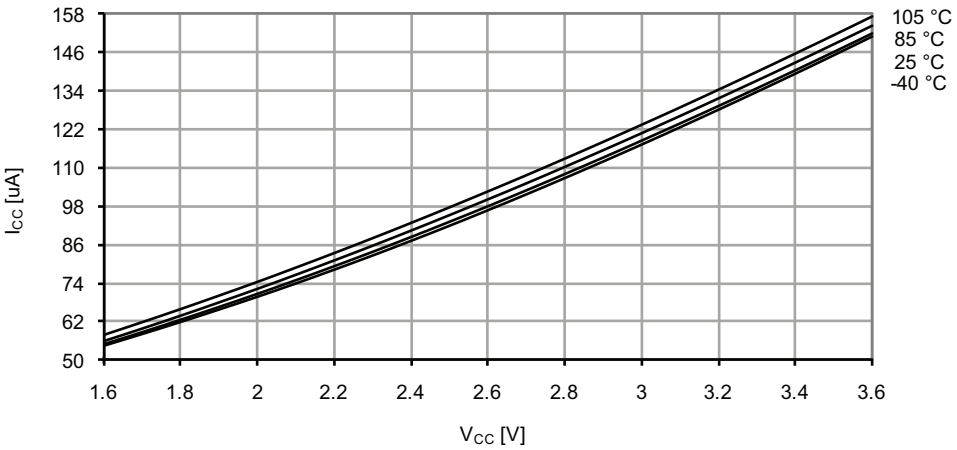
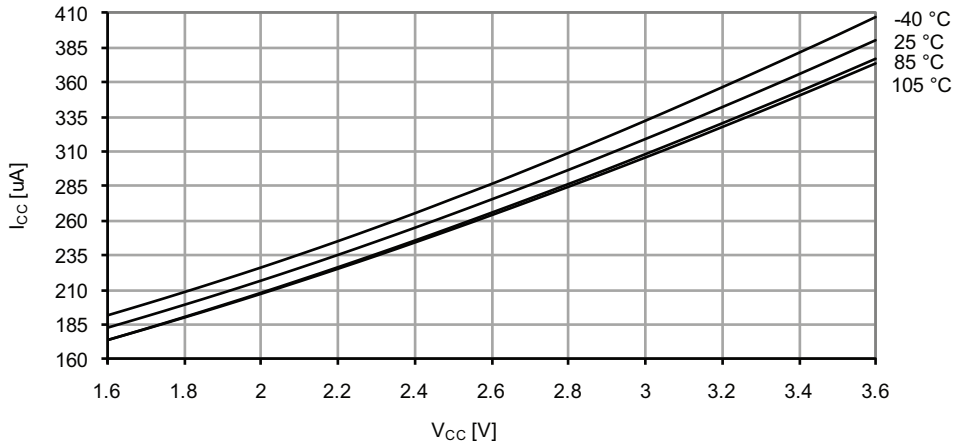


Figure 37-12. Idle mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.



37.1.8 External Reset Characteristics

Figure 37-62. Minimum Reset pin pulse width vs. V_{CC}.

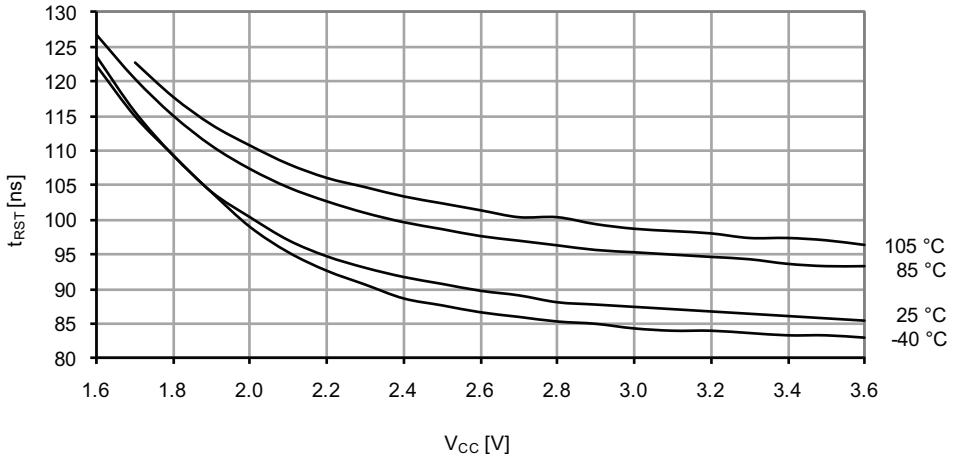


Figure 37-63. Reset pin pull-up resistor current vs. reset pin voltage.
V_{CC} = 1.8V.

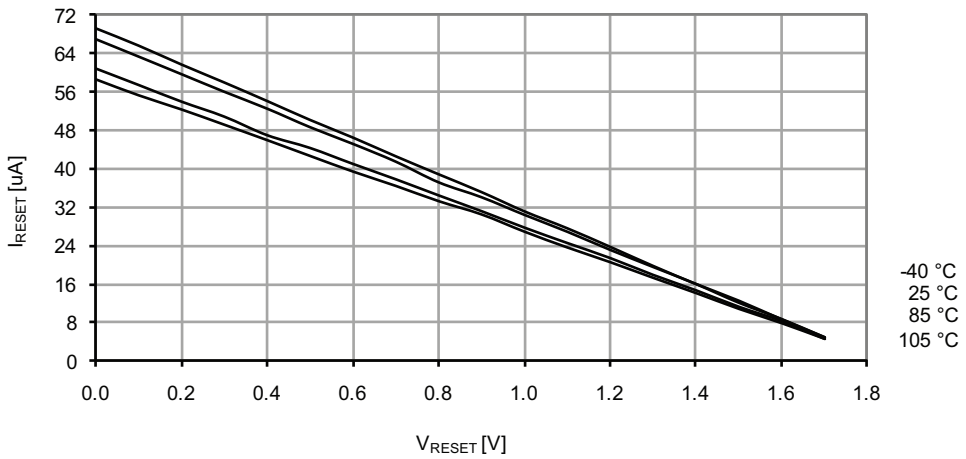


Figure 37-126. Gain error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps.

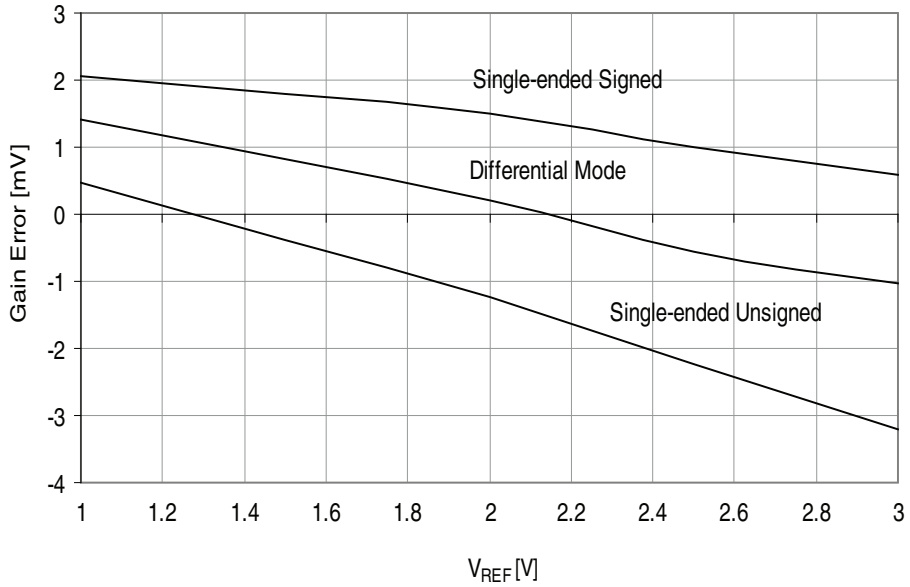


Figure 37-127. Gain error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.

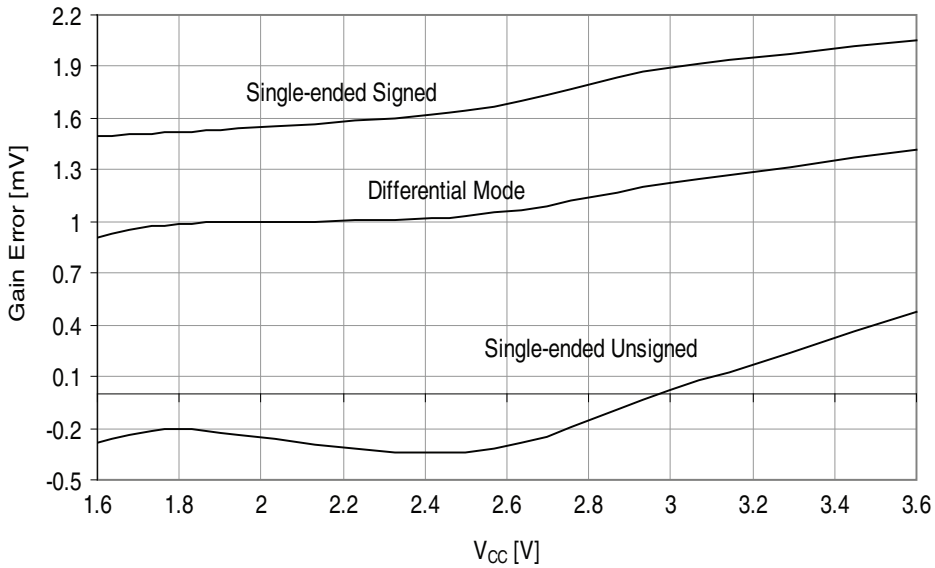
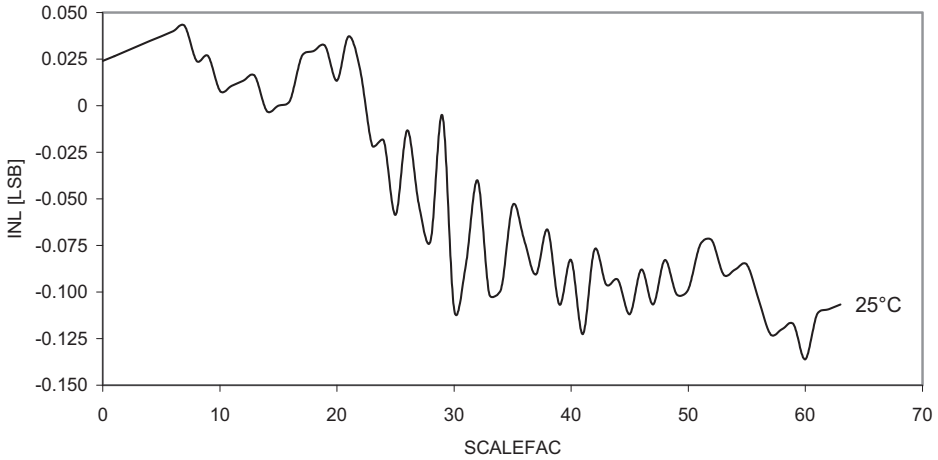


Figure 37-142. Voltage scaler INL vs. SCALEFAC.

T = 25°C, V_{CC} = 3.0V.



37.2.6 Internal 1.0V reference Characteristics

Figure 37-143. ADC/DAC Internal 1.0V reference vs. temperature.

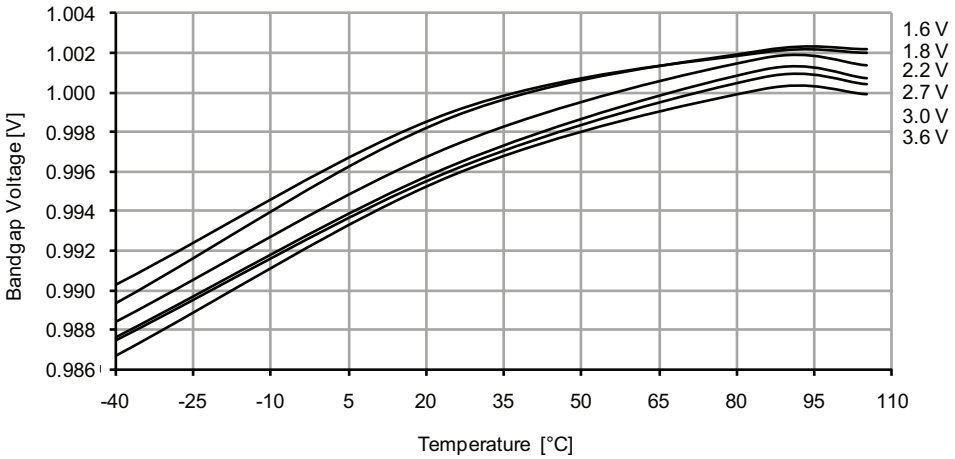


Figure 37-150. Reset pin input threshold voltage vs. V_{CC}.

V_{IH} - Reset pin read as "1".

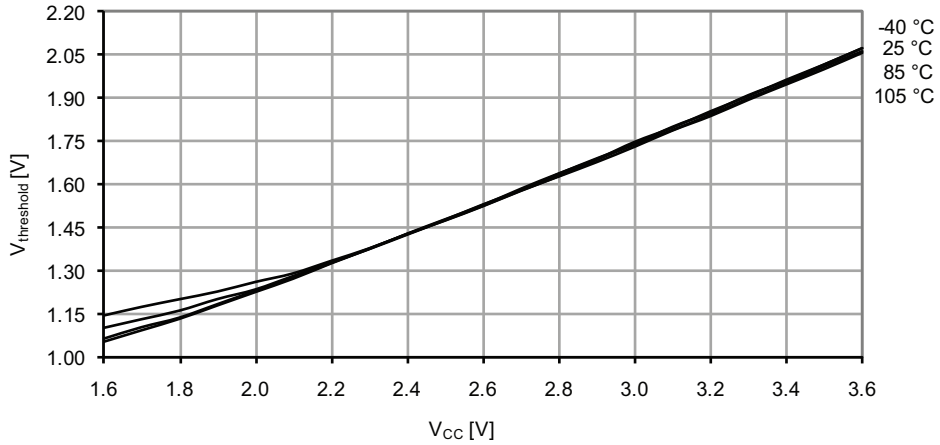


Figure 37-151. Reset pin input threshold voltage vs. V_{CC}.

V_{IL} - Reset pin read as "0".

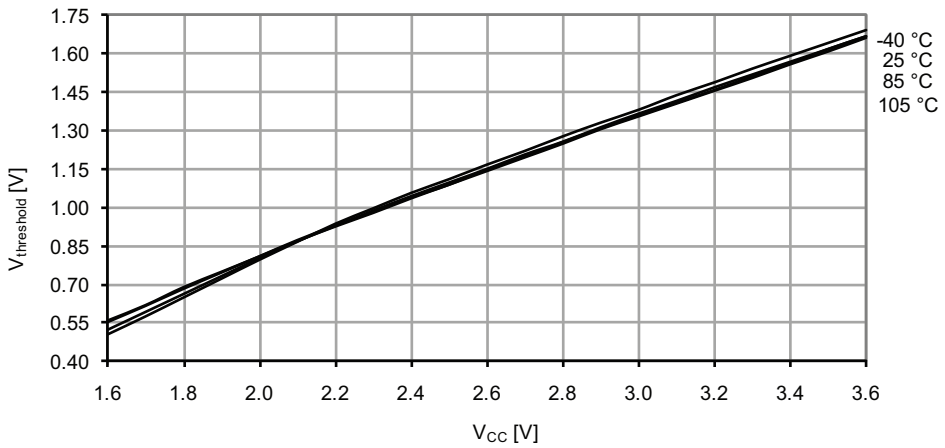


Figure 37-158. 2MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator .

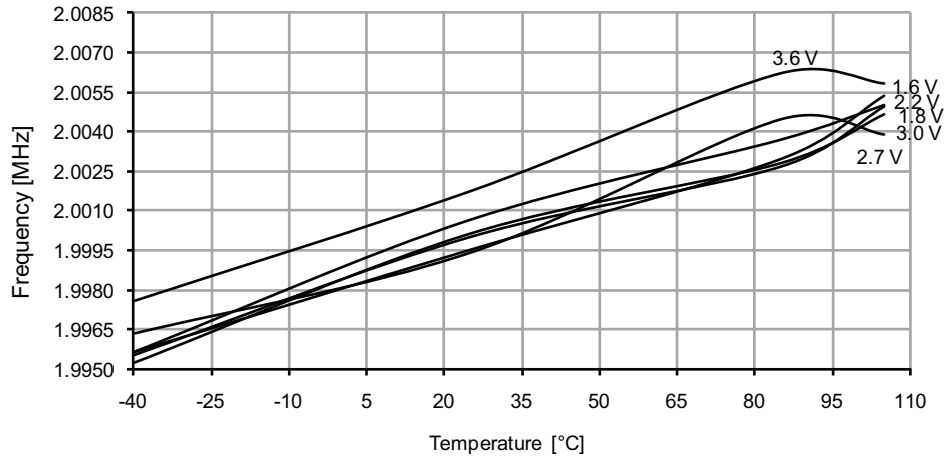


Figure 37-159. 2MHz internal oscillator CALA calibration step size.

V_{CC} = 3V.

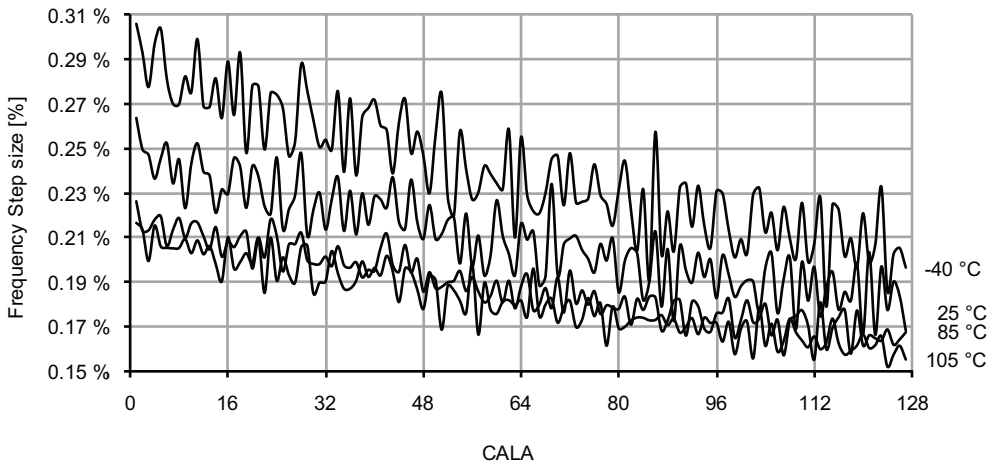


Figure 37-177. Idle mode supply current vs. frequency.

f_{SYS} = 1 - 32MHz external clock, T = 25°C.

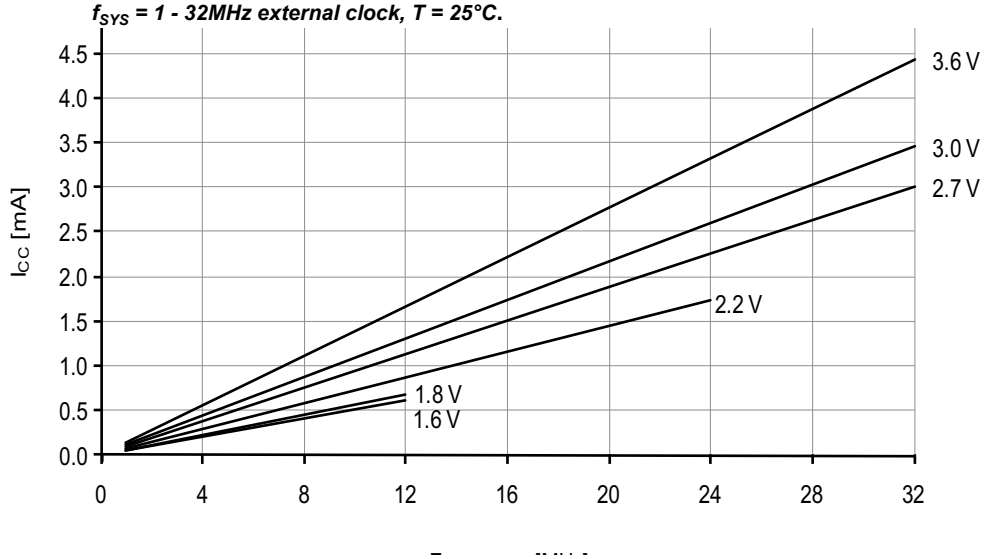
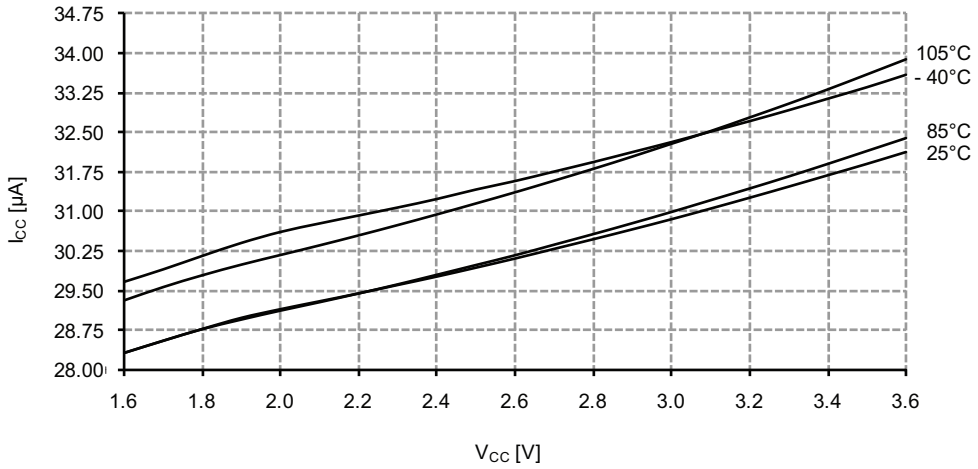


Figure 37-178. Idle mode supply current vs. V_{CC}.

f_{SYS} = 32.768kHz internal oscillator.



37.3.10.3 2MHz Internal Oscillator

Figure 37-241. 2MHz internal oscillator frequency vs. temperature.

DFLL disabled.

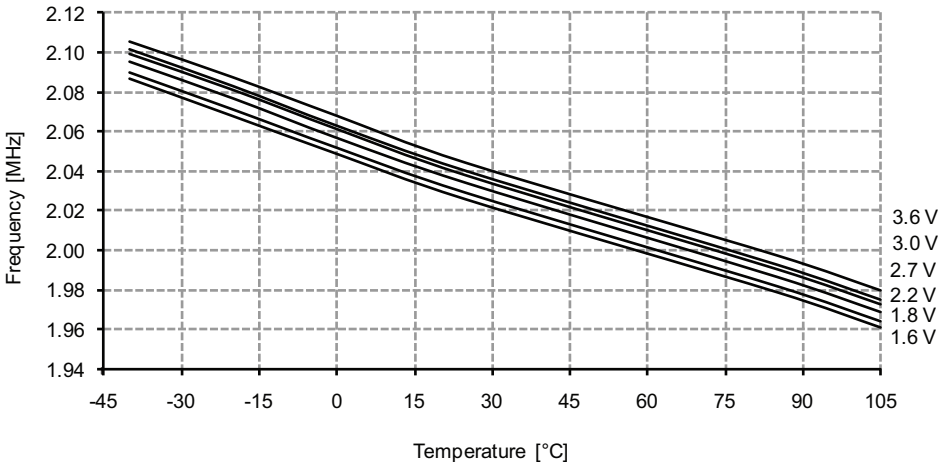
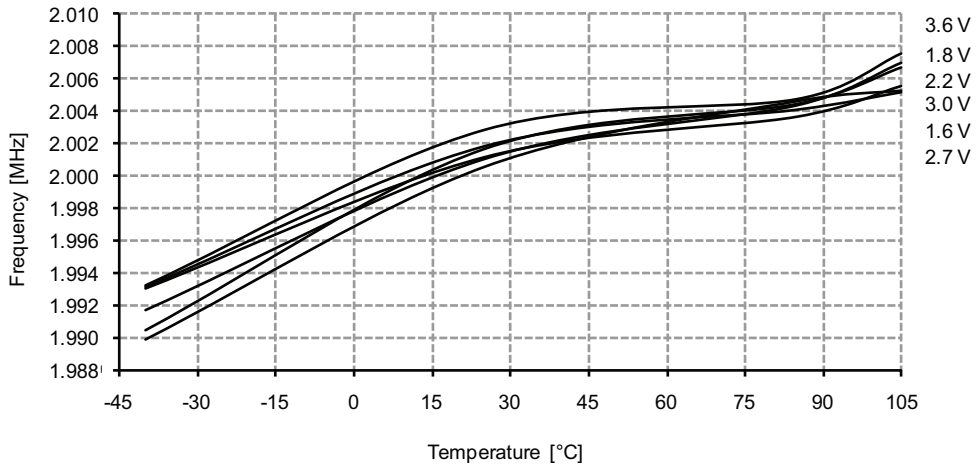


Figure 37-242. 2MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator .



37.4.1.3 Power-down mode supply current

Figure 37-267. Power-down mode supply current vs. temperature.

All functions disabled

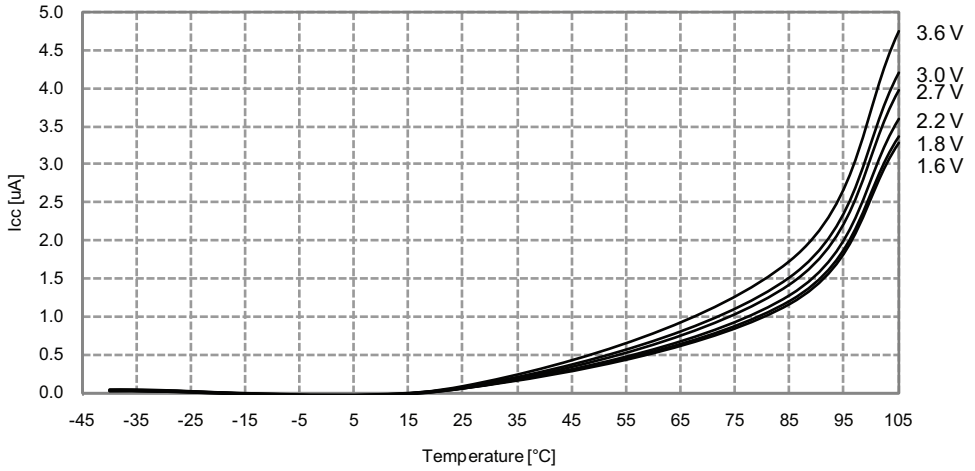
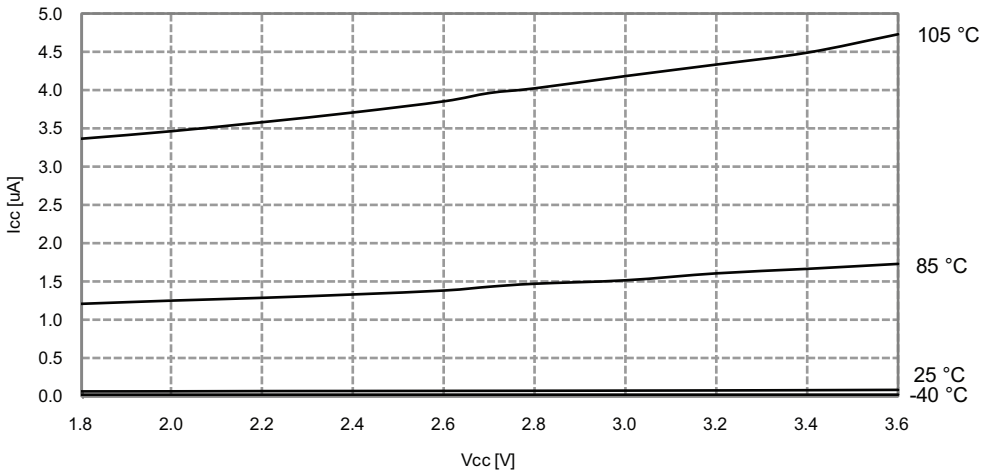


Figure 37-268. Power-down mode supply current vs. V_{CC}.

All functions disabled



37.4.4 DAC Characteristics

Figure 37-301. DAC INL error vs. V_{REF}

V_{CC} = 3.6V

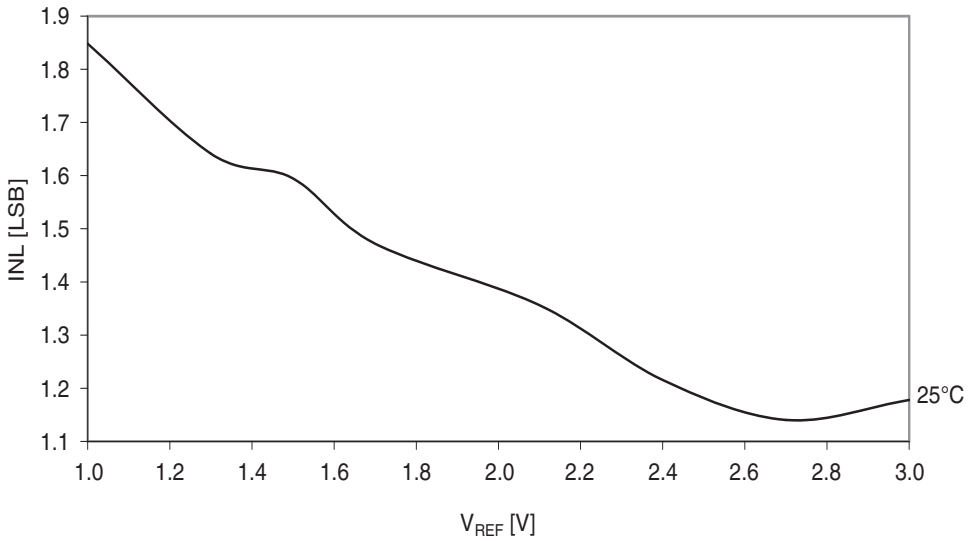


Figure 37-302. DNL error vs. V_{REF}.

T = 25°C, V_{CC} = 3.6V.