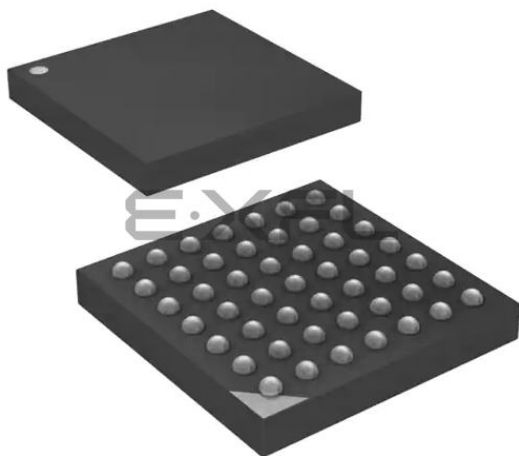




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Details

Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	49-VFBGA
Supplier Device Package	49-VFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64a4u-cu

9. Event System

9.1 Features

- System for direct peripheral-to-peripheral communication and signaling
- Peripherals can directly send, receive, and react to peripheral events
 - CPU and DMA controller independent operation
 - 100% predictable signal timing
 - Short and guaranteed response time
- Eight event channels for up to eight different and parallel signal routing configurations
- Events can be sent and/or used by most peripherals, clock system, and software
- Additional functions include
 - Quadrature decoders
 - Digital filtering of I/O pin state
- Works in active mode and idle sleep mode

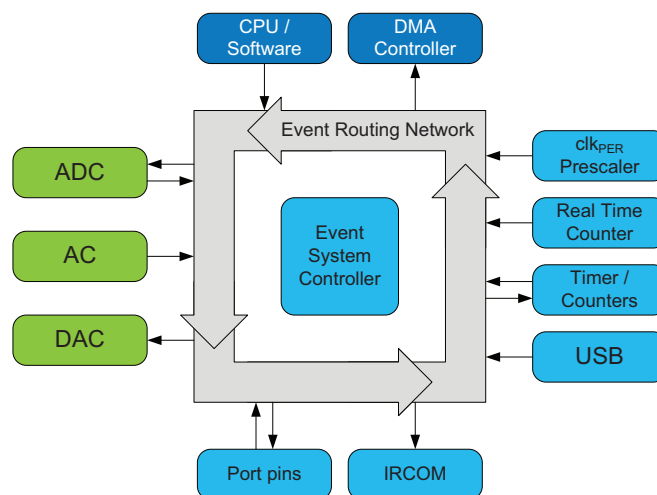
9.2 Overview

The event system enables direct peripheral-to-peripheral communication and signaling. It allows a change in one peripheral's state to automatically trigger actions in other peripherals. It is designed to provide a predictable system for short and predictable response times between peripherals. It allows for autonomous peripheral control and interaction without the use of interrupts, CPU, or DMA controller resources, and is thus a powerful tool for reducing the complexity, size and execution time of application code. It also allows for synchronized timing of actions in several peripheral modules.

A change in a peripheral's state is referred to as an event, and usually corresponds to the peripheral's interrupt conditions. Events can be directly passed to other peripherals using a dedicated routing network called the event routing network. How events are routed and used by the peripherals is configured in software.

Figure 9-1 on page 20 shows a basic diagram of all connected peripherals. The event system can directly connect together analog and digital converters, analog comparators, I/O port pins, the real-time counter, timer/counters, IR communication module (IRCOM), and USB interface. It can also be used to trigger DMA transactions (DMA controller). Events can also be generated from software and the peripheral clock.

Figure 9-1. Event system overview and connected peripherals.



The event routing network consists of eight software-configurable multiplexers that control how events are routed and used. These are called event channels, and allow for up to eight parallel event routing configurations. The maximum routing latency is two peripheral clock cycles. The event system works in both active mode and idle sleep mode.

13. WDT – Watchdog Timer

13.1 Features

- Issues a device reset if the timer is not reset before its timeout period
- Asynchronous operation from dedicated oscillator
- 1kHz output of the 32kHz ultra low power oscillator
- 11 selectable timeout periods, from 8ms to 8s
- Two operation modes:
 - Normal mode
 - Window mode
- Configuration lock to prevent unwanted changes

13.2 Overview

The watchdog timer (WDT) is a system function for monitoring correct program operation. It makes it possible to recover from error situations such as runaway or deadlocked code. The WDT is a timer, configured to a predefined timeout period, and is constantly running when enabled. If the WDT is not reset within the timeout period, it will issue a microcontroller reset. The WDT is reset by executing the WDR (watchdog timer reset) instruction from the application code.

The window mode makes it possible to define a time slot or window inside the total timeout period during which WDT must be reset. If the WDT is reset outside this window, either too early or too late, a system reset will be issued. Compared to the normal mode, this can also catch situations where a code error causes constant WDR execution.

The WDT will run in active mode and all sleep modes, if enabled. It is asynchronous, runs from a CPU-independent clock source, and will continue to operate to issue a system reset even if the main clocks fail.

The configuration change protection mechanism ensures that the WDT settings cannot be changed by accident. For increased safety, a fuse for locking the WDT settings is also available.

A DAC conversion is automatically started when new data to be converted are available. Events from the event system can also be used to trigger a conversion, and this enables synchronized and timed conversions between the DAC and other peripherals, such as a timer/counter. The DMA controller can be used to transfer data to the DAC.

The DAC has high drive strength, and is capable of driving both resistive and capacitive loads, as well as loads which combine both. A low-power mode is available, which will reduce the drive strength of the output. Internal and external voltage references can be used. The DAC output is also internally available for use as input to the analog comparator or ADC.

PORTB has one DAC. Notation of this peripheral is DACB.

Mnemonic s	Operand s	Description	Operation	Flags	#Clock s
RCALL	k	Relative Call Subroutine	PC ← PC + k + 1	None	2 / 3 ⁽¹⁾
ICALL		Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2 / 3 ⁽¹⁾
EICALL		Extended Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	3 ⁽¹⁾
CALL	k	call Subroutine	PC ← k	None	3 / 4 ⁽¹⁾
RET		Subroutine Return	PC ← STACK	None	4 / 5 ⁽¹⁾
RETI		Interrupt Return	PC ← STACK	I	4 / 5 ⁽¹⁾
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2 / 3
CP	Rd,Rr	Compare	Rd - Rr	Z,C,N,V,S,H	1
CPC	Rd,Rr	Compare with Carry	Rd - Rr - C	Z,C,N,V,S,H	1
CPI	Rd,K	Compare with Immediate	Rd - K	Z,C,N,V,S,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b) = 0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBRs	Rr, b	Skip if Bit in Register Set	if (Rr(b) = 1) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIC	A, b	Skip if Bit in I/O Register Cleared	if (I/O(A,b) = 0) PC ← PC + 2 or 3	None	2 / 3 / 4
SBIS	A, b	Skip if Bit in I/O Register Set	If (I/O(A,b) = 1) PC ← PC + 2 or 3	None	2 / 3 / 4
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC ← PC + k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC ← PC + k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V = 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than, Signed	if (N ⊕ V = 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2
Data transfer instructions					
MOV	Rd, Rr	Copy Register	Rd ← Rr	None	1

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Offset error, input referred	1x gain, normal mode			-2		mV
		8x gain, normal mode			-5		
		64x gain, normal mode			-4		
	Noise	1x gain, normal mode	$V_{CC} = 3.6V$ Ext. V_{REF}		0.5		mV rms
		8x gain, normal mode			1.5		
		64x gain, normal mode			11		

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.

36.1.7 DAC Characteristics

Table 36-12. Power supply, reference and output range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		$V_{CC} - 0.3$		$V_{CC} + 0.3$	V
AV_{REF}	External reference voltage		1.0		$V_{CC} - 0.6$	V
$R_{channel}$	DC output impedance				50	Ω
	Linear output voltage range		0.15		$AV_{CC} - 0.15$	V
R_{AREF}	Reference input resistance			>10		M Ω
CAREF	Reference input capacitance	Static load		7		pF
	Minimum resistance load		1.0			k Ω
	Maximum capacitance load				100	pF
		1000 Ω serial resistance			1.0	nF
	Output sink/source	Operating within accuracy specification			$AV_{CC}/1000$	mA
		Safe operation			10	

36.2.5 I/O Pin Characteristics

The I/O pins comply with the JEDEC LVTTTL and LVCMOS specification and the high- and low level input and output voltage limits reflect or exceed this specification.

Table 36-39. I/O pin characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
$I_{OH}^{(1)}$ / $I_{OL}^{(2)}$	I/O pin source/sink current			-20		20	mA
V_{IH}	High level input voltage	$V_{CC} = 2.7 - 3.6V$		2.0		$V_{CC}+0.3$	V
		$V_{CC} = 2.0 - 2.7V$		$0.7 \cdot V_{CC}$		$V_{CC}+0.3$	
		$V_{CC} = 1.6 - 2.0V$		$0.8 \cdot V_{CC}$		$V_{CC}+0.3$	
V_{IL}	Low level input voltage	$V_{CC} = 2.7 - 3.6V$		-0.3		0.8	V
		$V_{CC} = 2.0 - 2.7V$		-0.3		$0.3 \cdot V_{CC}$	
		$V_{CC} = 1.6 - 2.0V$		-0.3		$0.2 \cdot V_{CC}$	
V_{OH}	High level output voltage	$V_{CC} = 3.0 - 3.6V$	$I_{OH} = -2mA$	2.4	$0.94 \cdot V_{CC}$		V
		$V_{CC} = 2.3 - 2.7V$	$I_{OH} = -1mA$	2.0	$0.96 \cdot V_{CC}$		
			$I_{OH} = -2mA$	1.7	$0.92 \cdot V_{CC}$		
		$V_{CC} = 3.3V$	$I_{OH} = -8mA$	2.6	2.9		
		$V_{CC} = 3.0V$	$I_{OH} = -6mA$	2.1	2.6		
V_{OL}	Low level output voltage	$V_{CC} = 1.8V$	$I_{OH} = -2mA$	1.4	1.6		V
		$V_{CC} = 3.0 - 3.6V$	$I_{OL} = 2mA$		$0.05 \cdot V_{CC}$	0.4	
		$V_{CC} = 2.3 - 2.7V$	$I_{OL} = 1mA$		$0.03 \cdot V_{CC}$	0.4	
			$I_{OL} = 2mA$		$0.06 \cdot V_{CC}$	0.7	
		$V_{CC} = 3.3V$	$I_{OL} = 15mA$		0.4	0.76	
		$V_{CC} = 3.0V$	$I_{OL} = 10mA$		0.3	0.64	
I_{IN}	Input leakage current	$T = 25^{\circ}C$			<0.01	0.1	μA
R_P	Pull/buss keeper resistor				24		k Ω
t_r	Rise time	No load			4.0		ns
			slew rate limitation		7.0		

- Notes:
1. The sum of all I_{OH} for PORTA and PORTB must not exceed 100mA.
The sum of all I_{OH} for PORTC must not exceed 200mA.
The sum of all I_{OH} for PORTD and pins PE[0-1] on PORTE must not exceed 200mA.
The sum of all I_{OH} for PE[2-3] on PORTE, PORTR and PDI must not exceed 100mA.
 2. The sum of all I_{OL} for PORTA and PORTB must not exceed 100mA.
The sum of all I_{OL} for PORTC must not exceed 200mA.
The sum of all I_{OL} for PORTD and pins PE[0-1] on PORTE must not exceed 200mA.
The sum of all I_{OL} for PE[2-3] on PORTE, PORTR and PDI must not exceed 100mA.

36.3.3 Current consumption

Table 36-68. Current consumption for Active mode and sleep modes.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{CC}	Active power consumption ⁽¹⁾	32kHz, Ext. Clk	$V_{CC} = 1.8V$	52		μA
			$V_{CC} = 3.0V$	132		
		1MHz, Ext. Clk	$V_{CC} = 1.8V$	223		
			$V_{CC} = 3.0V$	476		
		2MHz, Ext. Clk	$V_{CC} = 1.8V$	400	600	mA
			$V_{CC} = 3.0V$	0.8	1.4	
	Idle power consumption ⁽¹⁾	32kHz, Ext. Clk	$V_{CC} = 1.8V$	2.4		μA
			$V_{CC} = 3.0V$	3.5		
		1MHz, Ext. Clk	$V_{CC} = 1.8V$	57		
			$V_{CC} = 3.0V$	110		
		2MHz, Ext. Clk	$V_{CC} = 1.8V$	115	225	mA
			$V_{CC} = 3.0V$	216	350	
	Power-down power consumption	T = 25°C		0.1	1.0	μA
				1.2	4.5	
				2.4	6.0	
		WDT and Sampled BOD enabled, T = 25°C	$V_{CC} = 3.0V$	1.4	3.0	
		WDT and Sampled BOD enabled, T = 85°C		2.4	6.0	
		WDT and Sampled BOD enabled, T = 105°C		3.5	8.0	
	Power-save power consumption ⁽²⁾	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	$V_{CC} = 1.8V$	1.2		μA
			$V_{CC} = 3.0V$	1.5		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	$V_{CC} = 1.8V$	0.6	2.0	
			$V_{CC} = 3.0V$	0.7	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	$V_{CC} = 1.8V$	0.8	3.0	
			$V_{CC} = 3.0V$	1.0	3.0	
	Reset power consumption	Current through $\overline{RESET}$ pin subtracted	$V_{CC} = 3.0V$	140		

- Notes:
1. All Power Reduction Registers set.
 2. Maximum limits are based on characterization, and not tested in production.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Duty cycle	XOSCPWR=0	FRQRANGE=0	40		%
			FRQRANGE=1	42		
			FRQRANGE=2 or 3	45		
		XOSCPWR=1		48		
R _Q	Negative impedance ⁽¹⁾	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF	2.4k		Ω
			1MHz crystal, CL=20pF	8.7k		
			2MHz crystal, CL=20pF	2.1k		
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal	4.2k		
			8MHz crystal	250		
			9MHz crystal	195		
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal	360		
			9MHz crystal	285		
			12MHz crystal	155		
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal	365		
			12MHz crystal	200		
			16MHz crystal	105		
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal	435		
			12MHz crystal	235		
			16MHz crystal	125		
		XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal	495		
			12MHz crystal	270		
			16MHz crystal	145		
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal	305		
			16MHz crystal	160		
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal	380		
			16MHz crystal	205		
	ESR	SF = Safety factor			min(RQ)/SF	kΩ
C _{XTAL1}	Parasitic capacitance XTAL1 pin			5.45		pF
C _{XTAL2}	Parasitic capacitance XTAL2 pin			7.51		pF
C _{LOAD}	Parasitic capacitance load			3.16		pF

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

Figure 37-42. Gain error vs. V_{REF} .

$T = 25^{\circ}\text{C}$, $V_{CC} = 3.6\text{V}$, ADC sampling speed = 500ksps.

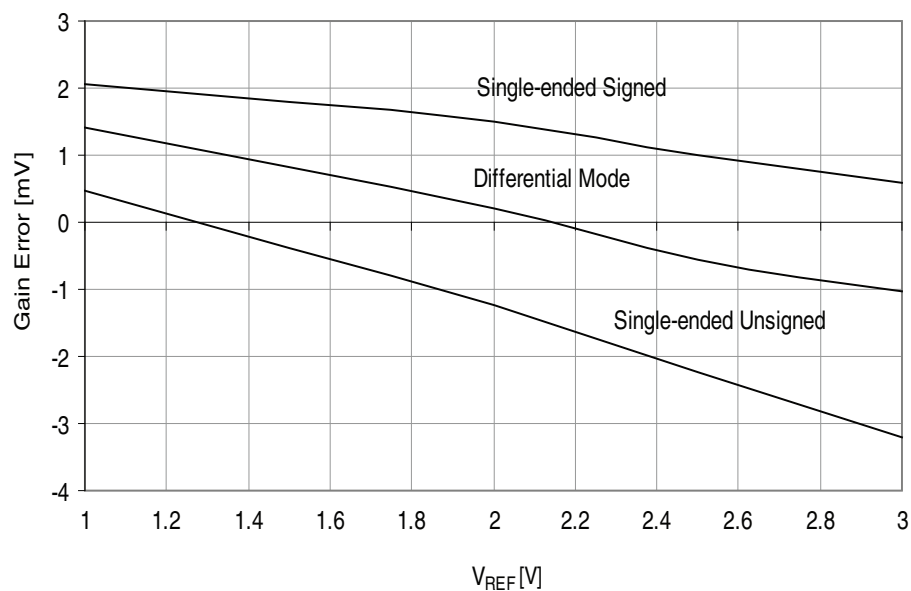
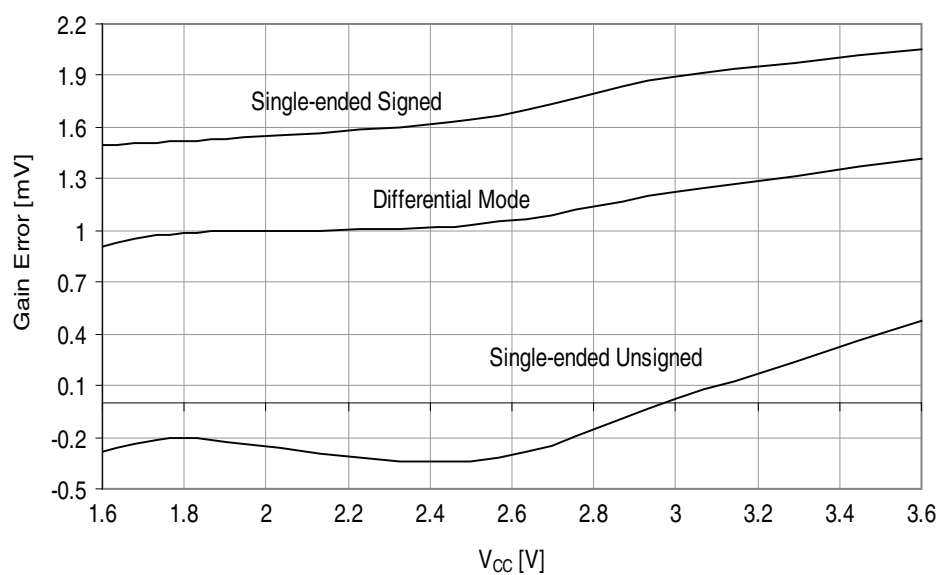


Figure 37-43. Gain error vs. V_{CC} .

$T = 25^{\circ}\text{C}$, $V_{REF} = \text{external } 1.0\text{V}$, ADC sampling speed = 500ksps.



37.1.8 External Reset Characteristics

Figure 37-62. Minimum Reset pin pulse width vs. V_{CC} .

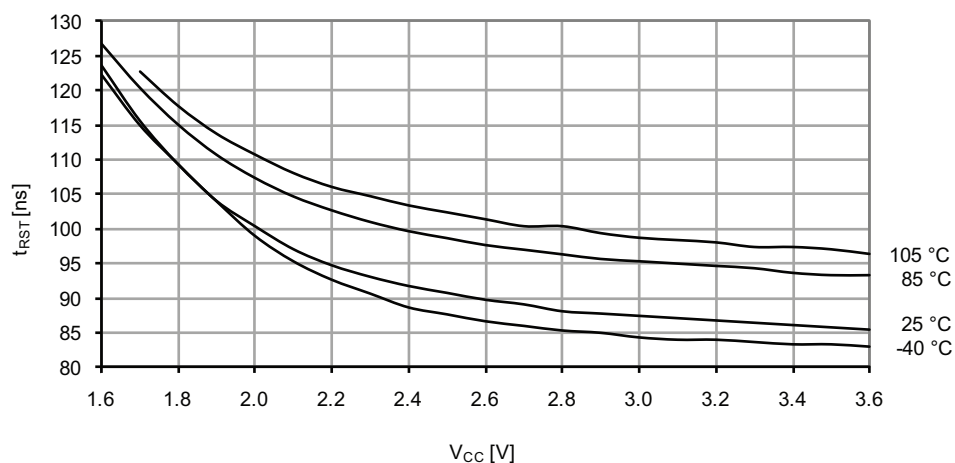


Figure 37-63. Reset pin pull-up resistor current vs. reset pin voltage.

$V_{CC} = 1.8V$.

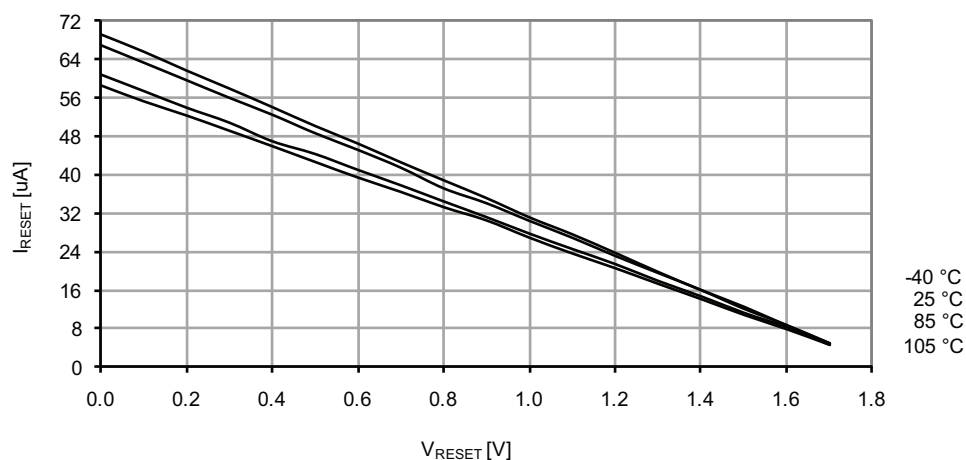


Figure 37-64. Reset pin pull-up resistor current vs. reset pin voltage.

$V_{CC} = 3.0V$.

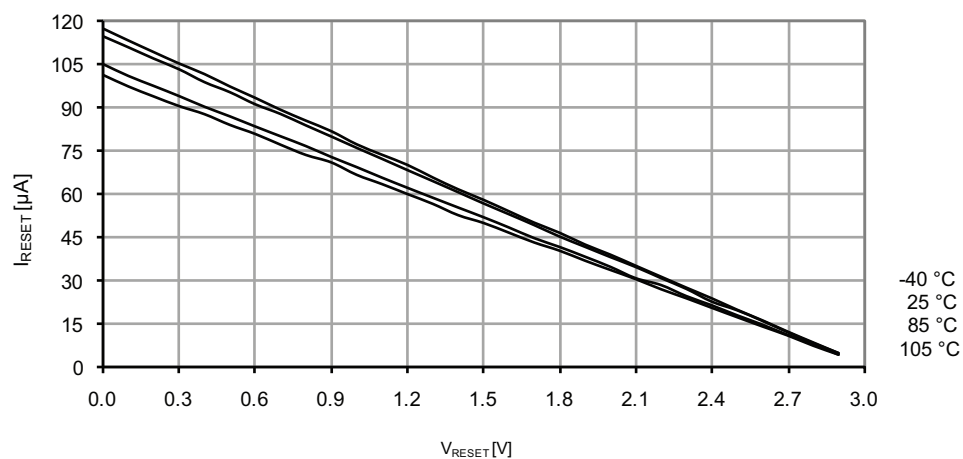


Figure 37-65. Reset pin pull-up resistor current vs. reset pin voltage.

$V_{CC} = 3.3V$.

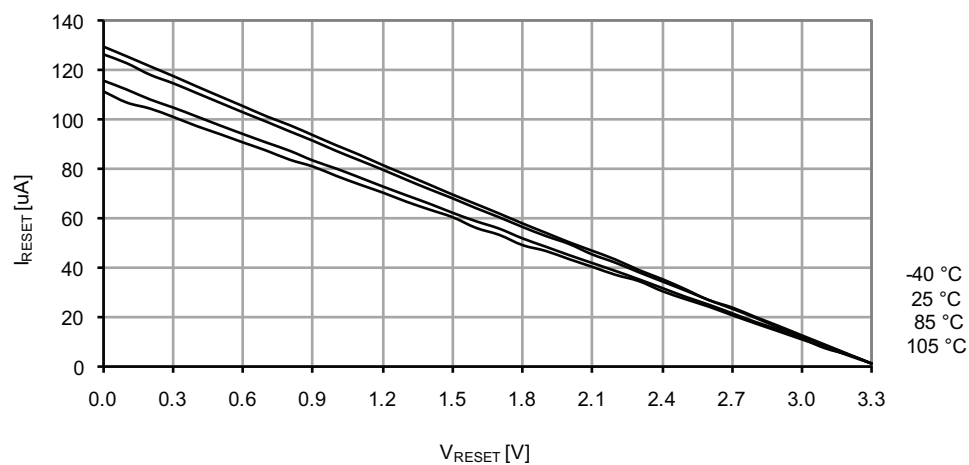


Figure 37-97. Idle mode supply current vs. V_{CC} .

$f_{SYS} = 32\text{MHz}$ internal oscillator prescaled to 8MHz.

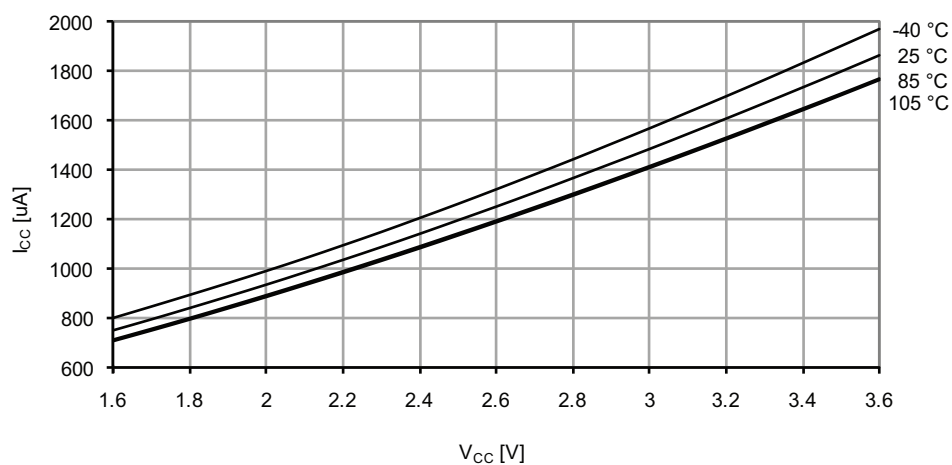


Figure 37-98. Idle mode current vs. V_{CC} .

$f_{SYS} = 32\text{MHz}$ internal oscillator.

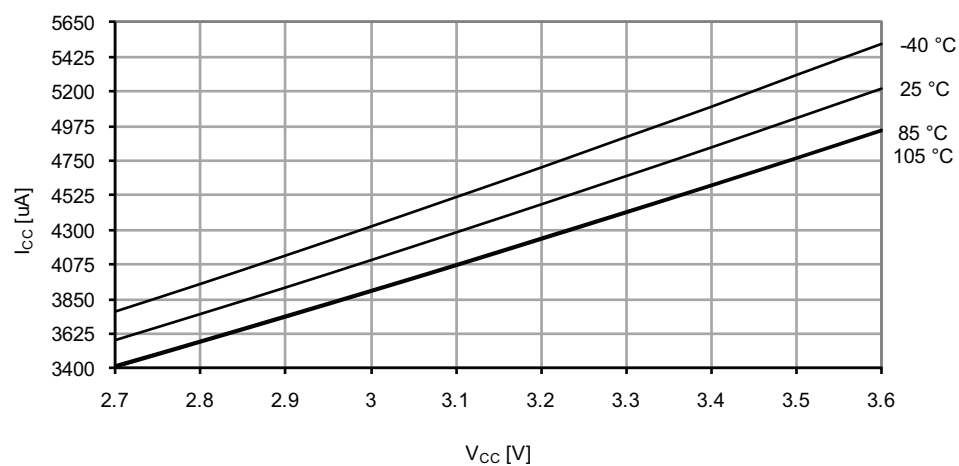
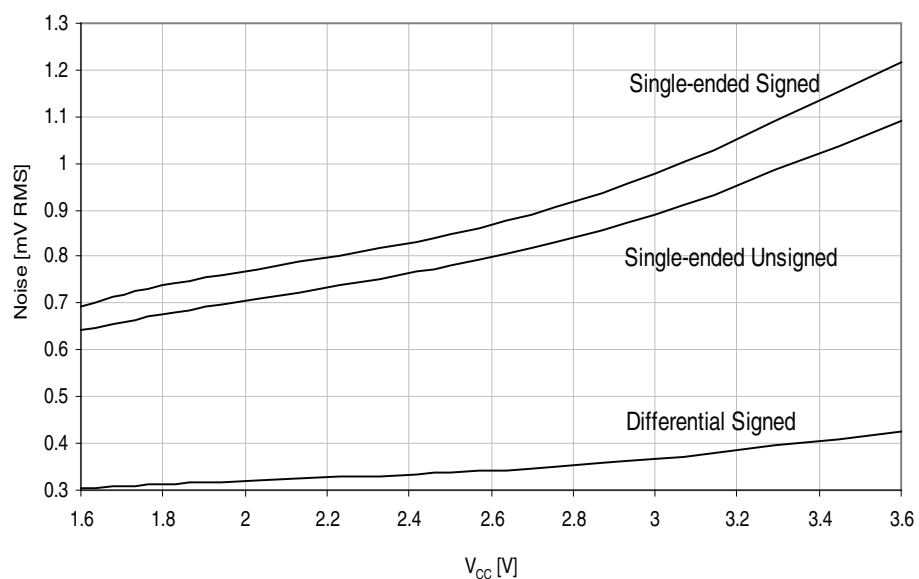


Figure 37-132. Noise vs. V_{CC} .

$T = 25^{\circ}\text{C}$, $V_{REF} = \text{external } 1.0\text{V}$, ADC sampling speed = 500ksps.



37.2.4 DAC Characteristics

Figure 37-133. DAC INL error vs. V_{REF} .

$V_{CC} = 3.6\text{V}$.

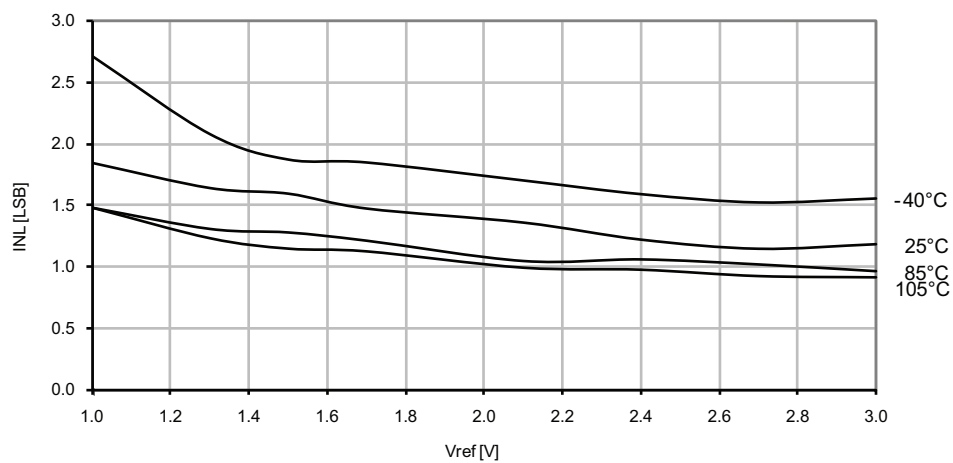


Figure 37-138. Analog comparator hysteresis vs. V_{CC} .
High-speed mode, large hysteresis.

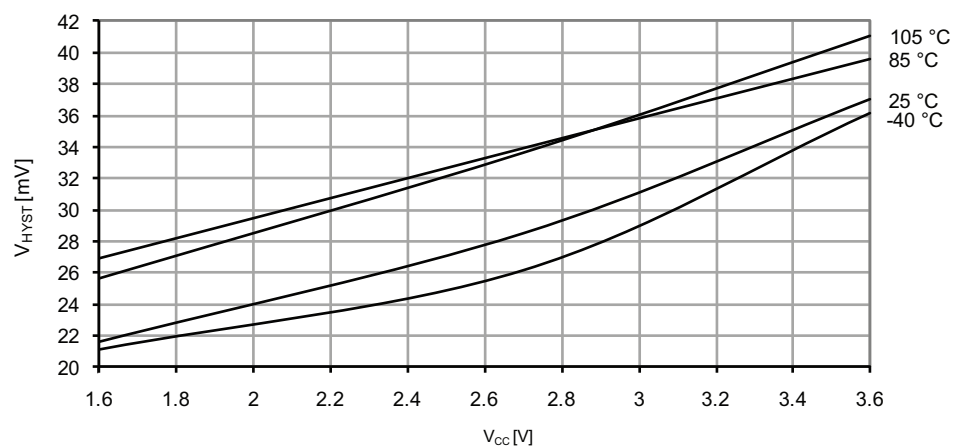
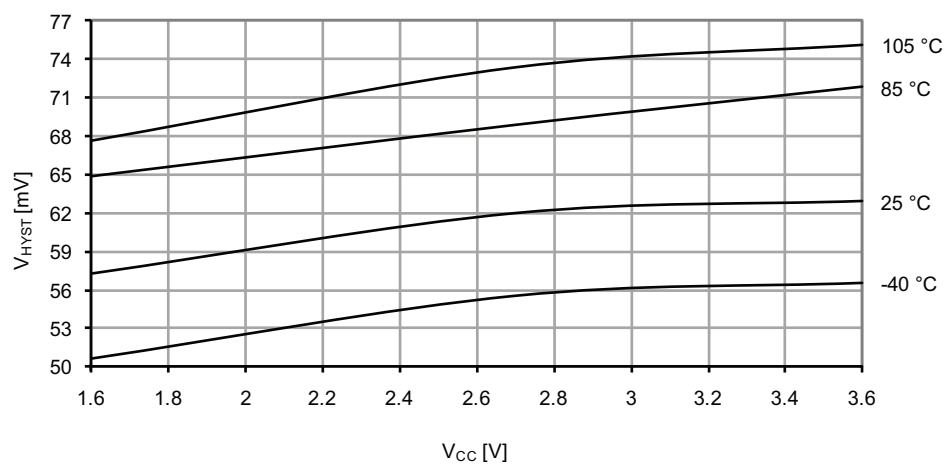


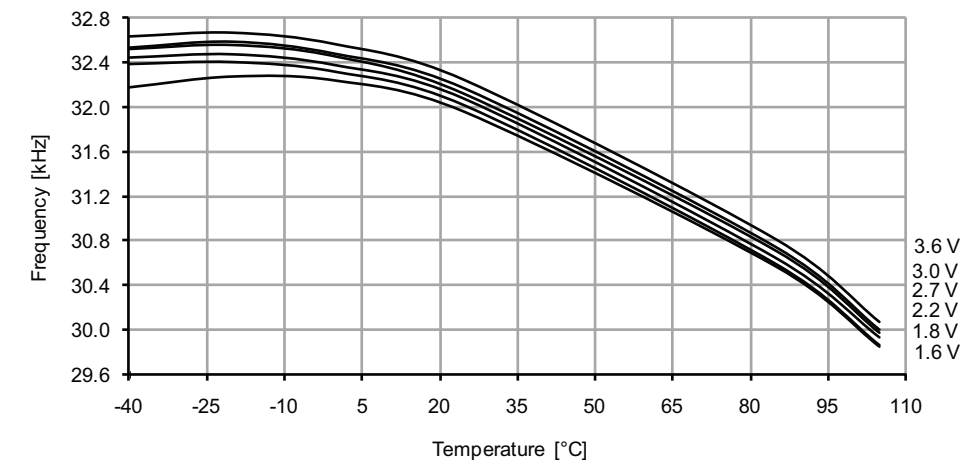
Figure 37-139. Analog comparator hysteresis vs. V_{CC} .
Low power, large hysteresis.



37.2.10 Oscillator Characteristics

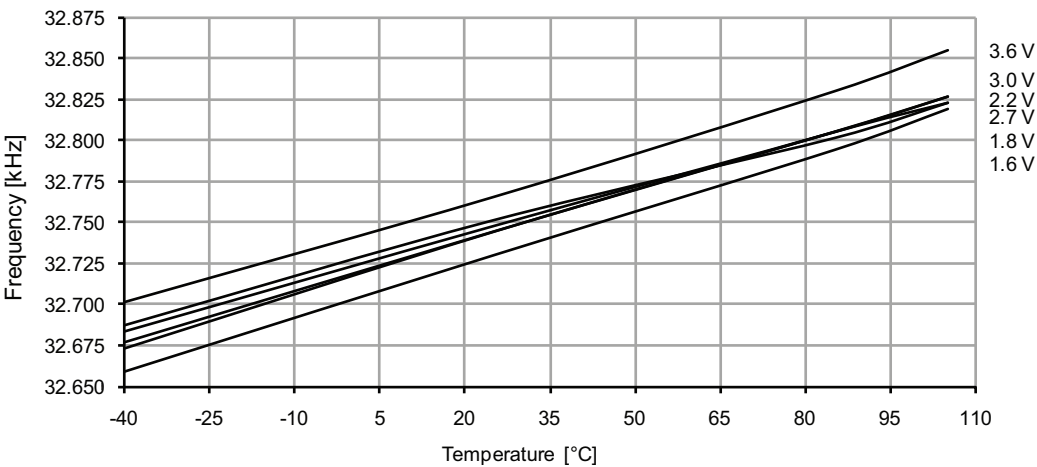
37.2.10.1 Ultra Low-Power internal oscillator

Figure 37-154. Ultra Low-Power internal oscillator frequency vs. temperature.



37.2.10.2 32.768kHz Internal Oscillator

Figure 37-155. 32.768kHz internal oscillator frequency vs. temperature.



37.3.2 I/O Pin Characteristics

37.3.2.1 Pull-up

Figure 37-189. I/O pin pull-up resistor current vs. input voltage.
 $V_{CC} = 1.8V$.

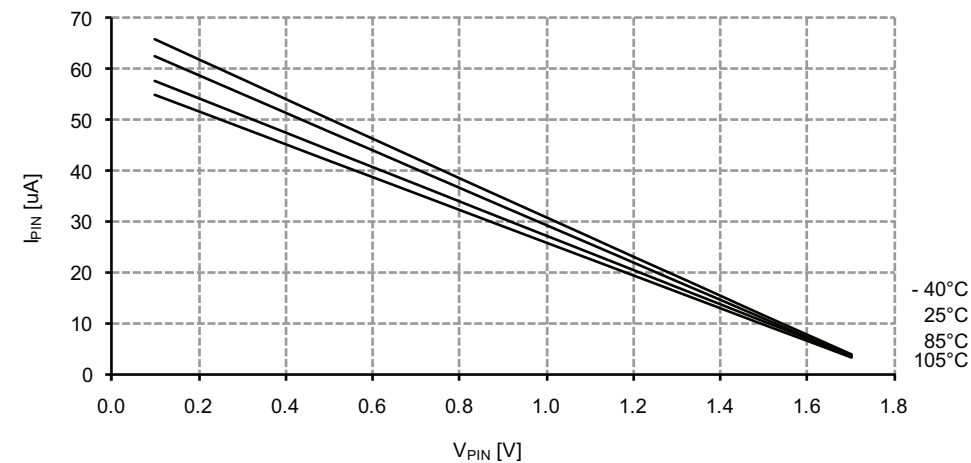
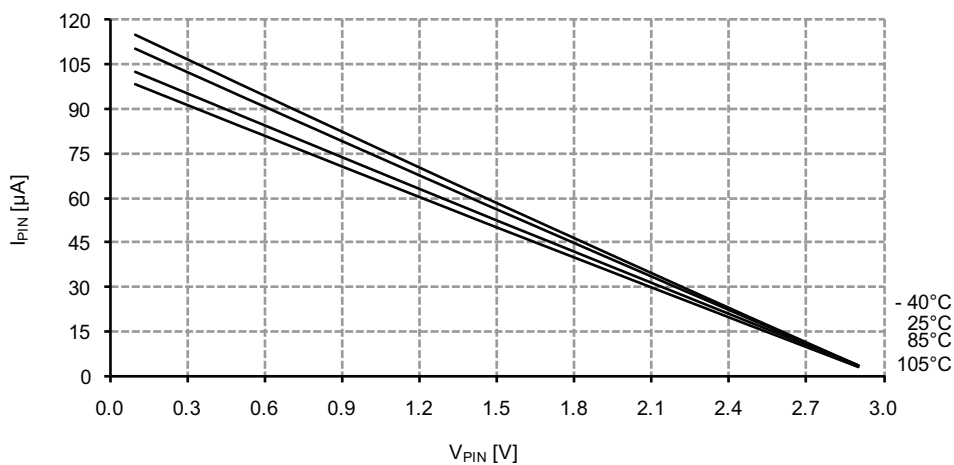
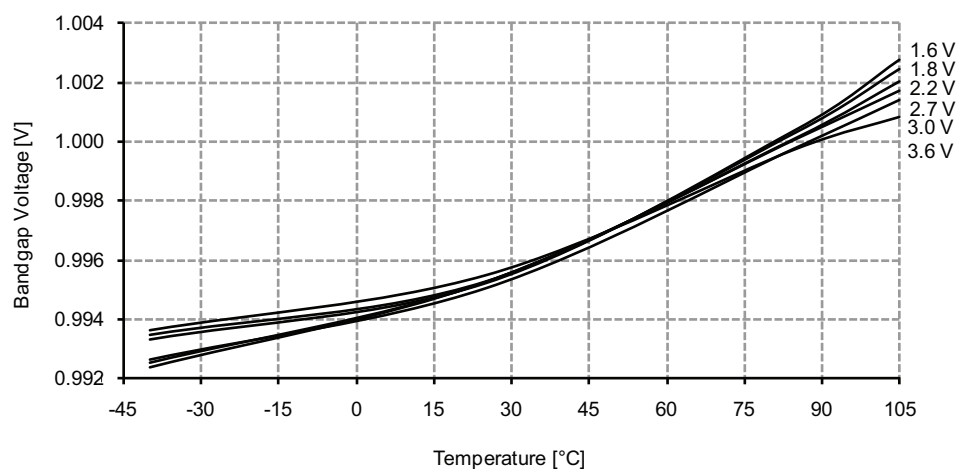


Figure 37-190. I/O pin pull-up resistor current vs. input voltage.
 $V_{CC} = 3.0V$.



37.3.6 Internal 1.0V reference Characteristics

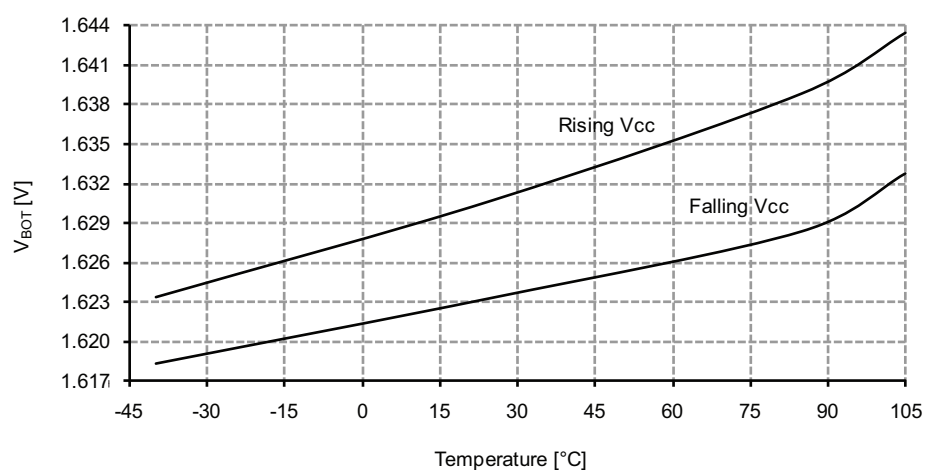
Figure 37-227. ADC/DAC Internal 1.0V reference vs. temperature.



37.3.7 BOD Characteristics

Figure 37-228. BOD thresholds vs. temperature.

BOD level = 1.6V.



37.3.10.2 32.768kHz Internal Oscillator

Figure 37-239. 32.768kHz internal oscillator frequency vs. temperature.

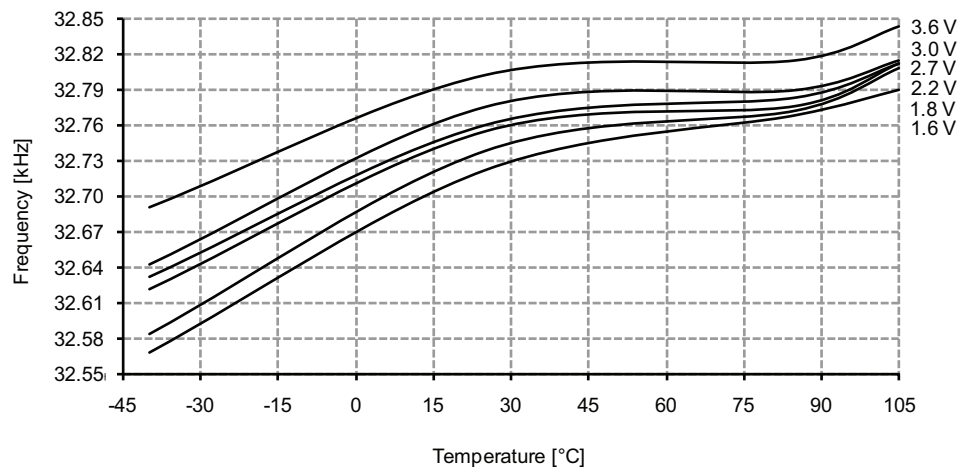


Figure 37-240. 32.768kHz internal oscillator frequency vs. calibration value.
 $V_{CC} = 3.0V$, $T = 25^{\circ}C$.

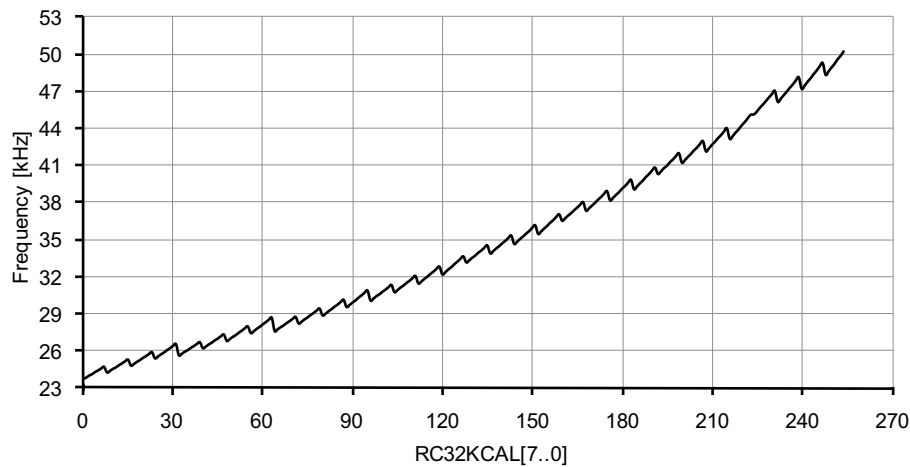


Figure 37-295. Gain error vs. V_{CC}

$T = 25^{\circ}\text{C}$, $V_{REF} = \text{external } 1.0\text{V}$, ADC sampling speed = 500kps

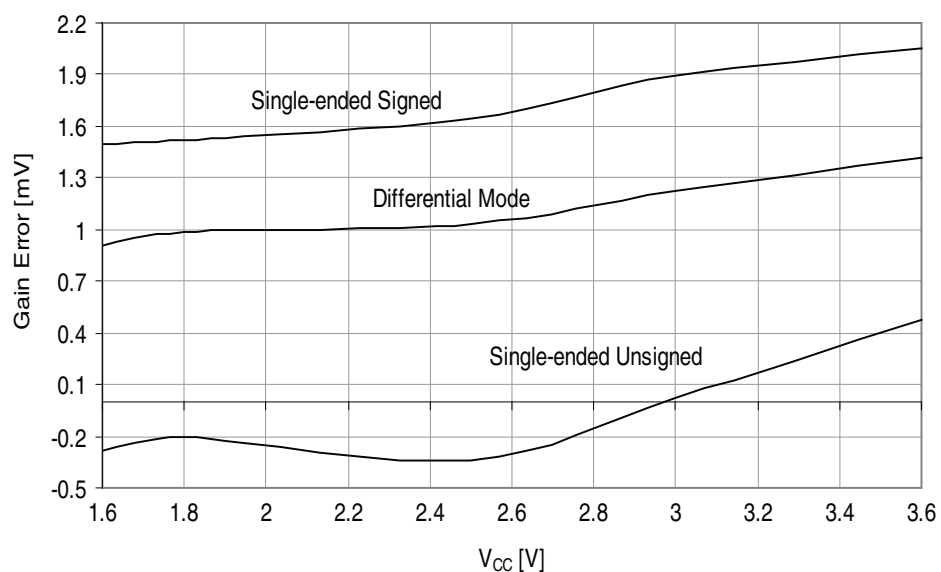


Figure 37-296. Offset error vs. V_{REF}

$T = 25^{\circ}\text{C}$, $V_{CC} = 3.6\text{V}$, ADC sampling speed = 500kps

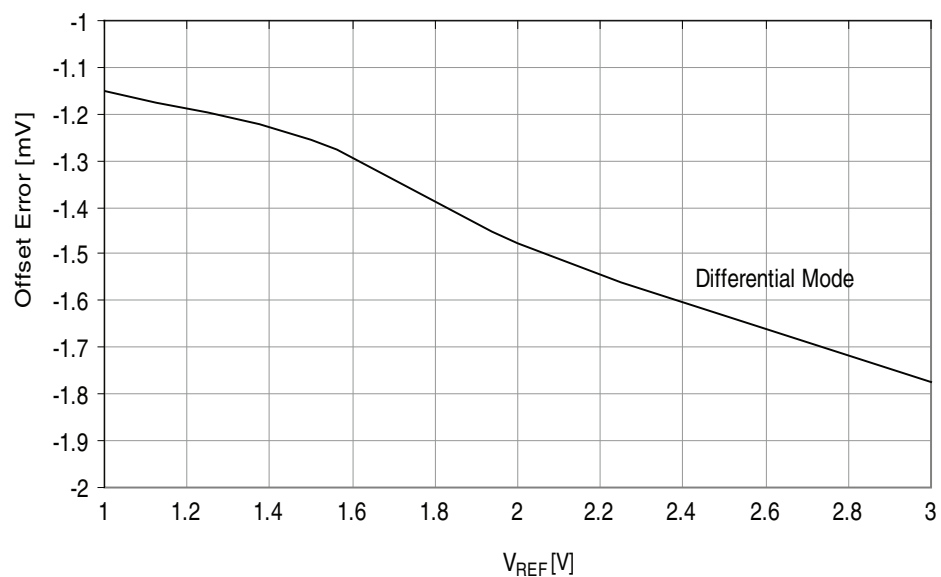


Figure 37-317. Reset pin pull-up resistor current vs. reset pin voltage

$V_{CC} = 3.3V$

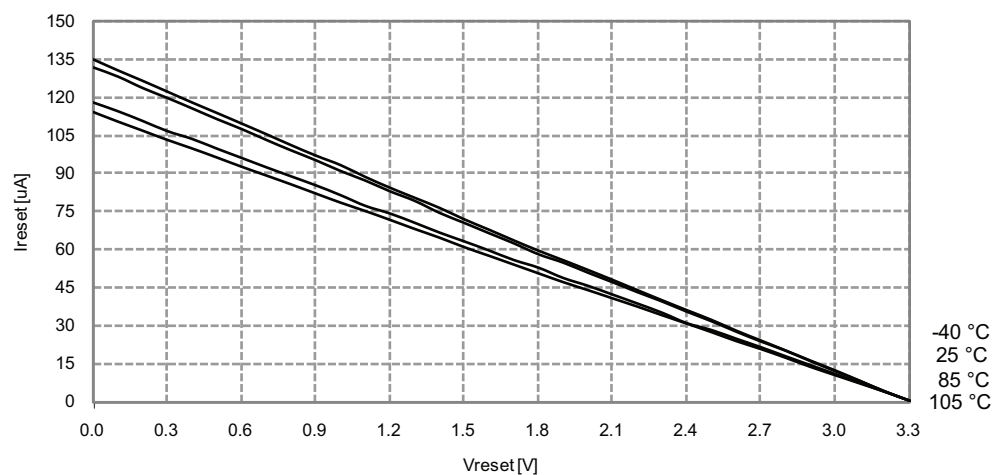


Figure 37-318. Reset pin input threshold voltage vs. V_{CC}

V_{IH} - Reset pin read as "1"

