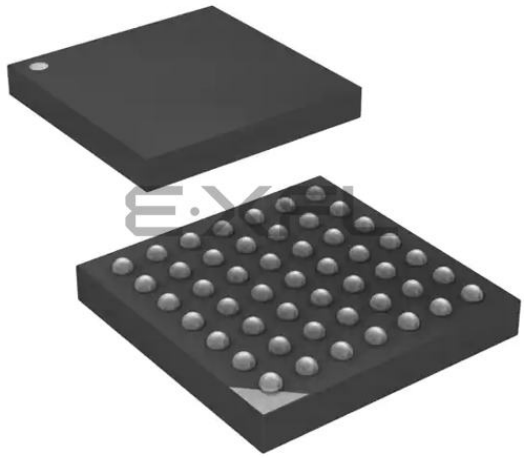

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	49-VFBGA
Supplier Device Package	49-VFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64a4u-cuk

6. AVR CPU

6.1 Features

- 8/16-bit, high-performance Atmel AVR RISC CPU
  - 142 instructions
  - Hardware multiplier
- 32x8-bit registers directly connected to the ALU
- Stack in RAM
- Stack pointer accessible in I/O memory space
- Direct addressing of up to 16MB of program memory and 16MB of data memory
- True 16/24-bit access to 16/24-bit I/O registers
- Efficient support for 8-, 16-, and 32-bit arithmetic
- Configuration change protection of system-critical features

6.2 Overview

All Atmel AVR XMEGA devices use the 8/16-bit AVR CPU. The main function of the CPU is to execute the code and perform all calculations. The CPU is able to access memories, perform calculations, control peripherals, and execute the program in the flash memory. Interrupt handling is described in a separate section, refer to “Interrupts and Programmable Multilevel Interrupt Controller” on page 29.

6.3 Architectural Overview

In order to maximize performance and parallelism, the AVR CPU uses a Harvard architecture with separate memories and buses for program and data. Instructions in the program memory are executed with single-level pipelining. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This enables instructions to be executed on every clock cycle. For details of all AVR instructions, refer to http://www.atmel.com/avr.

Table 14-1. Reset and interrupt vectors

Program address (base address)	Source	Interrupt description
0x000	RESET	
0x002	OSCF_INT_vect	Crystal oscillator failure interrupt vector (NMI)
0x004	PORTC_INT_base	Port C interrupt base
0x008	PORTR_INT_base	Port R interrupt base
0x00C	DMA_INT_base	DMA controller interrupt base
0x014	RTC_INT_base	Real time counter interrupt base
0x018	TWIC_INT_base	Two-Wire Interface on Port C interrupt base
0x01C	TCC0_INT_base	Timer/counter 0 on port C interrupt base
0x028	TCC1_INT_base	Timer/counter 1 on port C interrupt base
0x030	SPIC_INT_vect	SPI on port C interrupt vector
0x032	USARTC0_INT_base	USART 0 on port C interrupt base
0x038	USARTC1_INT_base	USART 1 on port C interrupt base
0x03E	AES_INT_vect	AES interrupt vector
0x040	NVM_INT_base	Nonvolatile Memory interrupt base
0x044	PORTB_INT_base	Port B interrupt base
0x056	PORTE_INT_base	Port E interrupt base
0x05A	TWIE_INT_base	Two-wire Interface on Port E interrupt base
0x05E	TCE0_INT_base	Timer/counter 0 on port E interrupt base
0x06A	TCE1_INT_base	Timer/counter 1 on port E interrupt base
0x074	USARTE0_INT_base	USART 0 on port E interrupt base
0x080	PORTD_INT_base	Port D interrupt base
0x084	PORTA_INT_base	Port A interrupt base
0x088	ACA_INT_base	Analog Comparator on Port A interrupt base
0x08E	ADCA_INT_base	Analog to Digital Converter on Port A interrupt base
0x09A	TCD0_INT_base	Timer/counter 0 on port D interrupt base
0x0A6	TCD1_INT_base	Timer/counter 1 on port D interrupt base
0x0AE	SPID_INT_vector	SPI on port D interrupt vector
0x0B0	USARTD0_INT_base	USART 0 on port D interrupt base
0x0B6	USARTD1_INT_base	USART 1 on port D interrupt base
0x0FA	USB_INT_base	USB on port D interrupt base

Multipacket transfer enables a data payload exceeding the maximum packet size of an endpoint to be transferred as multiple packets without software intervention. This reduces the CPU intervention and the interrupts needed for USB transfers.

For low-power operation, the USB module can put the microcontroller into any sleep mode when the USB bus is idle and a suspend condition is given. Upon bus resumes, the USB module can wake up the microcontroller from any sleep mode.

PORTD has one USB. Notation of this is USB.

28. ADC – 12-bit Analog to Digital Converter

28.1 Features

- One Analog to Digital Converter (ADC)
- 12-bit resolution
- Up to two million samples per second
  - Two inputs can be sampled simultaneously using ADC and 1x gain stage
  - Four inputs can be sampled within 1.5µs
  - Down to 2.5µs conversion time with 8-bit resolution
  - Down to 3.5µs conversion time with 12-bit resolution
- Differential and single-ended input
  - Up to 12 single-ended inputs
  - 12x4 differential inputs without gain
  - 8x4 differential inputs with gain
- Built-in differential gain stage
  - 1/2x, 1x, 2x, 4x, 8x, 16x, 32x, and 64x gain options
- Single, continuous and scan conversion options
- Four internal inputs
  - Internal temperature sensor
  - DAC output
  - AV_{CC} voltage divided by 10
  - 1.1V bandgap voltage
- Four conversion channels with individual input control and result registers
  - Enable four parallel configurations and results
- Internal and external reference options
- Compare function for accurate monitoring of user defined thresholds
- Optional event triggered conversion for accurate timing
- Optional DMA transfer of conversion results
- Optional interrupt/event on compare result

28.2 Overview

The ADC converts analog signals to digital values. The ADC has 12-bit resolution and is capable of converting up to two million samples per second (msps). The input selection is flexible, and both single-ended and differential measurements can be done. For differential measurements, an optional gain stage is available to increase the dynamic range. In addition, several internal signal inputs are available. The ADC can provide both signed and unsigned results.

This is a pipelined ADC that consists of several consecutive stages. The pipelined design allows a high sample rate at a low system clock frequency. It also means that a new input can be sampled and a new ADC conversion started while other ADC conversions are still ongoing. This removes dependencies between sample rate and propagation delay.

The ADC has four conversion channels (0-3) with individual input selection, result registers, and conversion start control. The ADC can then keep and use four parallel configurations and results, and this will ease use for applications with high data throughput or for multiple modules using the ADC independently. It is possible to use DMA to move ADC results directly to memory or peripherals when conversions are done.

Both internal and external reference voltages can be used. An integrated temperature sensor is available for use with the ADC. The output from the DAC, $AV_{CC}/10$ and the bandgap voltage can also be measured by the ADC.

The ADC has a compare function for accurate monitoring of user defined thresholds with minimum software intervention required.

30. AC – Analog Comparator

30.1 Features

- Two Analog Comparators (ACs)
- Selectable propagation delay versus current consumption
- Selectable hysteresis
  - No
  - Small
  - Large
- Analog comparator output available on pin
- Flexible input selection
  - All pins on the port
  - Output from the DAC
  - Bandgap reference voltage
  - A 64-level programmable voltage scaler of the internal AV_{CC} voltage
- Interrupt and event generation on:
  - Rising edge
  - Falling edge
  - Toggle
- Window function interrupt and event generation on:
  - Signal above window
  - Signal inside window
  - Signal below window
- Constant current source with configurable output pin selection

30.2 Overview

The analog comparator (AC) compares the voltage levels on two inputs and gives a digital output based on this comparison. The analog comparator may be configured to generate interrupt requests and/or events upon several different combinations of input change.

Two important properties of the analog comparator's dynamic behavior are: hysteresis and propagation delay. Both of these parameters may be adjusted in order to achieve the optimal operation for each application.

The input selection includes analog port pins, several internal signals, and a 64-level programmable voltage scaler. The analog comparator output state can also be output on a pin for use by external devices.

A constant current source can be enabled and output on a selectable pin. This can be used to replace, for example, external resistors used to charge capacitors in capacitive touch sensing applications.

The analog comparators are always grouped in pairs on each port. These are called analog comparator 0 (AC0) and analog comparator 1 (AC1). They have identical behavior, but separate control registers. Used as pair, they can be set in window mode to compare a signal to a voltage range instead of a voltage level.

PORTA has one AC pair. Notation is ACA.

Mnemonics	Operands	Description	Operation	Flags	#Clocks
MOVW	Rd, Rr	Copy Register Pair	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LDS	Rd, k	Load Direct from data space	Rd ← (k)	None	2 (1)(2)
LD	Rd, X	Load Indirect	Rd ← (X)	None	1 (1)(2)
LD	Rd, X+	Load Indirect and Post-Increment	Rd ← (X) X ← X + 1	None	1 (1)(2)
LD	Rd, -X	Load Indirect and Pre-Decrement	X ← X - 1, ← X - 1 Rd ← (X) ← (X)	None	2 (1)(2)
LD	Rd, Y	Load Indirect	Rd ← (Y) ← (Y)	None	1 (1)(2)
LD	Rd, Y+	Load Indirect and Post-Increment	Rd ← (Y) Y ← Y + 1	None	1 (1)(2)
LD	Rd, -Y	Load Indirect and Pre-Decrement	Y ← Y - 1 Rd ← (Y)	None	2 (1)(2)
LDD	Rd, Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2 (1)(2)
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	1 (1)(2)
LD	Rd, Z+	Load Indirect and Post-Increment	Rd ← (Z), Z ← Z+1	None	1 (1)(2)
LD	Rd, -Z	Load Indirect and Pre-Decrement	Z ← Z - 1, Rd ← (Z)	None	2 (1)(2)
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2 (1)(2)
STS	k, Rr	Store Direct to Data Space	(k) ← Rd	None	2 (1)
ST	X, Rr	Store Indirect	(X) ← Rr	None	1 (1)
ST	X+, Rr	Store Indirect and Post-Increment	(X) ← Rr, X ← X + 1	None	1 (1)
ST	-X, Rr	Store Indirect and Pre-Decrement	X ← X - 1, (X) ← Rr	None	2 (1)
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	1 (1)
ST	Y+, Rr	Store Indirect and Post-Increment	(Y) ← Rr, Y ← Y + 1	None	1 (1)
ST	-Y, Rr	Store Indirect and Pre-Decrement	Y ← Y - 1, (Y) ← Rr	None	2 (1)
STD	Y+q, Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2 (1)
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	1 (1)
ST	Z+, Rr	Store Indirect and Post-Increment	(Z) ← Rr Z ← Z + 1	None	1 (1)
ST	-Z, Rr	Store Indirect and Pre-Decrement	Z ← Z - 1	None	2 (1)
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2 (1)
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Increment	Rd ← (Z), Z ← Z + 1	None	3
ELPM		Extended Load Program Memory	R0 ← (RAMPZ:Z)	None	3
ELPM	Rd, Z	Extended Load Program Memory	Rd ← (RAMPZ:Z)	None	3

Table 36-10. Accuracy characteristics.

Symbol	Parameter	Condition [2]		Min.	Typ.	Max.	Units
RES	Resolution	Programmable to 8 or 12 bit		8	12	12	Bits
INL [1]	Integral non-linearity	500ksps	V_{CC}-1.0V < V_{REF}< V_{CC}-0.6V		±1.2	±2.0	lsb
			All V_{REF}		±1.5	±3.0	
		2000ksps	V_{CC}-1.0V < V_{REF}< V_{CC}-0.6V		±1.0	±2.0	
			All V_{REF}		±1.5	±3.0	
DNL [1]	Differential non-linearity	guaranteed monotonic			<±0.8	<±1.0	lsb
	Offset error				-1.0		mV
		Temperature drift			<0.01		mV/K
		Operating voltage drift			<0.6		mV/V
	Gain error	Differential mode	External reference		-1.0		mV
			AV_{CC}/1.6		10		
			AV_{CC}/2.0		8.0		
			Bandgap		±5.0		
		Temperature drift			<0.02		mV/K
		Operating voltage drift			<0.5		mV/V
	Noise	Differential mode, shorted input 2msps, V_{CC} = 3.6V, Clk_{PER} = 16MHz			0.4		mV rms

Notes:
1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.
2. Unless otherwise noted all linearity, offset and gain error numbers are valid under the condition that external V_{REF} is used.

Table 36-11. Gain stage characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_{in}	Input resistance	Switched in normal mode			4.0		kΩ
C_{sample}	Input capacitance	Switched in normal mode			4.4		pF
	Signal range	Gain stage output		0		V_{CC}- 0.6	V
	Propagation delay	ADC conversion rate			1.0		Clk_{ADC} cycles
	Sample rate	Same as ADC		100		1000	kHz
INL [1]	Integral non-linearity	500ksps	All gain settings		±1.5	±4	lsb
	Gain error	1x gain, normal mode			-0.8		%
		8x gain, normal mode			-2.5		
		64x gain, normal mode			-3.5		

36.2.6 ADC characteristics

Table 36-40. Power supply, reference and input range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	V
V_{REF}	Reference voltage		1		AV_{CC}- 0.6	V
R_{in}	Input resistance	Switched		4.0		kΩ
C_{sample}	Input capacitance	Switched		4.4		pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7		pF
V_{IN}	Input range		-0.1		AV_{CC}+0.1	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	V
	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF}-ΔV	V
ΔV	Fixed offset voltage			190		LSB

Table 36-41. Clock and timing.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC clock frequency	Maximum is 1/4 of peripheral clock frequency	100		2000	kHz
		Measuring internal signals	100		125	
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off	100		2000	ksps
		CURRLIMIT = LOW	100		1500	
		CURRLIMIT = MEDIUM	100		1000	
		CURRLIMIT = HIGH	100		500	
	Sampling time	1/2 Clk_{ADC} cycle	0.25		5	µs
	Conversion time (latency)	(RES+2)/2+(GAIN !=0) RES (Resolution) = 8 or 12	5		8	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	Clk_{ADC} cycles
	ADC settling time	After changing reference or input mode		7	7	Clk_{ADC} cycles
		After ADC flush		1	1	

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Offset error, input referred	1x gain, normal mode			-2.0		mV
		8x gain, normal mode			-5.0		
		64x gain, normal mode			-4.0		
	Noise	1x gain, normal mode	V_{CC} = 3.6V Ext. V_{REF}		0.5		mV rms
		8x gain, normal mode			1.5		
		64x gain, normal mode			11		

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.

36.2.7 DAC Characteristics

Table 36-44. Power supply, reference and output range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	V
AV_{REF}	External reference voltage		1.0		V_{CC}- 0.6	V
$R_{channel}$	DC output impedance				50	Ω
	Linear output voltage range		0.15		AV_{CC}-0.15	V
R_{AREF}	Reference input resistance			>10		MΩ
CAREF	Reference input capacitance	Static load		7.0		pF
	Minimum Resistance load		1.0			kΩ
	Maximum capacitance load				100	pF
		1000Ω serial resistance			1.0	nF
	Output sink/source	Operating within accuracy specification			AV_{CC}/1000	mA
		Safe operation			10	

Table 36-45. Clock and timing.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
f_{DAC}	Conversion rate	C_{load}=100pF, maximum step size	Normal mode	0		1000	ksps
			Low power mode			500	

36.2.8 Analog Comparator Characteristics

Table 36-47. Analog Comparator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage			<±10		mV
I_{lk}	Input leakage current			<1		nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			100		µs
V_{hys1}	Hysteresis, none			0		mV
V_{hys2}	Hysteresis, small	mode = High Speed (HS)		13		mV
		mode = Low Power (LP)		30		
V_{hys3}	Hysteresis, large	mode = HS		30		mV
		mode = LP		60		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T= 85°C mode = HS		30	90	ns
		mode = HS		30		
		V_{CC} = 3.0V, T= 85°C mode = LP		130	500	
		mode = LP		130		
	64-level voltage scaler	Integral non-linearity (INL)		0.3	0.5	lsb

36.2.9 Bandgap and Internal 1.0V Reference Characteristics

Table 36-48. Bandgap and Internal 1.0V reference characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC or DAC	1 Clk_{PER} + 2.5µs			µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T= 85°C, after calibration	0.99	1.0	1.01	V
	Variation over voltage and temperature	Relative to T= 85°C, V_{CC} = 3.0V		±1.5		%

36.2.13 Flash and EEPROM Memory Characteristics

Table 36-52. Endurance and data retention.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Flash	Write/Erase cycles	25°C	10K			Cycle
			85°C	10K			
			105°C	2K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			
	EEPROM	Write/Erase cycles	25°C	100K			Cycle
			85°C	100K			
			105°C	30K			
		Data retention	25°C	100			Year
			85°C	25			
			105°C	10			

Table 36-53. Programming time.

Symbol	Parameter	Condition	Min.	Typ.(1)	Max.	Units
	Chip Erase	32KB Flash, EEPROM(2) and SRAM erase		50		ms
	Application Erase	Section erase		6		ms
	Flash	Page erase		4		ms
		Page write		4		
		Atomic page erase and write		8		
	EEPROM	Page erase		4		ms
		Page write		4		
		Atomic page erase and write		8		

Notes:
1. Programming is timed from the 2MHz internal oscillator.
2. EEPROM is not erased if the EESAVE fuse is programmed.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
R_Q	Negative impedance [1]	XOSCPWR=0, FRQRANGE=0	0.4MHz resonator, CL=100pF	2.4k			Ω
			1MHz crystal, CL=20pF	8.7k			
			2MHz crystal, CL=20pF	2.1k			
		XOSCPWR=0, FRQRANGE=1, CL=20pF	2MHz crystal	4.2k			
			8MHz crystal	250			
			9MHz crystal	195			
		XOSCPWR=0, FRQRANGE=2, CL=20pF	8MHz crystal	360			
			9MHz crystal	285			
			12MHz crystal	155			
		XOSCPWR=0, FRQRANGE=3, CL=20pF	9MHz crystal	365			
			12MHz crystal	200			
			16MHz crystal	105			
		XOSCPWR=1, FRQRANGE=0, CL=20pF	9MHz crystal	435			
			12MHz crystal	235			
			16MHz crystal	125			
		XOSCPWR=1, FRQRANGE=1, CL=20pF	9MHz crystal	495			
			12MHz crystal	270			
			16MHz crystal	145			
		XOSCPWR=1, FRQRANGE=2, CL=20pF	12MHz crystal	305			
			16MHz crystal	160			
		XOSCPWR=1, FRQRANGE=3, CL=20pF	12MHz crystal	380			
			16MHz crystal	205			
	ESR	SF = Safety factor				$\min(R_Q)/SF$	kΩ
C_{XTAL1}	Parasitic capacitance XTAL1 pin				5.4		pF
C_{XTAL2}	Parasitic capacitance XTAL2 pin				7.1		pF
C_{LOAD}	Parasitic capacitance load				3.07		pF

Note: 1. Numbers for negative impedance are not tested in production but guaranteed from design and characterization.

Table 36-78. Accuracy characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
RES	Input resolution					12	Bits
INL [1]	Integral non-linearity	V_{REF}= Ext 1.0V	V_{CC} = 1.6V		±2.0	±3.0	lsb
			V_{CC} = 3.6V		±1.5	±2.5	
		V_{REF}=AV_{CC}	V_{CC} = 1.6V		±2.0	±4.0	
			V_{CC} = 3.6V		±1.5	±4.0	
		V_{REF}=INT1V	V_{CC} = 1.6V		±5.0		
			V_{CC} = 3.6V		±5.0		
DNL [1]	Differential non-linearity	V_{REF}=Ext 1.0V	V_{CC} = 1.6V		±1.5	3.0	lsb
			V_{CC} = 3.6V		±0.6	1.5	
		V_{REF}=AV_{CC}	V_{CC} = 1.6V		±1.0	3.5	
			V_{CC} = 3.6V		±0.6	1.5	
		V_{REF}=INT1V	V_{CC} = 1.6V		±4.5		
			V_{CC} = 3.6V		±4.5		
	Gain error	After calibration			<4.0		lsb
	Gain calibration step size				4.0		lsb
	Gain calibration drift	V_{REF}= Ext 1.0V			<0.2		mV/K
	Offset error	After calibration			<1.0		lsb
	Offset calibration step size				1.0		

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% output voltage range.

37.1.1.5 Standby mode supply current

Figure 37-19. Standby supply current vs. V_{CC}.

Standby, f_{SYS} = 1MHz.

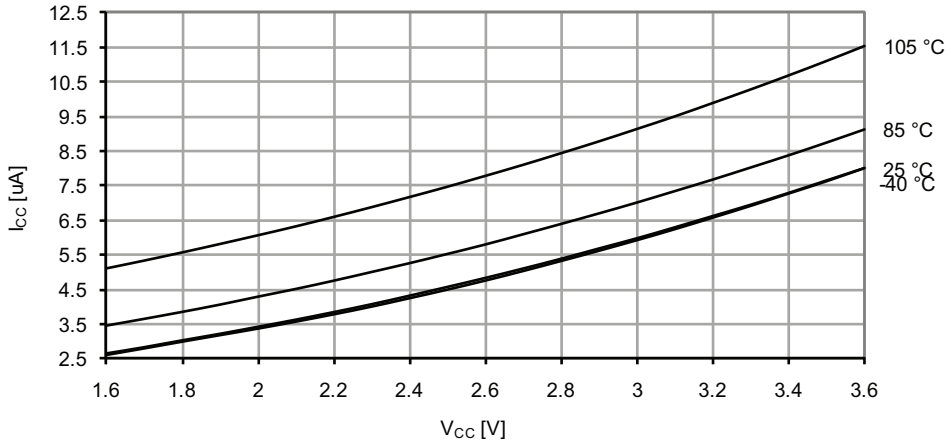
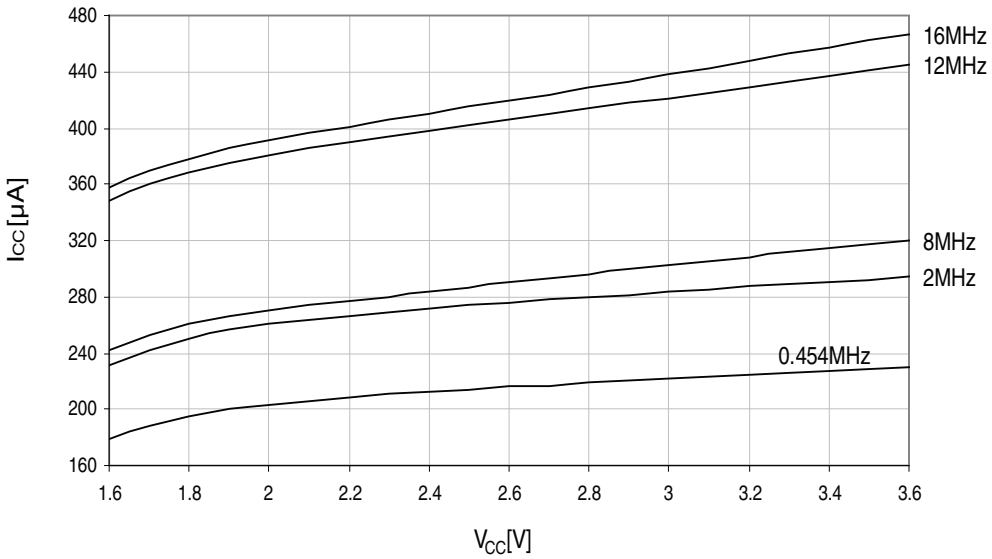


Figure 37-20. Standby supply current vs. V_{CC}.

25°C, running from different crystal oscillators.



37.1.9 Power-on Reset Characteristics

Figure 37-68. Power-on reset current consumption vs. V_{CC}.

BOD level = 3.0V, enabled in continuous mode.

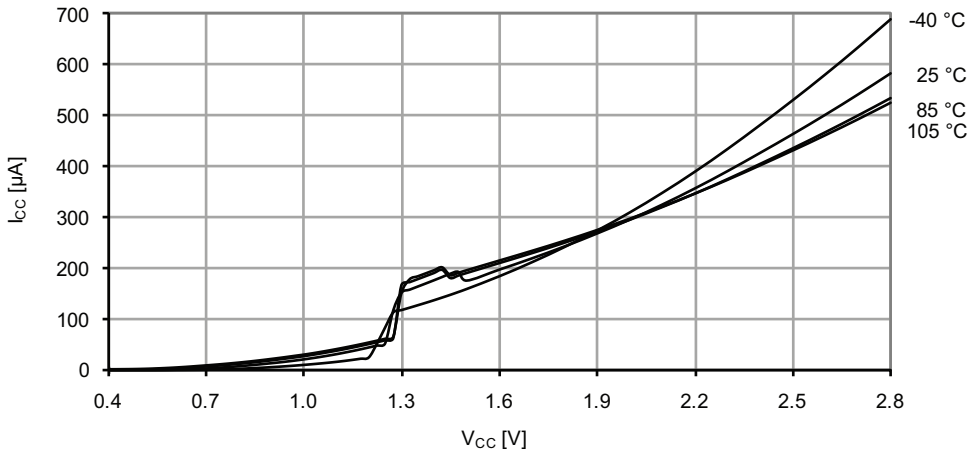
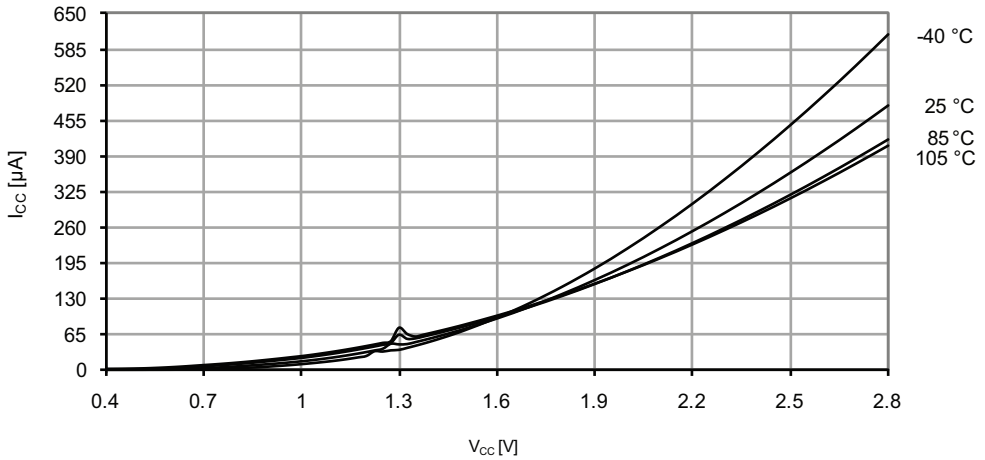


Figure 37-69. Power-on reset current consumption vs. V_{CC}.

BOD level = 3.0V, enabled in sampled mode.



37.1.12 PDI characteristics

Figure 37-84. Maximum PDI frequency vs. V_{CC}.

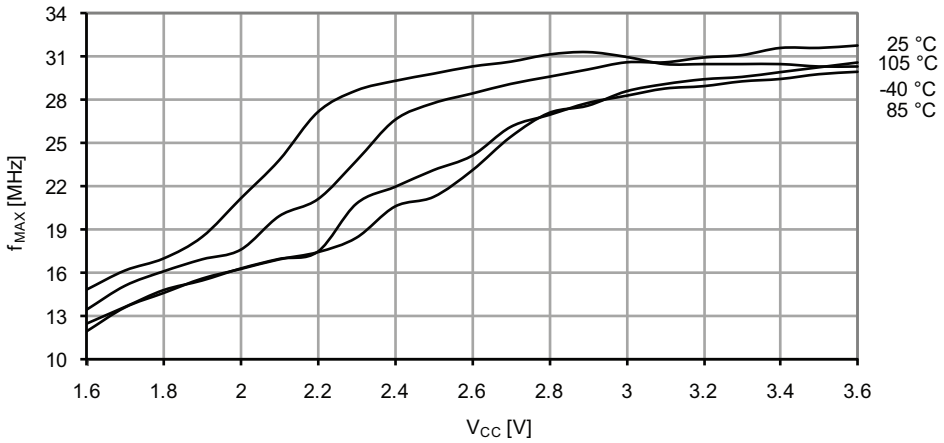


Figure 37-89.Active mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.

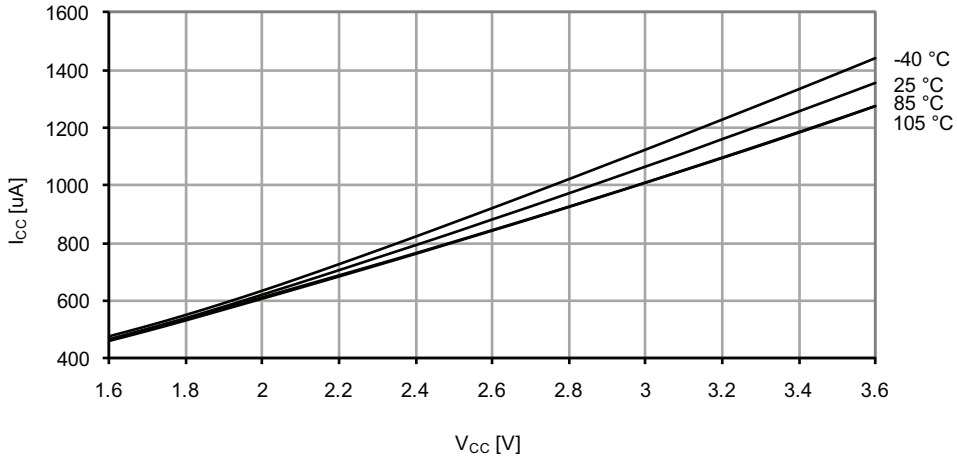


Figure 37-90.Active mode supply current vs. V_{CC}.

f_{SYS} = 32MHz internal oscillator prescaled to 8MHz.

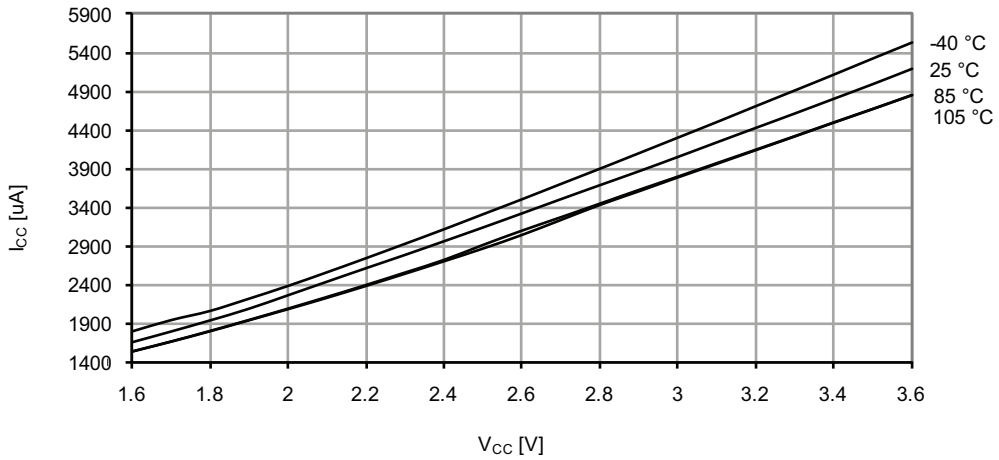
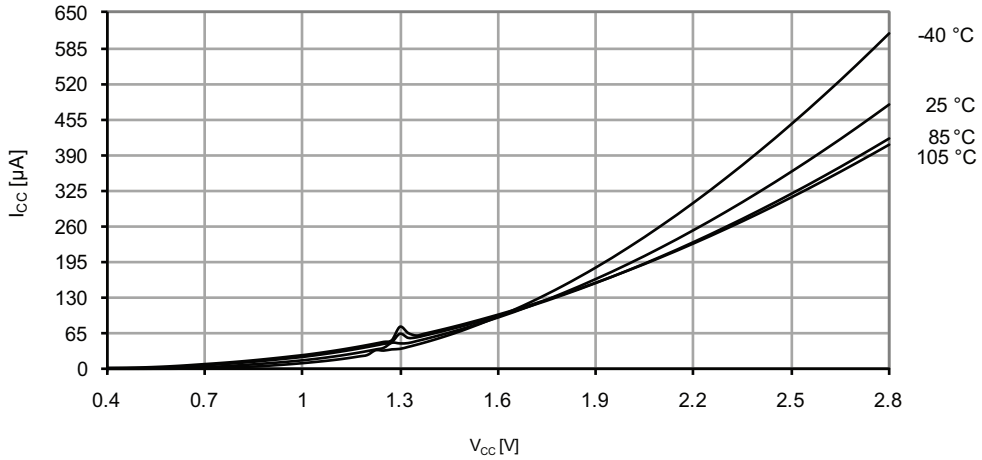


Figure 37-321. Power-on reset current consumption vs. V_{CC}

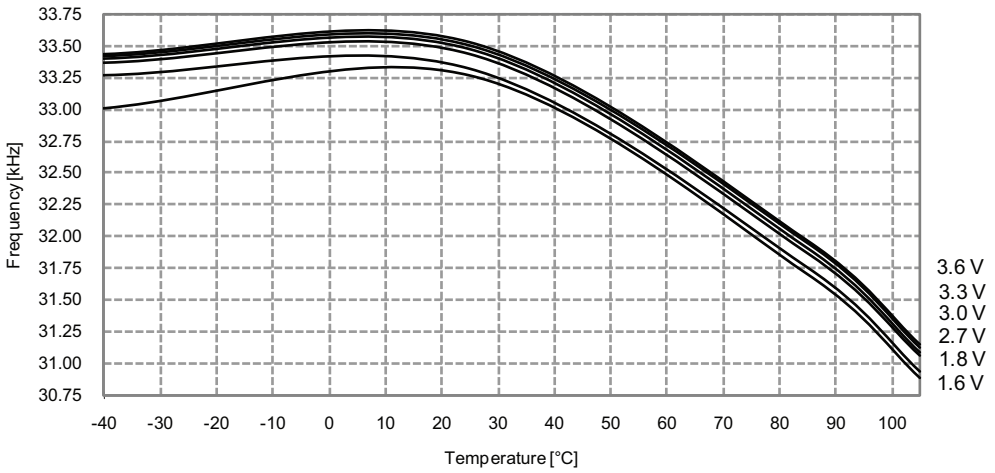
BOD level = 3.0V, enabled in sampled mode



37.4.10 Oscillator Characteristics

37.4.10.1 Ultra Low-Power internal oscillator

Figure 37-322. Ultra Low-Power internal oscillator frequency vs. temperature.



38.3 ATxmega64A4U

38.3.1 Rev. D

- ADC may have missing codes in SE unsigned mode at low temp and low Vcc
- CRC fails for Range CRC when end address is the last word address of a flash section

1. **ADC may have missing codes in SE unsigned mode at low temp and low Vcc**
   The ADC may have missing codes i single ended (SE) unsigned mode below 0C when Vcc is below 1.8V.

   Problem fix/Workaround
   Use the ADC in SE signed mode.

2. **CRC fails for Range CRC when end address is the last word address of a flash section**
   If boot read lock is enabled, the range CRC cannot end on the last address of the application section. If application table read lock is enabled, the range CRC cannot end on the last address before the application table.

   Problem fix/Workaround
   Ensure that the end address used in Range CRC does not end at the last address before a section with read lock enabled. Instead, use the dedicated CRC commands for complete applications sections.

38.3.2 Rev. C

- ADC may have missing codes in SE unsigned mode at low temp and low Vcc
- CRC fails for Range CRC when end address is the last word address of a flash section
- AWeX fault protection restore is not done correct in Pattern Generation Mode

1. **ADC may have missing codes in SE unsigned mode at low temp and low Vcc**
   The ADC may have missing codes i single ended (SE) unsigned mode below 0C when Vcc is below 1.8V.

   Problem fix/Workaround
   Use the ADC in SE signed mode.

2. **CRC fails for Range CRC when end address is the last word address of a flash section**
   If boot read lock is enabled, the range CRC cannot end on the last address of the application section. If application table read lock is enabled, the range CRC cannot end on the last address before the application table.

   Problem fix/Workaround
   Ensure that the end address used in Range CRC does not end at the last address before a section with read lock enabled. Instead, use the dedicated CRC commands for complete applications sections.