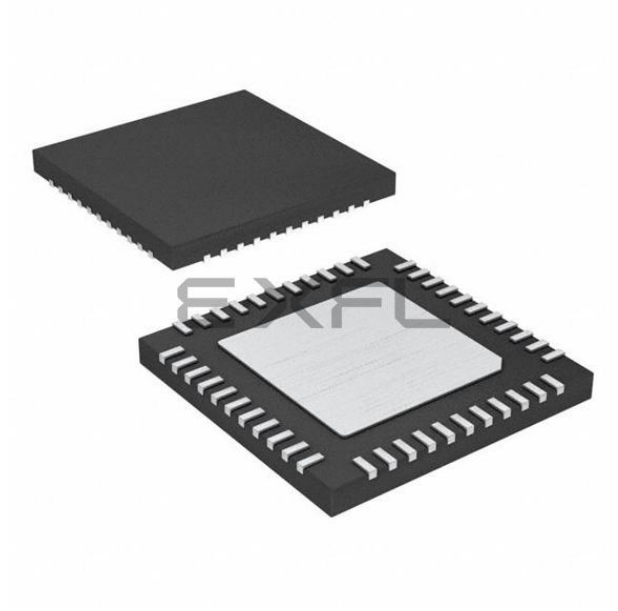

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64a4u-mh

1. Ordering Information

Ordering code	Flash (bytes)	EEPROM (bytes)	SRAM (bytes)	Speed (MHz)	Power supply	Package [1][2][3]	Temp.
ATxmega128A4U-AU	128K + 8K	2K	8K	32	1.6 - 3.6V	44A	-40°C - 85°C
ATxmega128A4U-AUR[4]	128K + 8K	2K	8K				
ATxmega64A4U-AU	64K + 4K	2K	4K				
ATxmega64A4U-AUR[4]	64K + 4K	2K	4K				
ATxmega32A4U-AU	32K + 4K	1K	4K				
ATxmega32A4U-AUR[4]	32K + 4K	1K	4K				
ATxmega16A4U-AU	16K + 4K	1K	2K				
ATxmega16A4U-AUR[4]	16K + 4K	1K	2K				
ATxmega128A4U-MH	128K + 8K	2K	8K			PW	
ATxmega128A4U-MHR[4]	128K + 8K	2K	8K				
ATxmega64A4U-MH	64K + 4K	2K	4K				
ATxmega64A4U-MHR[4]	64K + 4K	2K	4K				
ATxmega32A4U-MH	32K + 4K	1K	4K			44M1	
ATxmega32A4U-MHR[4]	32K + 4K	1K	4K				
ATxmega16A4U-MH	16K + 4K	1K	2K				
ATxmega16A4U-MHR[4]	16K + 4K	1K	2K				
ATxmega128A4U-CU	128K + 8K	2K	8K			49C2	
ATxmega128A4U-CUR[4]	128K + 8K	2K	8K				
ATxmega64A4U-CU	64K + 4K	2K	4K				
ATxmega64A4U-CUR[4]	64K + 4K	2K	4K				
ATxmega32A4U-CU	32K + 4K	1K	4K				
ATxmega32A4U-CUR[4]	32K + 4K	1K	4K				
ATxmega16A4U-CU	16K + 4K	1K	2K				
ATxmega16A4U-CUR[4]	16K + 4K	1K	2K				

6. AVR CPU

6.1 Features

- 8/16-bit, high-performance Atmel AVR RISC CPU
  - 142 instructions
  - Hardware multiplier
- 32x8-bit registers directly connected to the ALU
- Stack in RAM
- Stack pointer accessible in I/O memory space
- Direct addressing of up to 16MB of program memory and 16MB of data memory
- True 16/24-bit access to 16/24-bit I/O registers
- Efficient support for 8-, 16-, and 32-bit arithmetic
- Configuration change protection of system-critical features

6.2 Overview

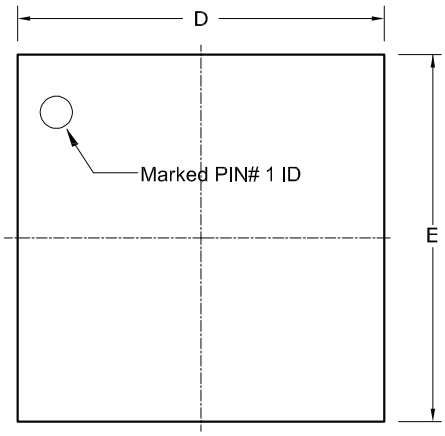
All Atmel AVR XMEGA devices use the 8/16-bit AVR CPU. The main function of the CPU is to execute the code and perform all calculations. The CPU is able to access memories, perform calculations, control peripherals, and execute the program in the flash memory. Interrupt handling is described in a separate section, refer to “Interrupts and Programmable Multilevel Interrupt Controller” on page 29.

6.3 Architectural Overview

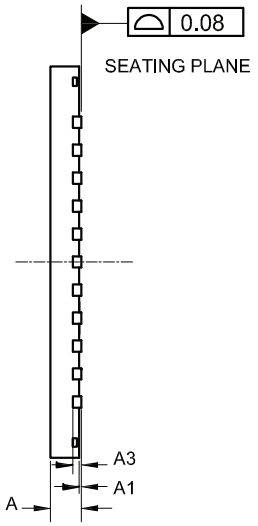
In order to maximize performance and parallelism, the AVR CPU uses a Harvard architecture with separate memories and buses for program and data. Instructions in the program memory are executed with single-level pipelining. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This enables instructions to be executed on every clock cycle. For details of all AVR instructions, refer to http://www.atmel.com/avr.

35.2 PW

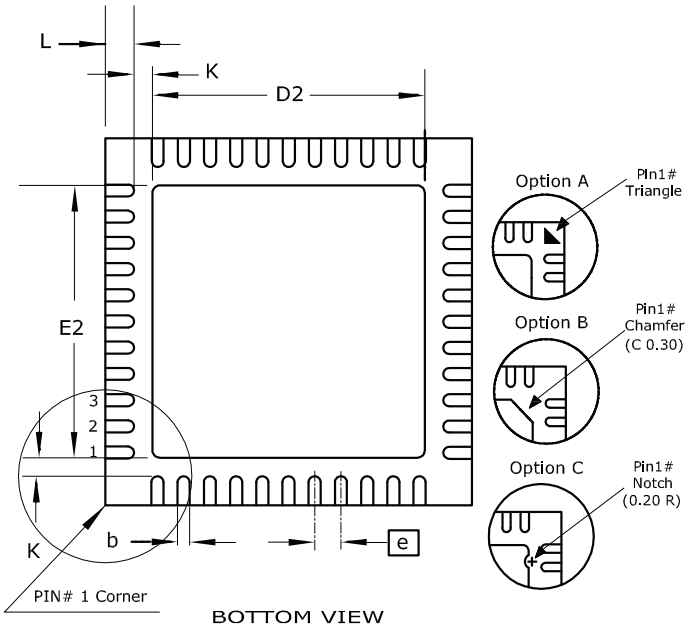
DRAWINGS NOT SCALED



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	-----	1.00	
A1	----	0.02	0.05	
A3		0.20 REF		
D/E	6.90	7.00	7.10	
D2/E2	5.00	5.20	5.40	
L	0.45	0.55	0.65	
K	----	0.35	----	
b	0.18	0.23	0.30	2
e		0.50 BSC		
n		44		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VKKD-1 for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

02/17/2012

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact: packagedrawings@atmel.com**	PW, 44 Lds - 0.50mm Pitch, 7x7x1mm Body size Very Thin Quad Flat Package (Punched) (VQFN) Sawn	ZCP	PW	H

36. Electrical Characteristics

All typical values are measured at T = 25°C unless other temperature condition is given. All minimum and maximum values are valid across operating temperature and voltage unless other conditions are given.

36.1 ATxmega16A4U

36.1.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 36-1 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 36-1. Absolute maximum ratings.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	mA
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC}+0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	°C

36.1.2 General Operating Ratings

The device must operate within the ratings listed in Table 36-2 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 36-2. General operating conditions.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	V
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	°C

36.1.3 Current consumption

Table 36-4. Current consumption for Active mode and sleep modes.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		40		µA
			V_{CC} = 3.0V		80		
		1MHz, Ext. Clk	V_{CC} = 1.8V		230		
			V_{CC} = 3.0V		480		
		2MHz, Ext. Clk	V_{CC} = 1.8V		430	600	
			V_{CC} = 3.0V		0.9	1.4	mA
		32MHz, Ext. Clk			9.6	12	
	Idle power consumption (1)	32kHz, Ext. Clk	V_{CC} = 1.8V		2.4		µA
			V_{CC} = 3.0V		3.9		
		1MHz, Ext. Clk	V_{CC} = 1.8V		62		
			V_{CC} = 3.0V		118		
		2MHz, Ext. Clk	V_{CC} = 1.8V		125	225	
			V_{CC} = 3.0V		240	350	
		32MHz, Ext. Clk			3.8	5.5	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			1.2	4.5	
		T = 105°C			3.5	6.0	
		WDT and Sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.3	3.0	
		WDT and Sampled BOD enabled, T = 85°C			2.4	6.0	
		WDT and Sampled BOD enabled, T = 105°C			4.5	8.0	
	Power-save power consumption (2)	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.2		µA
			V_{CC} = 3.0V		1.3		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.6	2.0	
			V_{CC} = 3.0V		0.7	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.8	3.0	
			V_{CC} = 3.0V		1.0	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		320		µA

Notes:
1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

36.2.6 ADC characteristics

Table 36-40. Power supply, reference and input range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	V
V_{REF}	Reference voltage		1		AV_{CC}- 0.6	V
R_{in}	Input resistance	Switched		4.0		kΩ
C_{sample}	Input capacitance	Switched		4.4		pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7		pF
V_{IN}	Input range		-0.1		AV_{CC}+0.1	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	V
	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF}-ΔV	V
ΔV	Fixed offset voltage			190		LSB

Table 36-41. Clock and timing.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC clock frequency	Maximum is 1/4 of peripheral clock frequency	100		2000	kHz
		Measuring internal signals	100		125	
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off	100		2000	ksps
		CURRLIMIT = LOW	100		1500	
		CURRLIMIT = MEDIUM	100		1000	
		CURRLIMIT = HIGH	100		500	
	Sampling time	1/2 Clk_{ADC} cycle	0.25		5	µs
	Conversion time (latency)	(RES+2)/2+(GAIN !=0) RES (Resolution) = 8 or 12	5		8	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	Clk_{ADC} cycles
	ADC settling time	After changing reference or input mode		7	7	Clk_{ADC} cycles
		After ADC flush		1	1	

Table 36-60. External clock with prescaler [1] for system clock.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency [2]	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes: 1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

36.2.14.7 External 16MHz crystal oscillator and XOSC characteristic

Table 36-61. External 16MHz crystal oscillator and XOSC characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0		<10		ns
			FRQRANGE=1, 2, or 3		<1		
		XOSCPWR=1			<1		
	Long term jitter	XOSCPWR=0	FRQRANGE=0		<6		ns
			FRQRANGE=1, 2, or 3		<0.5		
		XOSCPWR=1			<0.5		
	Frequency error	XOSCPWR=0	FRQRANGE=0		<0.1		%
			FRQRANGE=1		<0.05		
			FRQRANGE=2 or 3		<0.005		
		XOSCPWR=1			<0.005		
	Duty cycle	XOSCPWR=0	FRQRANGE=0		40		%
			FRQRANGE=1		42		
			FRQRANGE=2 or 3		45		
		XOSCPWR=1			48		

36.2.15 SPI Characteristics

Figure 36-12. SPI timing requirements in master mode.

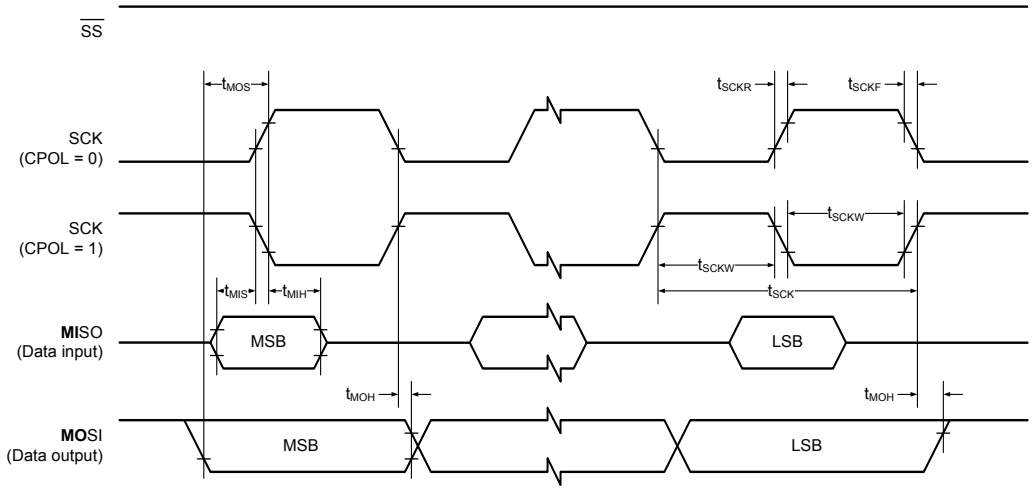


Figure 36-13. SPI timing requirements in slave mode.

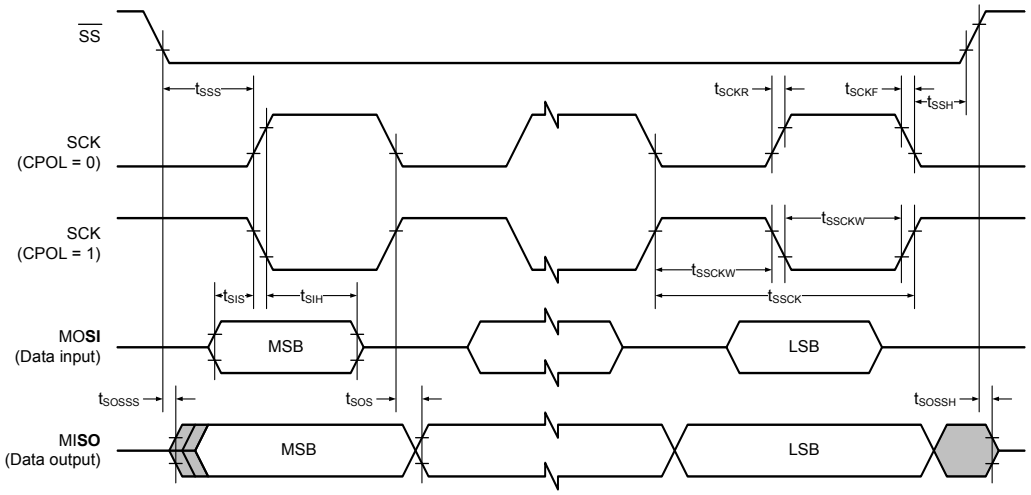


Figure 37-11. Idle mode supply current vs. V_{CC}.

f_{SYS} = 1MHz external clock.

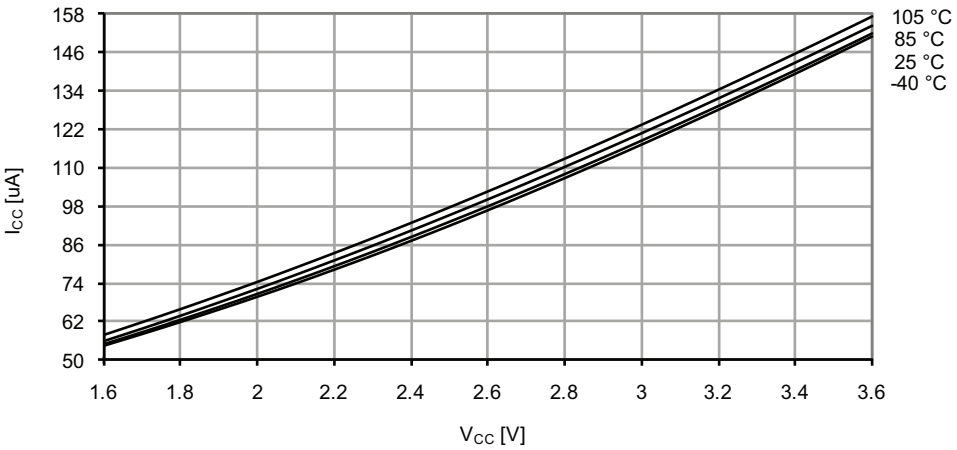
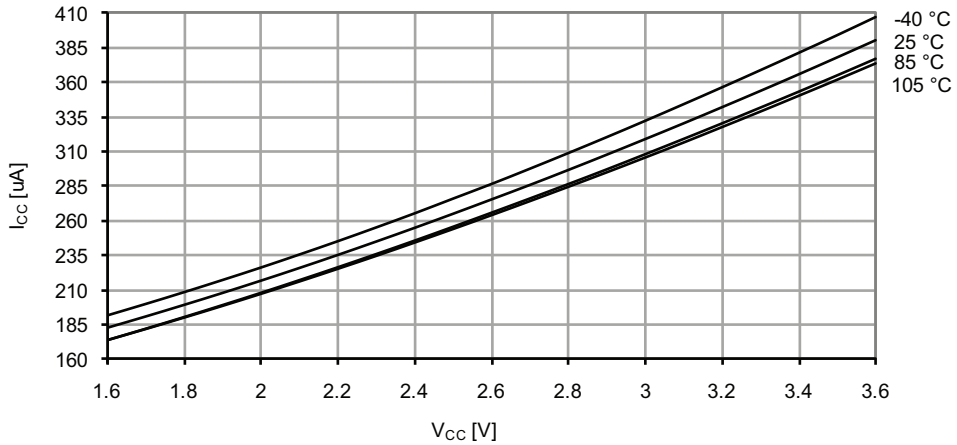


Figure 37-12. Idle mode supply current vs. V_{CC}.

f_{SYS} = 2MHz internal oscillator.



37.1.2.3 Thresholds and Hysteresis

Figure 37-32. I/O pin input threshold voltage vs. V_{CC}.
T = 25°C.

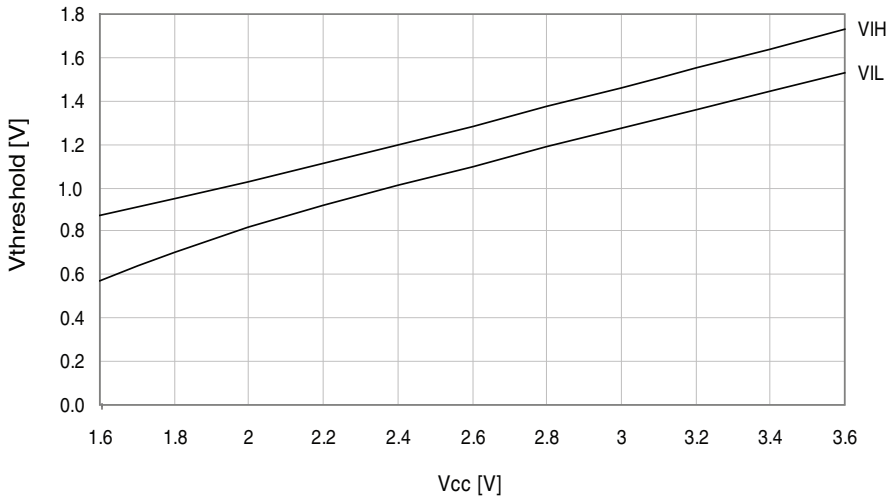


Figure 37-33. I/O pin input threshold voltage vs. V_{CC}.
V_{IH} I/O pin read as "1".

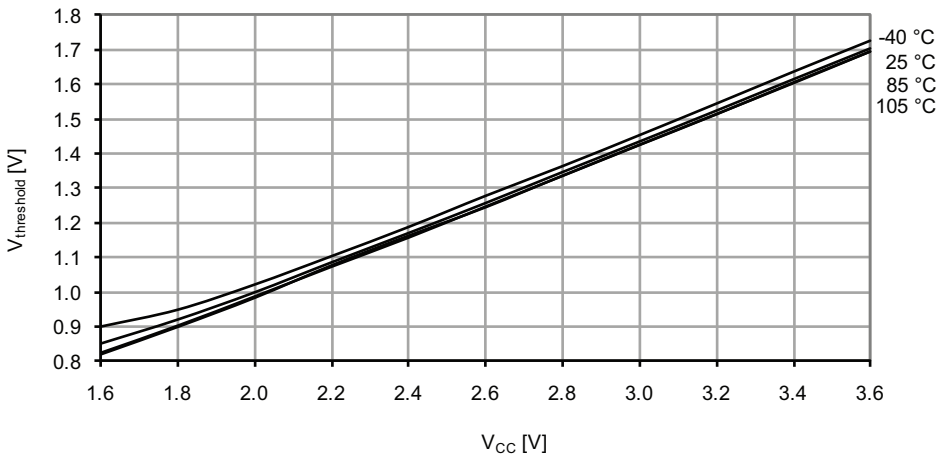


Figure 37-40. DNL error vs. sample rate.

T = 25°C, V_{CC} = 3.6V, V_{REF} = 3.0V external.

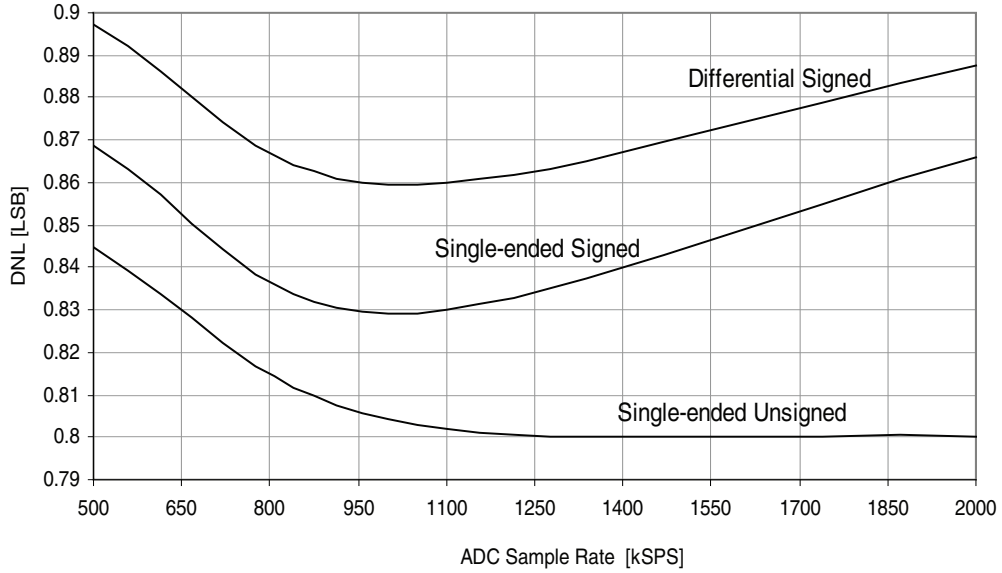


Figure 37-41. DNL error vs. input code.

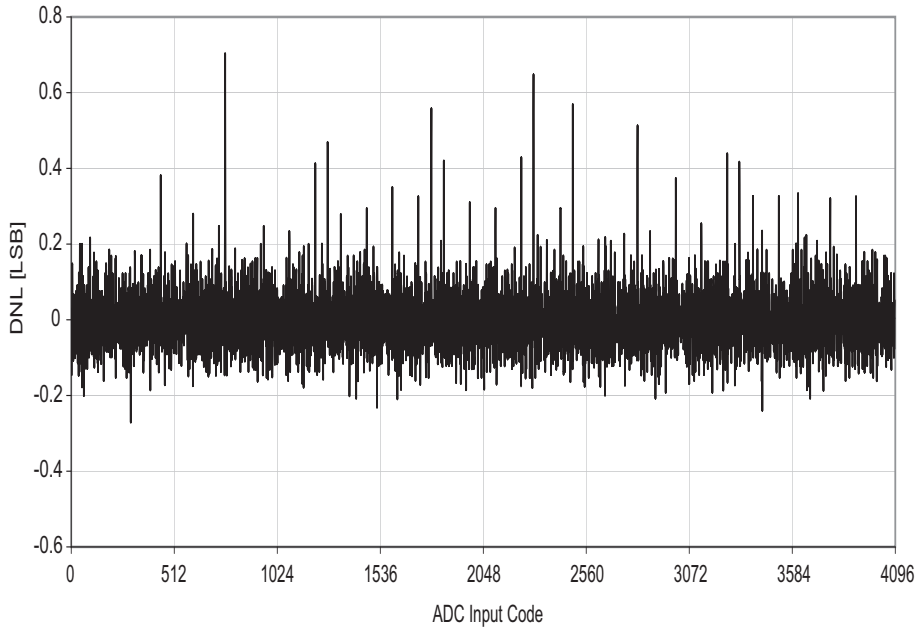


Figure 37-46. Offset error vs. V_{CC}.

T = 25°C, V_{REF} = external 1.0V, ADC sampling speed = 500ksps.

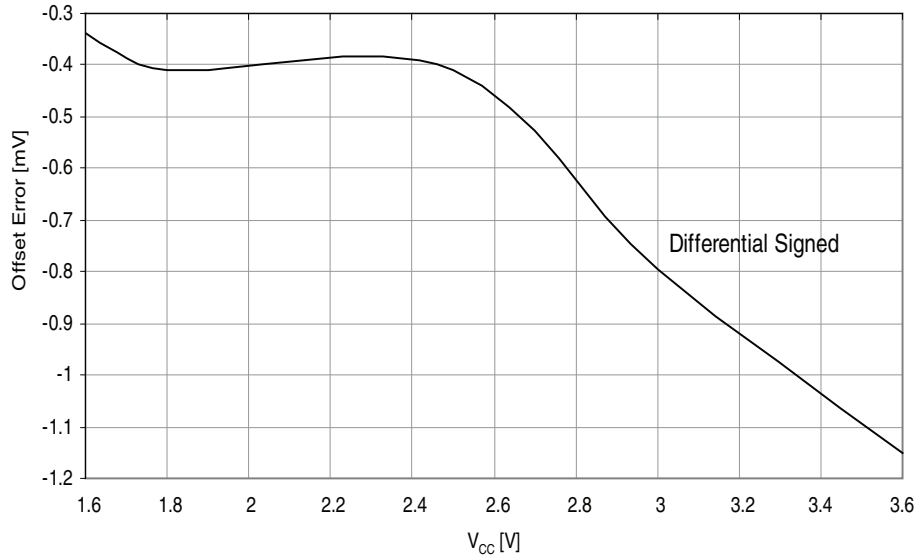
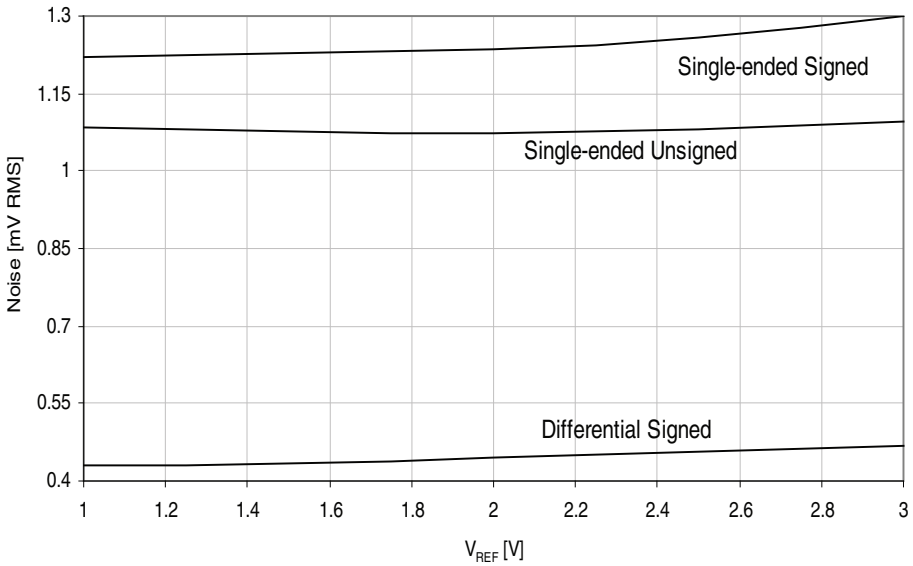


Figure 37-47. Noise vs. V_{REF}.

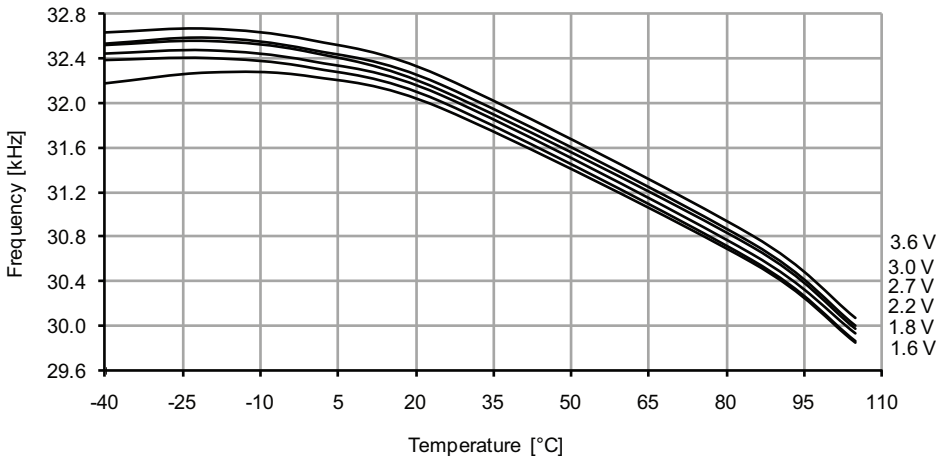
T = 25°C, V_{CC} = 3.6V, ADC sampling speed = 500ksps.



37.1.10 Oscillator Characteristics

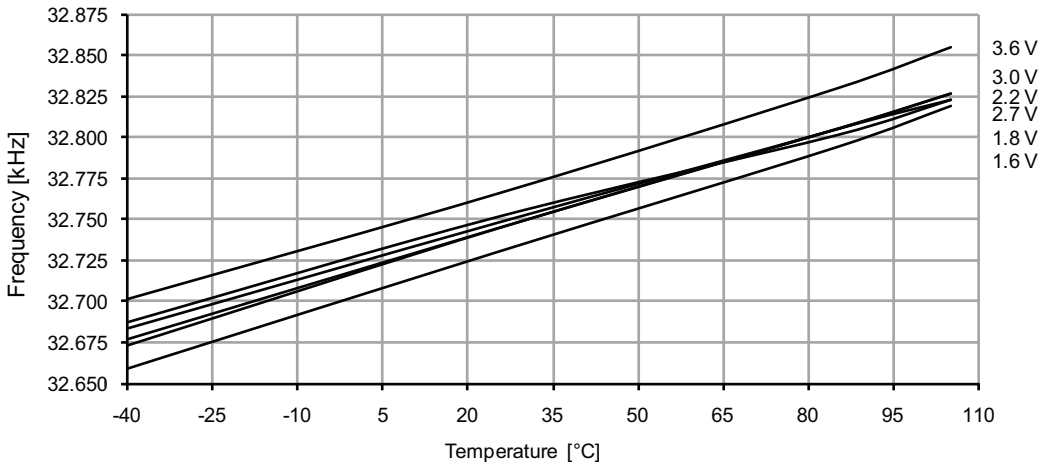
37.1.10.1 Ultra Low-Power internal oscillator

Figure 37-70. Ultra Low-Power internal oscillator frequency vs. temperature.



37.1.10.2 32.768kHz Internal Oscillator

Figure 37-71. 32.768kHz internal oscillator frequency vs. temperature.



37.1.12 PDI characteristics

Figure 37-84. Maximum PDI frequency vs. V_{CC}.

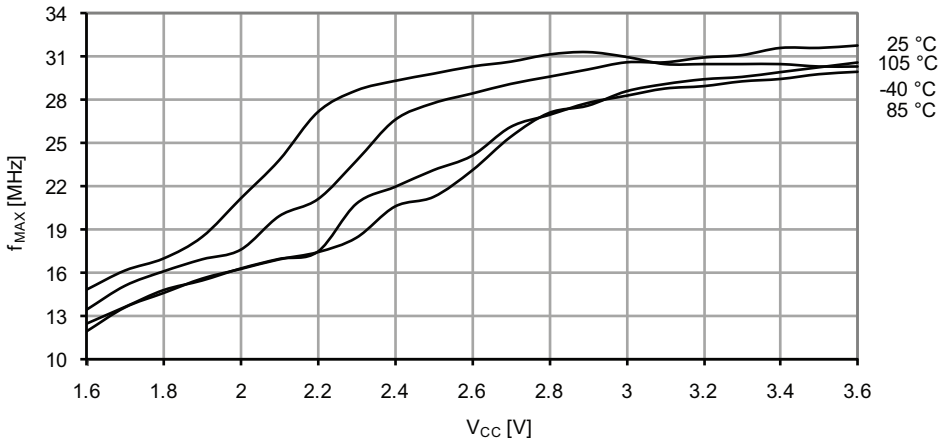
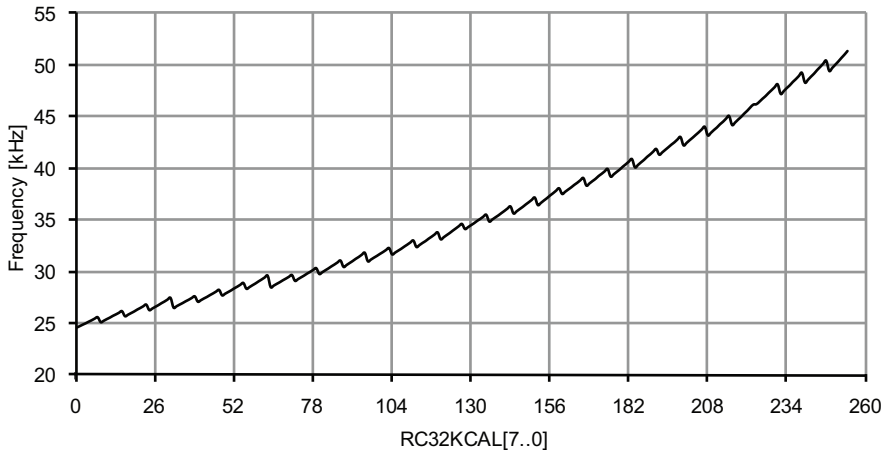


Figure 37-156. 32.768kHz internal oscillator frequency vs. calibration value.

V_{CC} = 3.0V, T = 25°C.



37.2.10.3 2MHz Internal Oscillator

Figure 37-157. 2MHz internal oscillator frequency vs. temperature.

DFLL disabled.

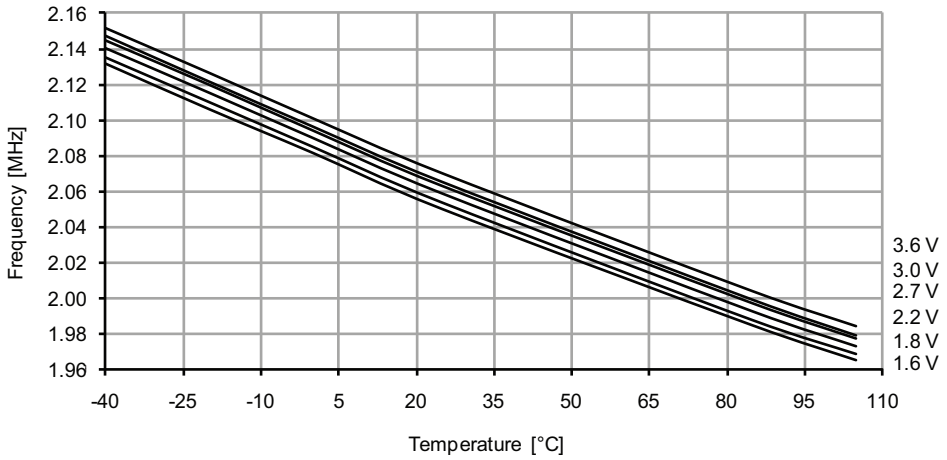
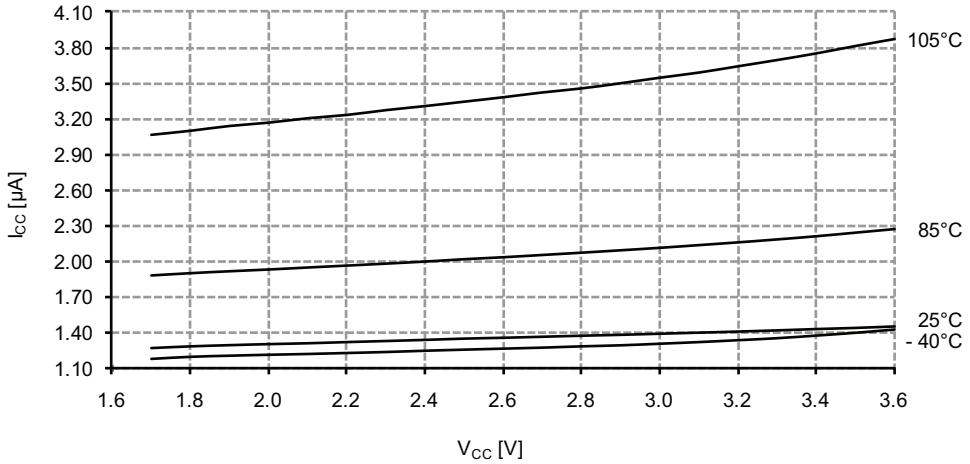


Figure 37-185. Power-down mode supply current vs. V_{CC}.

Watchdog and sampled BOD enabled.



37.3.1.4 Power-save mode supply current

Figure 37-186. Power-save mode supply current vs.V_{CC}.

Real Time Counter enabled and running from 1.024kHz output of 32.768kHz TOSC.

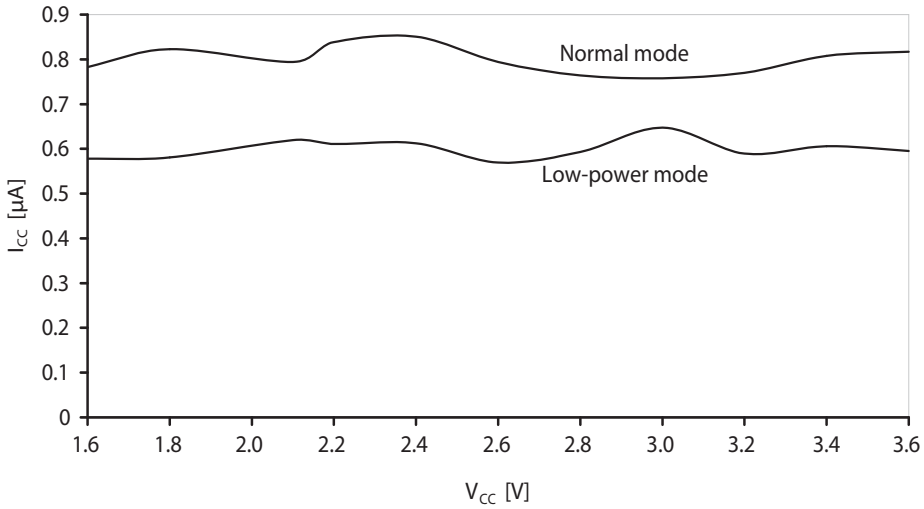


Figure 37-207. DNL error vs. external V_{REF}.

T = 25°C, V_{CC} = 3.6V, external reference.

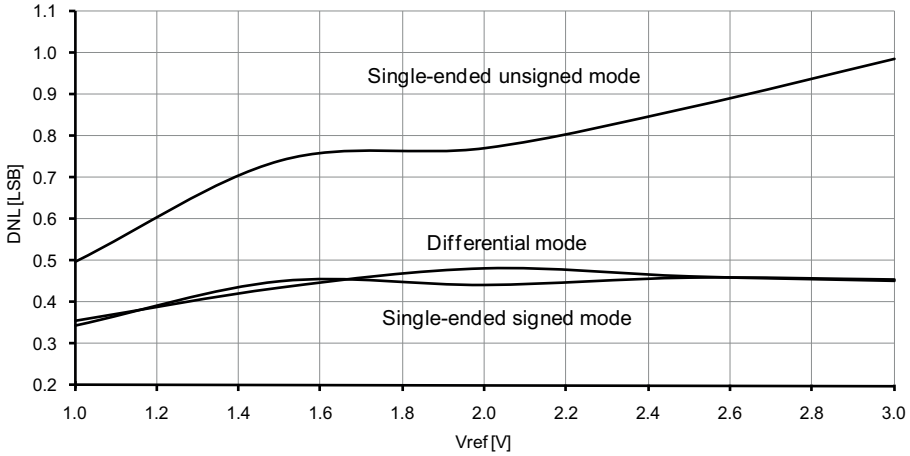
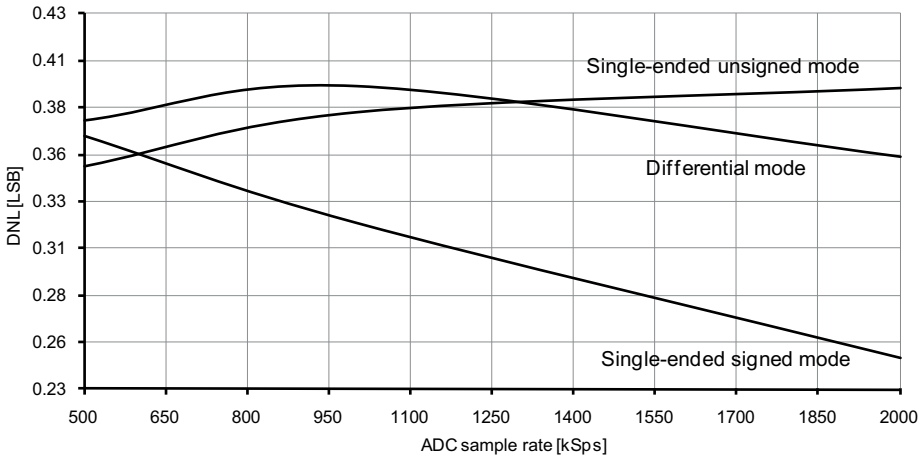


Figure 37-208. DNL error vs. sample rate.

T = 25°C, V_{CC} = 2.7V, V_{REF} = 1.0V external.



37.4.1.5 Standby mode supply current

Figure 37-271. Standby supply current vs. V_{CC}.

Standby, f_{SYS} = 1MHz

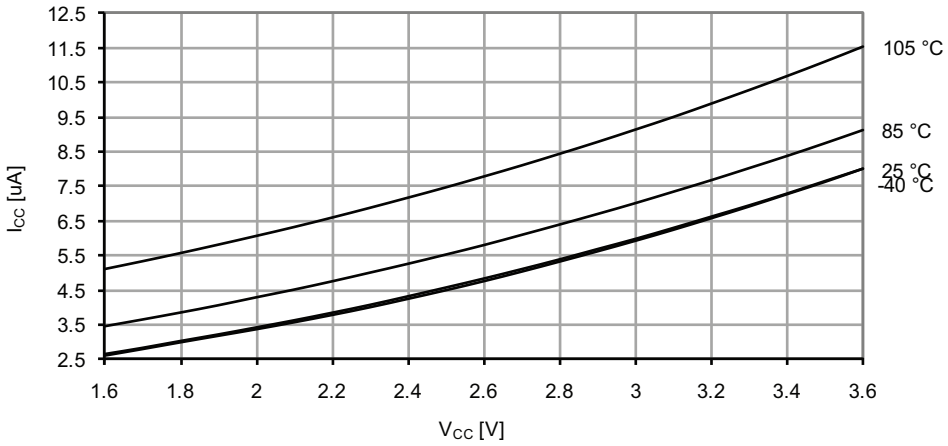


Figure 37-272. Standby supply current vs. V_{CC}.

T = 25°C, running from different crystal oscillators

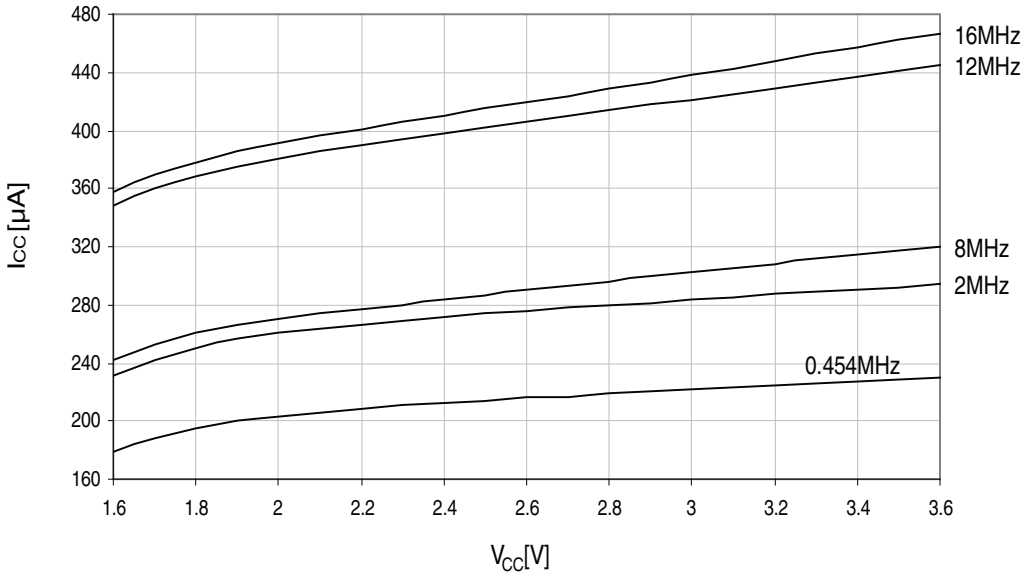


Figure 37-305. Analog comparator hysteresis vs. V_{CC}.

Low power, small hysteresis

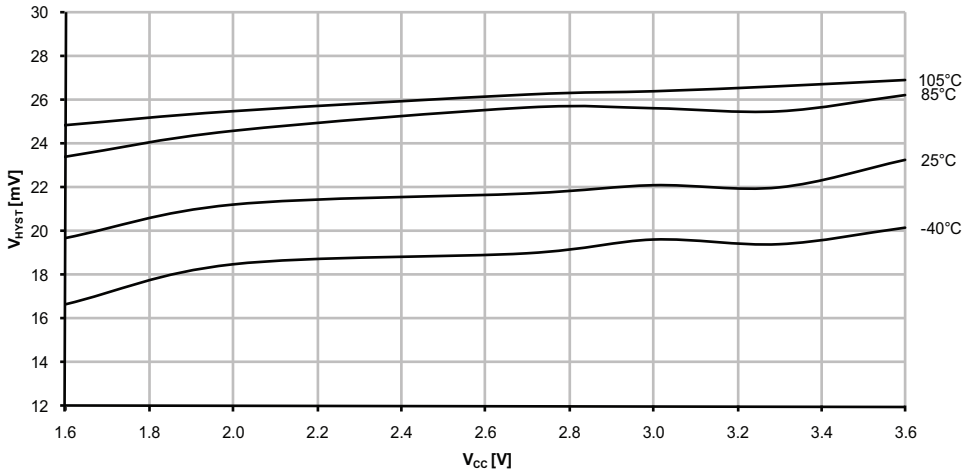


Figure 37-306. Analog comparator hysteresis vs. V_{CC}.

High-speed mode, large hysteresis

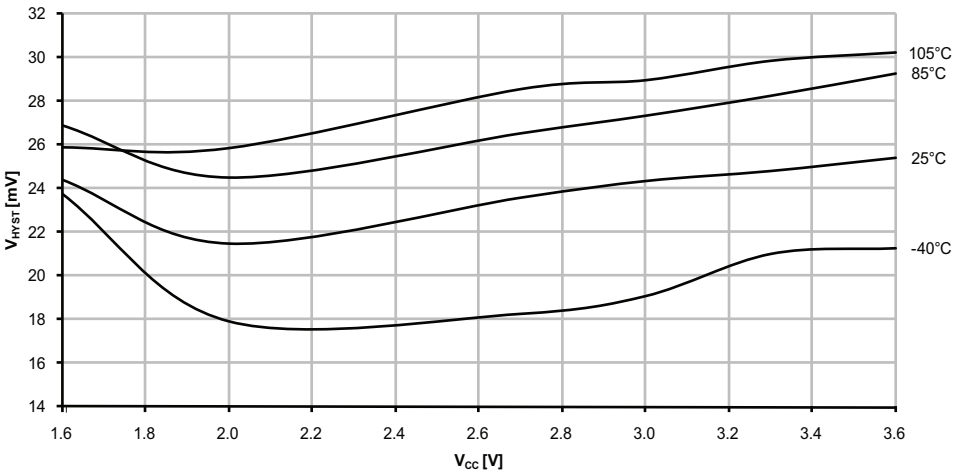
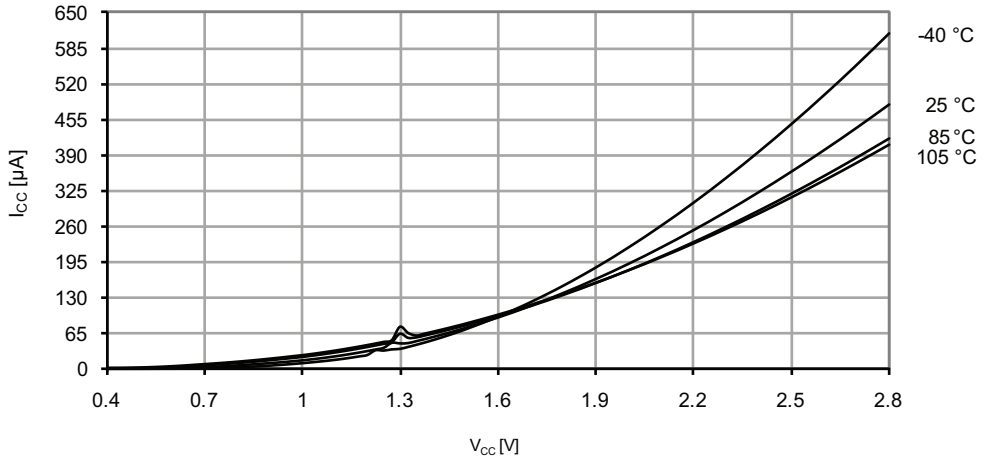


Figure 37-321. Power-on reset current consumption vs. V_{CC}

BOD level = 3.0V, enabled in sampled mode



37.4.10 Oscillator Characteristics

37.4.10.1 Ultra Low-Power internal oscillator

Figure 37-322. Ultra Low-Power internal oscillator frequency vs. temperature.