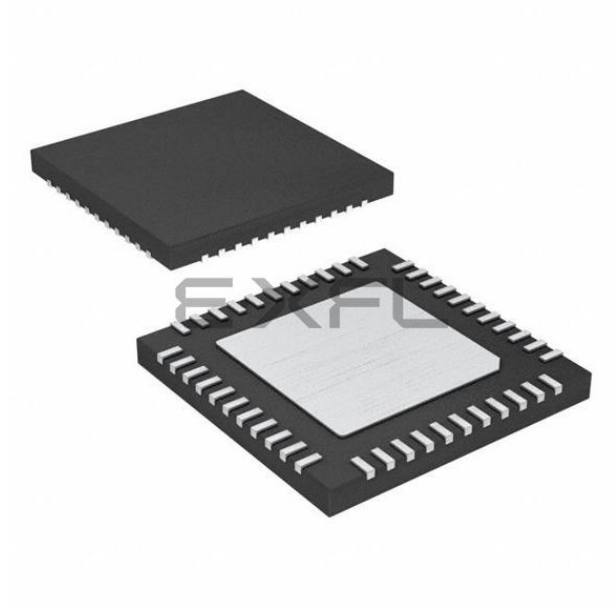

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega64a4u-mn

13. WDT – Watchdog Timer

13.1 Features

- Issues a device reset if the timer is not reset before its timeout period
- Asynchronous operation from dedicated oscillator
- 1kHz output of the 32kHz ultra low power oscillator
- 11 selectable timeout periods, from 8ms to 8s
- Two operation modes:
  - Normal mode
  - Window mode
- Configuration lock to prevent unwanted changes

13.2 Overview

The watchdog timer (WDT) is a system function for monitoring correct program operation. It makes it possible to recover from error situations such as runaway or deadlocked code. The WDT is a timer, configured to a predefined timeout period, and is constantly running when enabled. If the WDT is not reset within the timeout period, it will issue a microcontroller reset. The WDT is reset by executing the WDR (watchdog timer reset) instruction from the application code.

The window mode makes it possible to define a time slot or window inside the total timeout period during which WDT must be reset. If the WDT is reset outside this window, either too early or too late, a system reset will be issued. Compared to the normal mode, this can also catch situations where a code error causes constant WDR execution.

The WDT will run in active mode and all sleep modes, if enabled. It is asynchronous, runs from a CPU-independent clock source, and will continue to operate to issue a system reset even if the main clocks fail.

The configuration change protection mechanism ensures that the WDT settings cannot be changed by accident. For increased safety, a fuse for locking the WDT settings is also available.

20. RTC – 16-bit Real-Time Counter

20.1 Features

- 16-bit resolution
- Selectable clock source
  - 32.768kHz external crystal
  - External clock
  - 32.768kHz internal oscillator
  - 32kHz internal ULP oscillator
- Programmable 10-bit clock prescaling
- One compare register
- One period register
- Clear counter on period overflow
- Optional interrupt/event on overflow and compare match

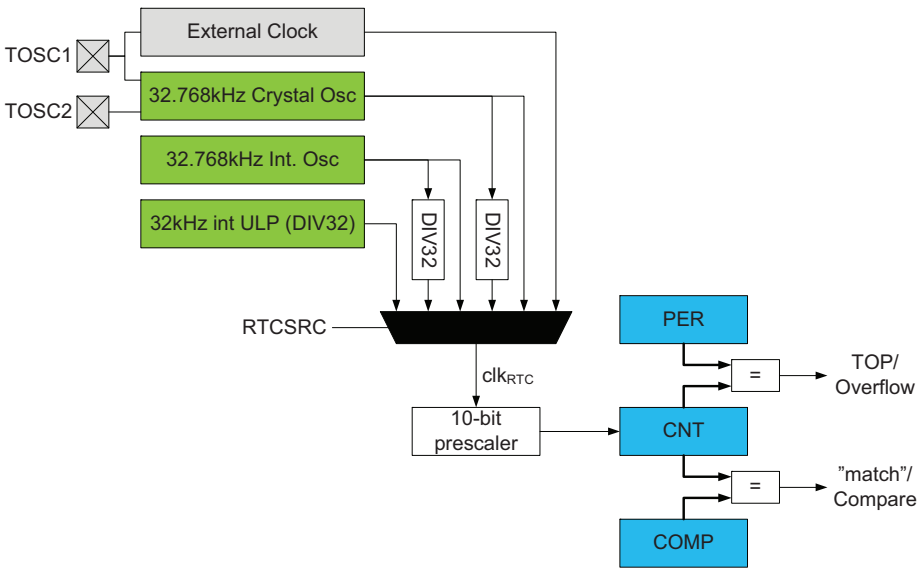
20.2 Overview

The 16-bit real-time counter (RTC) is a counter that typically runs continuously, including in low-power sleep modes, to keep track of time. It can wake up the device from sleep modes and/or interrupt the device at regular intervals.

The reference clock is typically the 1.024kHz output from a high-accuracy crystal of 32.768kHz, and this is the configuration most optimized for low power consumption. The faster 32.768kHz output can be selected if the RTC needs a resolution higher than 1ms. The RTC can also be clocked from an external clock signal, the 32.768kHz internal oscillator or the 32kHz internal ULP oscillator.

The RTC includes a 10-bit programmable prescaler that can scale down the reference clock before it reaches the counter. A wide range of resolutions and time-out periods can be configured. With a 32.768kHz clock source, the maximum resolution is 30.5µs, and time-out periods can range up to 2000 seconds. With a resolution of 1s, the maximum timeout period is more than18 hours (65536 seconds). The RTC can give a compare interrupt and/or event when the counter equals the compare register value, and an overflow interrupt and/or event when it equals the period register value.

Figure 20-1. Real-time counter overview.



32.2 Alternate Pin Functions

The tables below show the primary/default function for each pin on a port in the first column, the pin number in the second column, and then all alternate pin functions in the remaining columns. The head row shows what peripheral that enable and use the alternate pin functions.

For better flexibility, some alternate functions also have selectable pin locations for their functions, this is noted under the first table where this apply.

Table 32-1. Port A - alternate functions.

PORT A	PIN #	INTERRUPT	ADCA POS/ GAINPOS	ADCA NEG	ADCA GAINNEG	ACA POS	ACA NEG	ACAOUT	REFA
GND	38								
AVCC	39								
PA0	40	SYNC	ADC0	ADC0		AC0	AC0		AREF
PA1	41	SYNC	ADC1	ADC1		AC1	AC1		
PA2	42	SYNC/ASYNC	ADC2	ADC2		AC2			
PA3	43	SYNC	ADC3	ADC3		AC3	AC3		
PA4	44	SYNC	ADC4		ADC4	AC4			
PA5	1	SYNC	ADC5		ADC5	AC5	AC5		
PA6	2	SYNC	ADC6		ADC6	AC6		AC1OUT	
PA7	3	SYNC	ADC7		ADC7		AC7	AC0OUT	

Table 32-2. Port B - alternate functions.

PORT B	PIN #	INTERRUPT	ADCA POS	DACB	REFB
PB0	4	SYNC	ADC8		AREF
PB1	5	SYNC	ADC9		
PB2	6	SYNC/ASYNC	ADC10	DAC0	
PB3	7	SYNC	ADC11	DAC1	

Mnemonics	Operands	Description	Operation	Flags	#Clocks
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Two's Complement Overflow	V ← 1	V	1
CLV		Clear Two's Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
MCU control instructions					
BREAK		Break	(See specific descr. for BREAK)	None	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR)	None	1

Notes:
1. Cycle times for Data memory accesses assume internal memory accesses, and are not valid for accesses via the external RAM interface.
2. One extra cycle must be added when accessing Internal SRAM.

36.1.6 ADC characteristics

Table 36-8. Power supply, reference and input range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	V
V_{REF}	Reference voltage		1.0		AV_{CC}- 0.6	V
R_{in}	Input resistance	Switched		4.0		kΩ
C_{sample}	Input capacitance	Switched		4.4		pF
R_{AREF}	Reference input resistance	(leakage only)		>10		MΩ
C_{AREF}	Reference input capacitance	Static load		7.0		pF
V_{IN}	Input range		-0.1		AV_{CC}+0.1	V
	Conversion range	Differential mode, Vinp - Vinn	$-V_{REF}$		V_{REF}	V
	Conversion range	Single ended unsigned mode, Vinp	-ΔV		V_{REF}-ΔV	V
ΔV	Fixed offset voltage			190		LSB

Table 36-9. Clock and timing.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{ADC}	ADC Clock frequency	Maximum is 1/4 of peripheral clock frequency	100		2000	kHz
		Measuring internal signals	100		125	
f_{ADC}	Sample rate	Current limitation (CURRLIMIT) off	100		2000	ksps
		CURRLIMIT = LOW	100		1500	
		CURRLIMIT = MEDIUM	100		1000	
		CURRLIMIT = HIGH	100		500	
	Sampling time	1/2 Clk_{ADC} cycle	0.25		5	µs
	Conversion time (latency)	(RES+2)/2+(GAIN !=0) RES (Resolution) = 8 or 12	5		8	Clk_{ADC} cycles
	Start-up time	ADC clock cycles		12	24	Clk_{ADC} cycles
	ADC settling time	After changing reference or input mode		7	7	Clk_{ADC} cycles
		After ADC flush		1	1	

36.1.8 Analog Comparator Characteristics

Table 36-15. Analog Comparator characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{off}	Input offset voltage			<±10		mV
I_{lk}	Input leakage current			<1.0		nA
	Input voltage range		-0.1		AV_{CC}	V
	AC startup time			100		µs
V_{hys1}	Hysteresis, none			0		mV
V_{hys2}	Hysteresis, small	mode = High Speed (HS)		13		mV
		mode = Low Power (LP)		30		
V_{hys3}	Hysteresis, large	mode = HS		30		mV
		mode = LP		60		
t_{delay}	Propagation delay	V_{CC} = 3.0V, T= 85°C mode = HS		30	90	ns
		mode = HS		30		
		V_{CC} = 3.0V, T= 85°C mode = LP		130	500	
		mode = LP		130		
	64-level voltage scaler	Integral non-linearity (INL)		0.3	0.5	lsb

36.1.9 Bandgap and Internal 1.0V Reference Characteristics

Table 36-16. Bandgap and Internal 1.0V reference characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
	Startup time	As reference for ADC or DAC	1 Clk_{PER} + 2.5µs			µs
		As input voltage to ADC and AC		1.5		
	Bandgap voltage			1.1		V
INT1V	Internal 1.00V reference	T= 85°C, after calibration	0.99	1.0	1.01	V
	Variation over voltage and temperature	Relative to T= 85°C, V_{CC} = 3.0V		±1.5		%

36.2 ATxmega32A4U

36.2.1 Absolute Maximum Ratings

Stresses beyond those listed in Table 36-33 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 36-33. Absolute maximum ratings.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		-0.3		4	V
I_{VCC}	Current into a V_{CC} pin				200	mA
I_{GND}	Current out of a Gnd pin				200	mA
V_{PIN}	Pin voltage with respect to Gnd and V_{CC}		-0.5		V_{CC}+0.5	V
I_{PIN}	I/O pin sink/source current		-25		25	mA
T_A	Storage temperature		-65		150	°C
T_j	Junction temperature				150	°C

36.2.2 General Operating Ratings

The device must operate within the ratings listed in Table 36-34 in order for all other electrical characteristics and typical characteristics of the device to be valid.

Table 36-34. General operating conditions.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power supply voltage		1.60		3.6	V
AV_{CC}	Analog supply voltage		1.60		3.6	V
T_A	Temperature range		-40		85	°C
T_j	Junction temperature		-40		105	°C

Table 36-35. Operating voltage and frequency.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clk_{CPU}	CPU clock frequency	V_{CC} = 1.6V	0		12	MHz
		V_{CC} = 1.8V	0		12	
		V_{CC} = 2.7V	0		32	
		V_{CC} = 3.6V	0		32	

The maximum CPU clock frequency depends on V_{CC}. As shown in Figure 36-8 the Frequency vs. V_{CC} curve is linear between 1.8V < V_{CC} < 2.7V.

36.2.3 Current consumption

Table 36-36. Current consumption for Active mode and sleep modes.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Active power consumption[1]	32kHz, Ext. Clk	V_{CC} = 1.8V		40		µA
			V_{CC} = 3.0V		80		
		1MHz, Ext. Clk	V_{CC} = 1.8V		230		
			V_{CC} = 3.0V		480		
		2MHz, Ext. Clk	V_{CC} = 1.8V		430	600	
			V_{CC} = 3.0V		0.9	1.4	mA
		32MHz, Ext. Clk			9.6	12	
	Idle power consumption[1]	32kHz, Ext. Clk	V_{CC} = 1.8V		2.4		µA
			V_{CC} = 3.0V		3.9		
		1MHz, Ext. Clk	V_{CC} = 1.8V		62		
			V_{CC} = 3.0V		118		
		2MHz, Ext. Clk	V_{CC} = 1.8V		125	225	
			V_{CC} = 3.0V		240	350	
		32MHz, Ext. Clk			3.8	5.5	mA
	Power-down power consumption	T = 25°C	V_{CC} = 3.0V		0.1	1.0	µA
		T = 85°C			1.2	4.5	
		T = 105°C			3.5	6.0	
		WDT and sampled BOD enabled, T = 25°C	V_{CC} = 3.0V		1.3	3.0	
		WDT and sampled BOD enabled, T = 85°C			2.4	6.0	
		WDT and sampled BOD enabled, T = 105°C			4.5	8.0	
	Power-save power consumption[2]	RTC from ULP clock, WDT and sampled BOD enabled, T = 25°C	V_{CC} = 1.8V		1.2		µA
			V_{CC} = 3.0V		1.3		
		RTC from 1.024kHz low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.6	2.0	
			V_{CC} = 3.0V		0.7	2.0	
		RTC from low power 32.768kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.8	3.0	
			V_{CC} = 3.0V		1.0	3.0	
	Reset power consumption	Current through $\overline{\text{RESET}}$ pin substracted	V_{CC} = 3.0V		320		

Notes:
1. All Power Reduction Registers set.
2. Maximum limits are based on characterization, and not tested in production.

Table 36-37. Current consumption for modules and peripherals.

Symbol	Parameter	Condition (1)		Min.	Typ.	Max.	Units
I_{CC}	ULP oscillator				1.0		µA
	32.768kHz int. oscillator				27		µA
	2MHz int. oscillator				85		µA
		DFLL enabled with 32.768kHz int. osc. as reference			115		
	32MHz int. oscillator				270		µA
		DFLL enabled with 32.768kHz int. osc. as reference			460		
	PLL	20x multiplication factor, 32MHz int. osc. DIV4 as reference			220		µA
	Watchdog timer				1.0		µA
	BOD	Continuous mode			138		µA
		Sampled mode, includes ULP oscillator			1.2		
	Internal 1.0V reference				100		µA
	Temperature sensor				95		µA
	ADC	250ksps V_{REF} = Ext ref			3.0		mA
			CURRLIMIT = LOW		2.6		
			CURRLIMIT = MEDIUM		2.1		
			CURRLIMIT = HIGH		1.6		
	DAC	250ksps V_{REF} = Ext ref No load	Normal mode		1.9		mA
			Low power mode		1.1		
	AC	High speed mode			330		µA
		Low power mode			130		
	DMA	615kbps between I/O registers and SRAM			108		µA
	Timer/counter				16		µA
	USART	Rx and Tx enabled, 9600 BAUD			2.5		µA
	Flash memory and EEPROM programming				4.0	8.0	mA

Note: 1. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1MHz external clock without prescaling, T = 25°C unless other conditions are given.

36.3.16 Two-Wire Interface Characteristics

Table 36-96 describes the requirements for devices connected to the Two-Wire Interface Bus. The Atmel AVR XMEGA Two-Wire Interface meets or exceeds these requirements under the noted conditions. Timing symbols refer to Figure 36-21.

Figure 36-21.Two-wire interface bus timing.

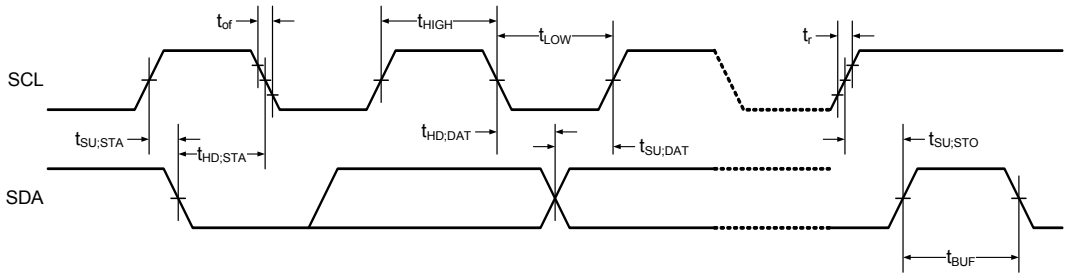


Table 36-96. Two-wire interface characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		$0.7*V_{CC}$		$V_{CC}+0.5$	V
V_{IL}	Input low voltage		-0.5		$0.3*V_{CC}$	V
V_{hys}	Hysteresis of Schmitt trigger inputs		$0.05*V_{CC}$ (1)		0	V
V_{OL}	Output low voltage	3mA, sink current	0		0.4	V
t_r	Rise time for both SDA and SCL		$20+0.1C_b$ (1)(2)		0	ns
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	$10pF < C_b < 400pF$ (2)	$20+0.1C_b$ (1)(2)		300	ns
t_{SP}	Spikes suppressed by input filter		0		50	ns
I_I	Input current for each I/O pin	$0.1V_{CC} < V_I < 0.9V_{CC}$	-10		10	µA
C_I	Capacitance for each I/O pin		0		10	pF
f_{SCL}	SCL clock frequency	f_{PER} (3)>max($10f_{SCL}$, 250kHz)	0		400	kHz
R_P	Value of pull-up resistor	$f_{SCL} \leq 100kHz$	$\frac{V_{CC}-0.4V}{3mA}$		$\frac{100ns}{C_b}$	Ω
		$f_{SCL} > 100kHz$			$\frac{300ns}{C_b}$	
$t_{HD;STA}$	Hold time (repeated) START condition	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
t_{LOW}	Low period of SCL clock	$f_{SCL} \leq 100kHz$	4.7			µs
		$f_{SCL} > 100kHz$	1.3			
t_{HIGH}	High period of SCL clock	$f_{SCL} \leq 100kHz$	4.0			µs
		$f_{SCL} > 100kHz$	0.6			
$t_{SU;STA}$	Set-up time for a repeated START condition	$f_{SCL} \leq 100kHz$	4.7			µs
		$f_{SCL} > 100kHz$	0.6			

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Offset error, input referred	1x gain, normal mode			-2.0		mV
		8x gain, normal mode			-5.0		
		64x gain, normal mode			-4.0		
	Noise	1x gain, normal mode	V_{CC} = 3.6V Ext. V_{REF}		0.5		mV rms
		8x gain, normal mode			1.5		
		64x gain, normal mode			11		

Note: 1. Maximum numbers are based on characterisation and not tested in production, and valid for 5% to 95% input voltage range.

36.4.7 DAC Characteristics

Table 36-108. Power supply, reference and output range.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
AV_{CC}	Analog supply voltage		V_{CC}- 0.3		V_{CC}+ 0.3	
AV_{REF}	External reference voltage		1.0		V_{CC}- 0.6	V
$R_{channel}$	DC output impedance				50	Ω
	Linear output voltage range		0.15		AV_{CC}-0.15	V
R_{AREF}	Reference input resistance			>10		MΩ
CAREF	Reference input capacitance	Static load		7.0		pF
	Minimum Resistance load		1			kΩ
	Maximum capacitance load				100	pF
		1000Ω serial resistance			1	nF
	Output sink/source	Operating within accuracy specification			AV_{CC}/1000	mA
		Safe operation			10	

Table 36-109. Clock and timing.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
f_{DAC}	Conversion rate	C_{load}=100pF, maximum step size	Normal mode	0		1000	ksps
			Low power mode			500	

36.4.14.5 Internal Phase Locked Loop (PLL) characteristics

Table 36-122. Internal PLL characteristics.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{IN}	Input frequency	Output frequency must be within f_{OUT}	0.4		64	MHz
f_{OUT}	Output frequency (1)	V_{CC}= 1.6 - 1.8V	20		48	MHz
		V_{CC}= 2.7 - 3.6V	20		128	
	Start-up time			25		µs
	Re-lock time			25		µs

Note: 1. The maximum output frequency vs. supply voltage is linear between 1.8V and 2.7V, and can never be higher than four times the maximum CPU frequency.

36.4.14.6 External clock characteristics

Figure 36-24. External clock drive waveform

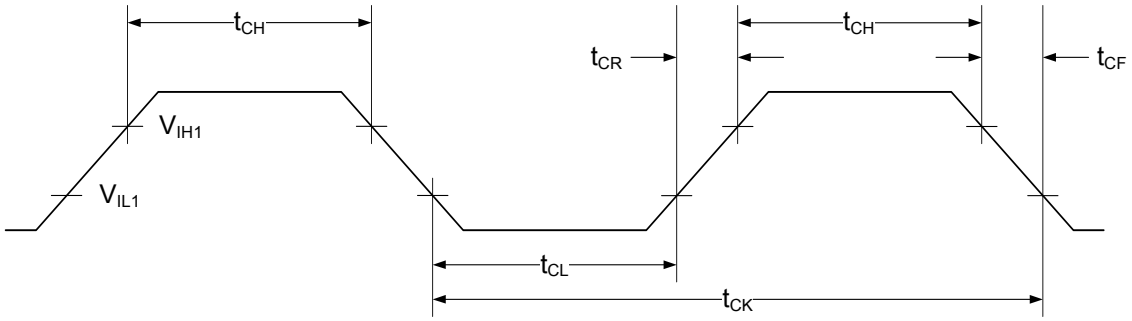


Table 36-123.External clock used as system clock without prescaling.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency (1)	V_{CC} = 1.6 - 1.8V	0		12	MHz
		V_{CC} = 2.7 - 3.6V	0		32	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	83.3			ns
		V_{CC} = 2.7 - 3.6V	31.5			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	30.0			ns
		V_{CC} = 2.7 - 3.6V	12.5			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			10	ns
		V_{CC} = 2.7 - 3.6V			3	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Note: 1. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

Table 36-124. External clock with prescaler [1] for system clock.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$1/t_{CK}$	Clock Frequency [2]	V_{CC} = 1.6 - 1.8V	0		90	MHz
		V_{CC} = 2.7 - 3.6V	0		142	
t_{CK}	Clock Period	V_{CC} = 1.6 - 1.8V	11			ns
		V_{CC} = 2.7 - 3.6V	7			
t_{CH}	Clock High Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CL}	Clock Low Time	V_{CC} = 1.6 - 1.8V	4.5			ns
		V_{CC} = 2.7 - 3.6V	2.4			
t_{CR}	Rise Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
t_{CF}	Fall Time (for maximum frequency)	V_{CC} = 1.6 - 1.8V			1.5	ns
		V_{CC} = 2.7 - 3.6V			1.0	
Δt_{CK}	Change in period from one clock cycle to the next				10	%

Notes:
1. System Clock Prescalers must be set so that maximum CPU clock frequency for device is not exceeded.
2. The maximum frequency vs. supply voltage is linear between 1.6V and 2.7V, and the same applies for all other parameters with supply voltage conditions.

36.4.14.7 External 16MHz crystal oscillator and XOSC characteristic

Table 36-125. External 16MHz crystal oscillator and XOSC characteristics.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
	Cycle to cycle jitter	XOSCPWR=0	FRQRANGE=0		<10		ns
			FRQRANGE=1, 2, or 3		<1		
		XOSCPWR=1			<1		
	Long term jitter	XOSCPWR=0	FRQRANGE=0		<6		ns
			FRQRANGE=1, 2, or 3		<0.5		
		XOSCPWR=1			<0.5		
	Frequency error	XOSCPWR=0	FRQRANGE=0		<0.1		%
			FRQRANGE=1		<0.05		
			FRQRANGE=2 or 3		<0.005		
		XOSCPWR=1			<0.005		

37.1.1.5 Standby mode supply current

Figure 37-19. Standby supply current vs. V_{CC}.

Standby, f_{SYS} = 1MHz.

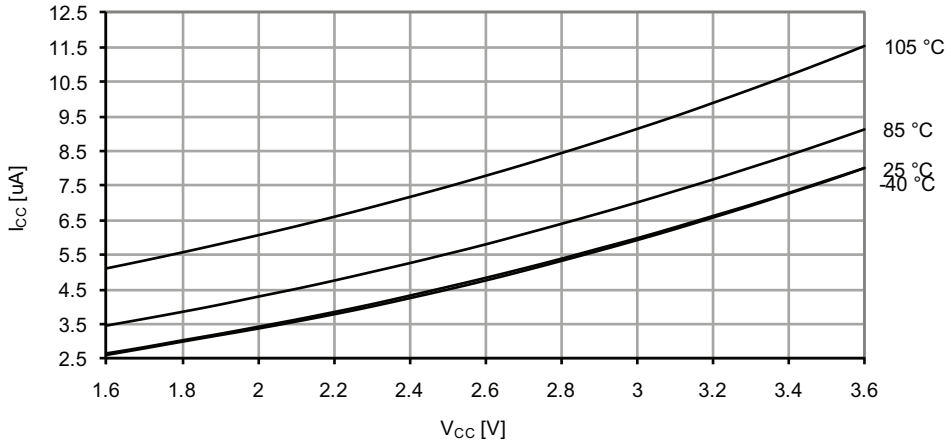
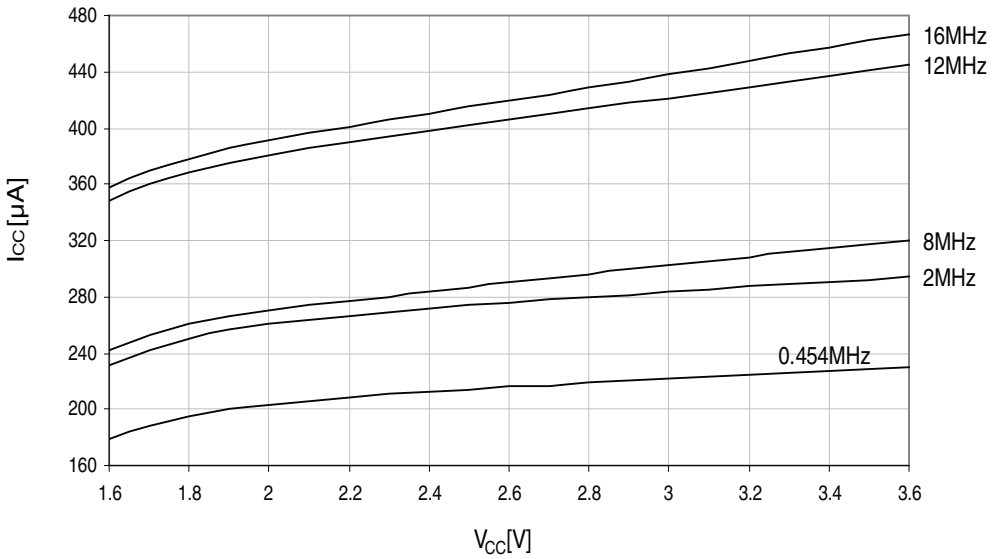


Figure 37-20. Standby supply current vs. V_{CC}.

25°C, running from different crystal oscillators.



37.1.2 I/O Pin Characteristics

37.1.2.1 Pull-up

Figure 37-21. I/O pin pull-up resistor current vs. input voltage.
V_{CC} = 1.8V.

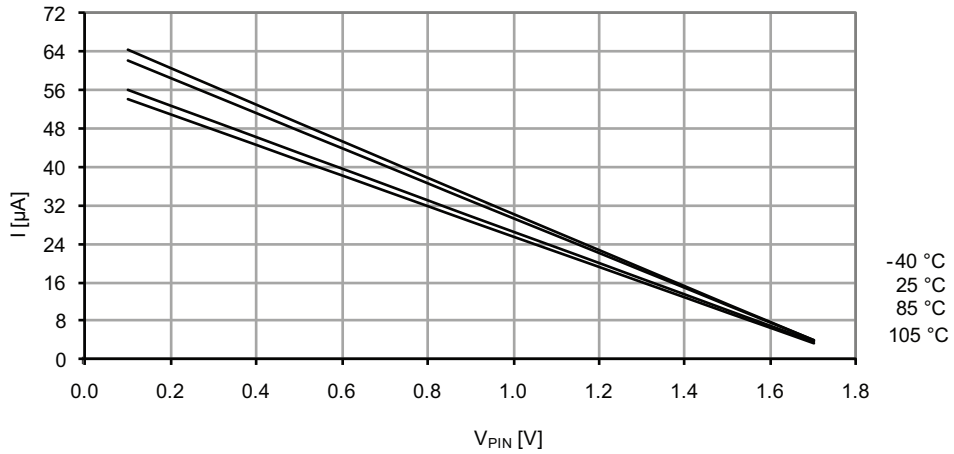
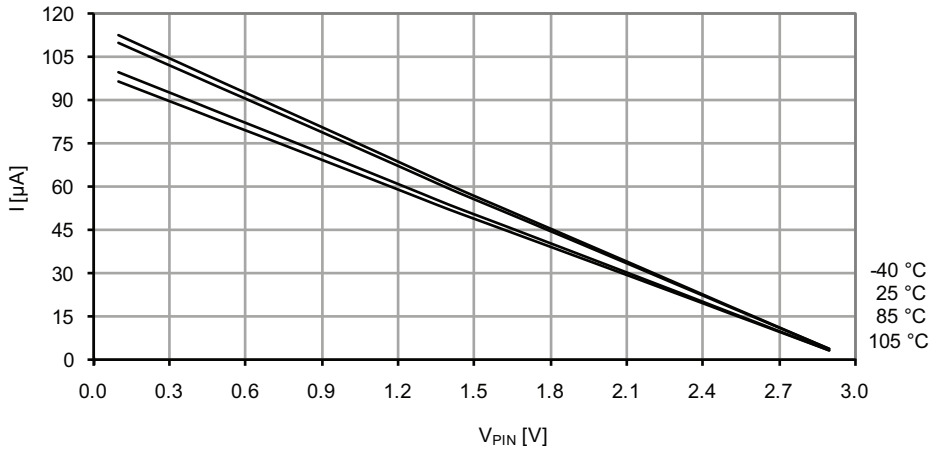


Figure 37-22. I/O pin pull-up resistor current vs. input voltage.
V_{CC} = 3.0V.



37.1.5 Analog Comparator Characteristics

Figure 37-52. Analog comparator hysteresis vs. V_{CC}.

High-speed, small hysteresis.

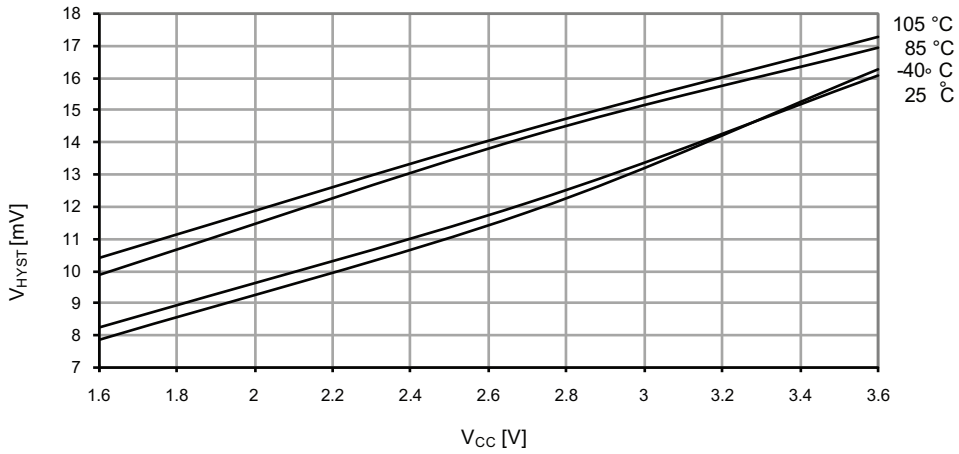


Figure 37-53. Analog comparator hysteresis vs. V_{CC}.

Low power, small hysteresis.

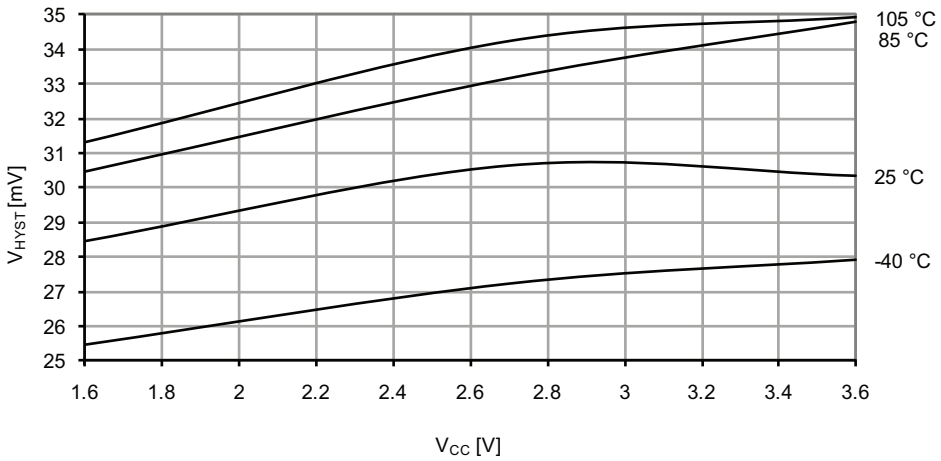


Figure 37-74. 2MHz internal oscillator frequency vs. temperature.

DFLL enabled, from the 32.768kHz internal oscillator .

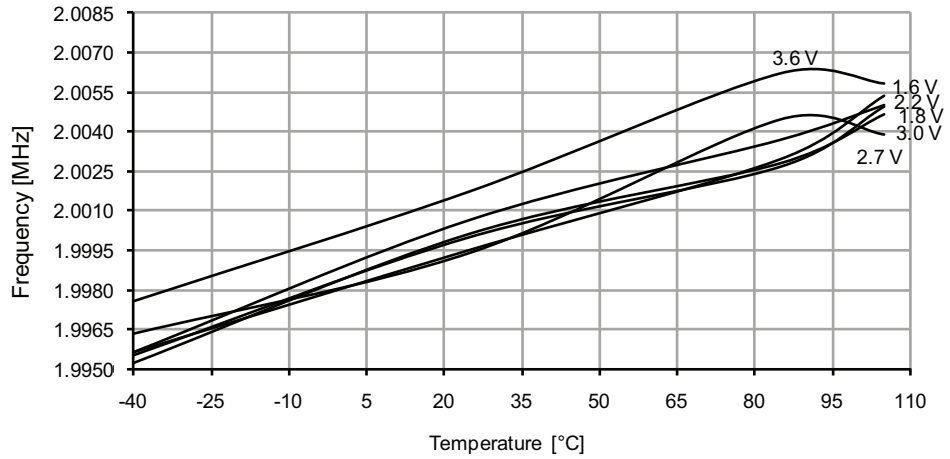


Figure 37-75. 2MHz internal oscillator CALA calibration step size.

V_{CC} = 3V.

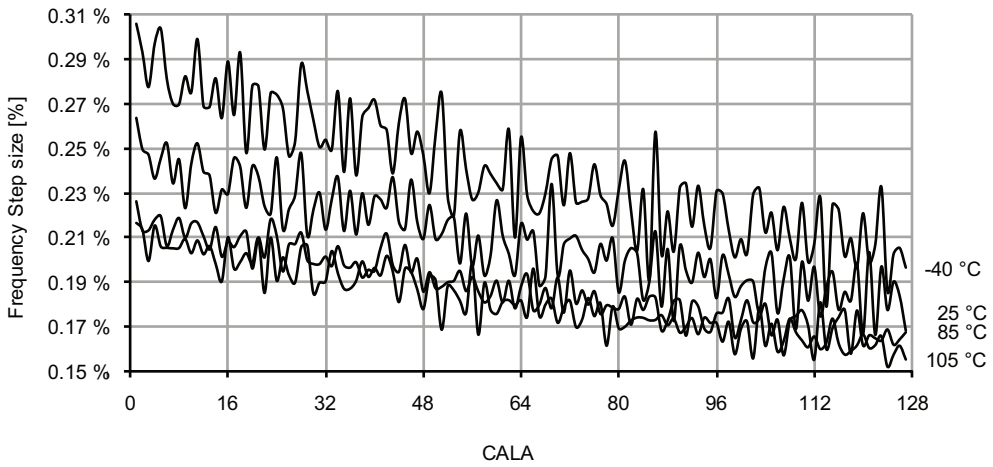


Figure 37-148. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 3.0V.

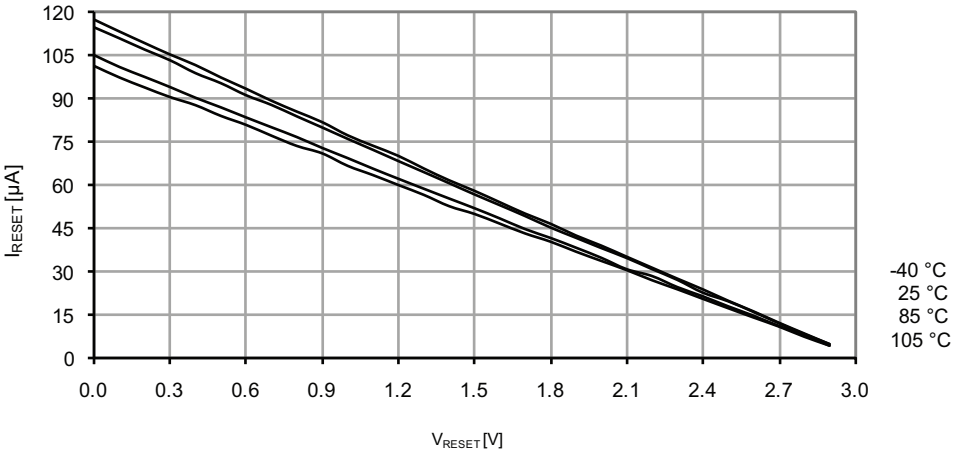


Figure 37-149. Reset pin pull-up resistor current vs. reset pin voltage.

V_{CC} = 3.3V.

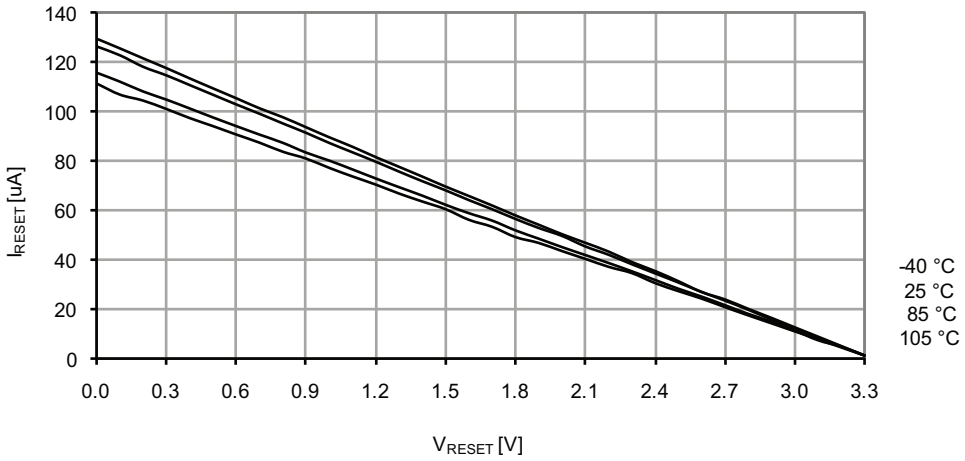
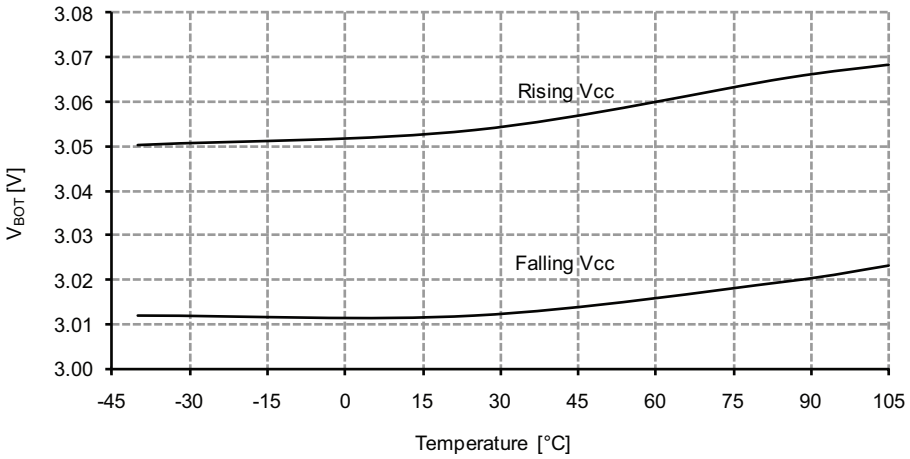


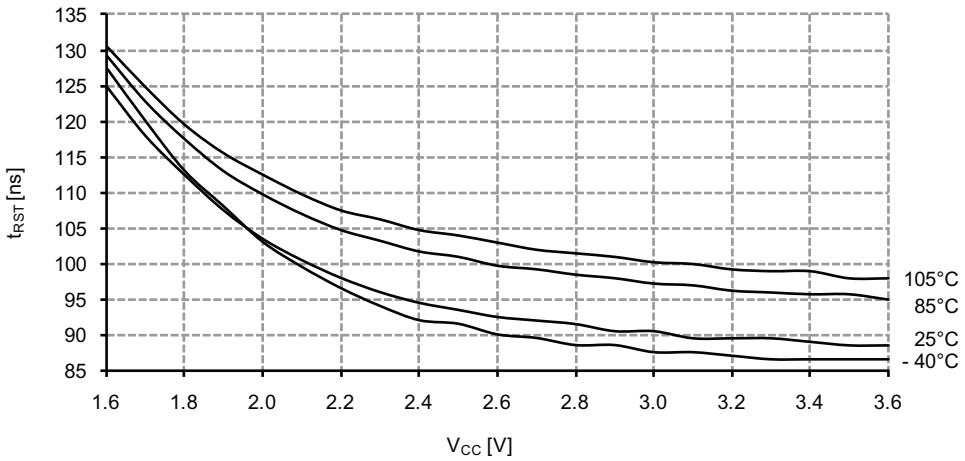
Figure 37-229. BOD thresholds vs. temperature.

BOD level = 3.0V.



37.3.8 External Reset Characteristics

Figure 37-230. Minimum Reset pin pulse width vs. V_{CC}.



38. Errata

38.1 ATxmega16A4U

38.1.1 Rev. E

- ADC may have missing codes in SE unsigned mode at low temp and low Vcc
- CRC fails for Range CRC when end address is the last word address of a flash section
- AWeX fault protection restore is not done correct in Pattern Generation Mode

1. **ADC may have missing codes in SE unsigned mode at low temp and low Vcc**
   The ADC may have missing codes i single ended (SE) unsigned mode below 0C when Vcc is below 1.8V.

   Problem fix/Workaround
   Use the ADC in SE signed mode.

2. **CRC fails for Range CRC when end address is the last word address of a flash section**
   If boot read lock is enabled, the range CRC cannot end on the last address of the application section. If application table read lock is enabled, the range CRC cannot end on the last address before the application table.

   Problem fix/Workaround
   Ensure that the end address used in Range CRC does not end at the last address before a section with read lock enabled. Instead, use the dedicated CRC commands for complete applications sections.

3. **AWeX fault protection restore is not done correct in Pattern Generation Mode**
   When a fault is detected the OUTOVEN register is cleared, and when fault condition is cleared, OUTOVEN is restored according to the corresponding enabled DTI channels. For Common Waveform Channel Mode (CWCM), this has no effect as the OUTOVEN is correct after restoring from fault. For Pattern Generation Mode (PGM), OUTOVEN should instead have been restored according to the DTLSBUF register.

   Problem fix/Workaround
   For CWCM no workaround is required.

   For PGM in latched mode, disable the DTI channels before returning from the fault condition. Then, set correct OUTOVEN value and enable the DTI channels, before the direction (DIR) register is written to enable the correct outputs again.

38.1.2 Rev. A - D

Not sampled.