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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA, FCBGA
Supplier Device Package	624-FCPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6d5eym12ad

8.8.2.1.3 WRITE_FILE

The transaction for the WRITE_FILE command consists of these reports: Report1 for the command phase, Report2 for the data phase, Report3 for the HAB mode, and Report4 to indicate that the data are received in full.

The size of each Report2 is limited to 1024 bytes (limitation of the USB HID protocol). Hence, multiple Report2 packets are sent by the host in the data phase until the entire data is transferred to the device. When the entire data (DATA_COUNT bytes) is received, the device sends Report3 with the HAB mode and Report4 with 0x88888888, indicating that the file download completed.

Report1, Host to Device:

1	Valid values for WRITE_FILE COMMAND, ADDRESS, DATA_COUNT

ID 16-byte SDP command

==========Optional Begin==========

Host sends the ERROR_STATUS command to query if the HAB rejected the address

========== Optional End==========

Report2, Host to Device:

2	File data

ID Max 1024 bytes data per report

Report2, Host to Device:

2	File data

ID Max 1024 bytes data per report

Report3, Device to Host:

3	4 bytes indicating security configuration

ID 4 bytes status

Report4, Response, Device to Host:

Table 9-8. VPU decoding/encoding capabilities (continued)

Dec/Enc	Standard	Profile	Resolution	Bitrate	Comments
	VC1	SP/MP/AP	1080 i/p, 30 fps	45 Mbps	1080p+SD at 30 fps, 720p60
	RV	8/9/10	1080 p, 30 fps	40 Mbps	—
	DivX	3/4/5/6	1080 i/p, 30 fps	40 Mbps	—
	On2 VP8	—	720p, 30 fps	20 Mbps	—
AVS	Jizhun	1080 i/p, 30fp	40 Mbps	—	—
MJPEG	Baseline	8192x8192	120 Mpixel/sec	Perf shown at 4:4:4 format	—
Hardware encoder	MPEG4	Simple	720p, 30 fps	12 Mbps	VPU can generate higher bitrate than the maximum specified by the corresponding standard.
	H.263	P0/P3	4CIF, 30 fps	8 Mbps	
	H.264	BP/CBP	1080p, 30 fps	14 Mbps	
	MJPEG	Baseline	8192 x 8192	160 Mpixel/sec	Perf shown at 4:2:2 format

VPU can also perform the following:

- On-the-fly (90 x n) degree simultaneous rotation and mirroring (n = 0,1,2,3).
- Post-processing
  - De-blocking filtering for MPEG-4
  - De-ringing filtering for MPEG-4 and H.264 decoder

9.7 OpenGL ES 3D Graphics Processing Unit (GPU3Dv4)

9.7.1 OpenGL Overview

9.7.2 OpenGL Features

Summary of features in the GPU3D includes:

- OpenGL ES 2.0 compliance, including extensions; OpenGL ES 1.1; OpenVG 1.1
- IEEE 32-bit floating-point pipeline
- Ultra-threaded, unified vertex and fragment shaders
- Low bandwidth at both high and low data rates
- Low CPU loading
- Up to 12 programmable elements per vertex

21.1.2 Modes and Operations

The ECSPI supports the modes described in the indicated sections:

- Master Mode
- Slave Mode
- Low Power Modes

As described in Operations, the ECSPI supports the operations described in the indicated sections:

- Typical Master Mode
  - Master Mode with SPI_RDY
  - Master Mode with Wait States
  - Master Mode with SS_CTL[3:0] Control
  - Master Mode with Phase Control
- Typical Slave Mode

21.2 External Signals

The following table describes the external signals of ECSPI:

Table 21-1. ECSPI1 External Signals

Signal	Description	Pad	Mode	Direction
ECSPI1_MISO (MISO)	Master data in; slave data out	CSI0_DAT6	ALT2	IO
		DISP0_DAT22	ALT2	
		EIM_D17	ALT1	
		KEY_COL1	ALT0	
ECSPI1_MOSI (MOSI)	Master data out; slave data in	CSI0_DAT5	ALT2	IO
		DISP0_DAT21	ALT2	
		EIM_D18	ALT1	
		KEY_ROW0	ALT0	
ECSPI1_RDY (RDY)	SPI data ready signal	GPIO_19	ALT4	I
ECSPI1_SCLK (SCLK)	SPI clock signal	CSI0_DAT4	ALT2	IO
		DISP0_DAT20	ALT2	
		EIM_D16	ALT1	
		KEY_COL0	ALT0	
ECSPI1_SS0 (SS0)	Chip select signal	CSI0_DAT7	ALT2	IO
		DISP0_DAT23	ALT2	
		EIM_EB2	ALT1	
		KEY_ROW1	ALT0	

Table continues on the next page...

Table 22-7. AXI to Memory Burst Splits Number (continued)

AXI Burst Type	Memory Burst Type Config.	# of accesses to X8 Memory Port size	# of accesses to X16 Memory Port size	# of accesses to X32 Memory Port size
Unaligned Addr.	WRAP16	2 or 3	2	1 or 2
WRAP8	WRAP16	2	1	1
Aligned Addr.	Cont.	1	1	1
WRAP8 Unaligned Addr.	WRAP16	2 or 3	1	2
	Cont.	2	2	2

22.5.9 WAIT_B Signal, RWSC and WWSC bit fields Usage

Most of the external devices supporting burst mode for write or read accesses provide a signal which indicates data is valid on the memory bus (a.k.a. handshake mode). For this mode, RFL and WFL bits should be cleared and RWSC/ WWSC bit fields indicate when the controller should start sampling this signal from the external device or, in other words, how many BCLK cycles should be masked.

For devices which do not use this signal or have a fixed latency ability, the RFL and WFL bits may be set for internal calculation regarding BCLK cycles penalty until data is valid (memory initial access time). For this mode, RWSC/ WWSC indicates when the data is ready for sampling by the controller (read access) or the external device (write access). There is separation between read and write accesses wait-state control. For read access, RWSC bit field is valid and WWSC bit field is ignored; for write access, WWSC is valid and RWSC is ignored.

22.5.10 IPS Register Interface

Access to the registers of the EIM, read or write, is made with IPS protocol signals. The system should avoid changing the registers while master/memory transaction is valid, as this can cause an unknown behavior of the controller.

Register access size is 32-bit as the register size definition, other size of access (byte or half word) is not supported.

Although the IEEE specification dictates that the inner-packet gap should be at least 96 bits, the MAC core is designed to accept frames separated by only 64 10/100-Mbit/s operation (MII) bits.

The MAC core removes the preamble and SFD bytes.

23.6.4.3 MAC address check

The destination address bit 0 differentiates between multicast and unicast addresses.

- If bit 0 is 0, the MAC address is an individual (unicast) address.
- If bit 0 is 1, the MAC address defines a group (multicast) address.
- If all 48 bits of the MAC address are set, it indicates a broadcast address.

23.6.4.3.1 Unicast address check

If a unicast address is received, the destination MAC address is compared to the node MAC address programmed by the host in the PADDR1/2 registers.

If the destination address matches any of the programmed MAC addresses, the frame is accepted.

If Promiscuous mode is enabled (RCR[PROM] = 1) no address checking is performed and all unicast frames are accepted.

23.6.4.3.2 Multicast and unicast address resolution

The hash table algorithm used in the group and individual hash filtering operates as follows.

- The 48-bit destination address is mapped into one of 64 bits, represented by 64 bits in ENET*n*_GAUR/GALR (group address hash match) or ENET*n*_IAUR/IALR (individual address hash match).
- This mapping is performed by passing the 48-bit address through the on-chip 32-bit CRC generator and selecting the six most significant bits of the CRC-encoded result to generate a number between 0 and 63.
- The msb of the CRC result selects ENET*n*_GAUR (msb = 1) or ENET*n*_GALR (msb = 0).
- The five lsbs of the hash result select the bit within the selected register.
- If the CRC generator selects a bit set in the hash table, the frame is accepted; else, it is rejected.

GPMI_DEBUG3 field descriptions

Field	Description
31–16 APB_WORD_ CNTR	Reflects the number of bytes remains to be transferred on the APB bus.
DEV_WORD_ CNTR	Reflects the number of bytes remains to be transferred on the ATA/Nand bus.

29.6.17 GPMI Double Rate Read DLL Control Register Description (GPMI_READ_DDR_DLL_CTRL)

GPMI DDR Read Delay Loop Lock Control Register. This register provides programmability in DDR mode for data input timing and data formats.

GPMI_READ_DDR_DLL_CTRL 0x100

Address: 11_2000h base + 100h offset = 11_2100h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	REF_UPDATE_INT				SLV_UPDATE_INT								RSVD1		SLV_ OVERRIDE_ VAL	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	SLV_OVERRIDE_VAL						SLV_OVERRIDE	REFCLK_ON	GATE_UPDATE	SLV_DLY_TARGET				SLV_FORCE_UPD	RESET	ENABLE
W																
Reset	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

33.5.19 Frame Composer Interrupt Mute Control Register 0 (HDMI_IH_MUTE_FC_STAT0)

- Address Offset: 0x0180
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 180h offset = 12_0180h

Bit	7	6	5	4	3	2	1	0
Read Write	AUDI	ACP	HBR	DST	OBA	AUDS	ACR	NULL
Reset	0	0	0	0	0	0	0	0

HDMI_IH_MUTE_FC_STAT0 field descriptions

Field	Description
7 AUDI	When set to 1, mutes IH_ FC_STAT0[7]
6 ACP	When set to 1, mutes IH_ FC_STAT0[6]
5 HBR	When set to 1, mutes IH_ FC_STAT0[5]
4 DST	When set to 1, mutes IH_ FC_STAT0[4]
3 OBA	When set to 1, mutes IH_ FC_STAT0[3]
2 AUDS	When set to 1, mutes IH_ FC_STAT0[2]
1 ACR	When set to 1, mutes IH_ FC_STAT0[1]
0 NULL	When set to 1, mutes IH_ FC_STAT0[0]

HDMI_PHY_CONF0 field descriptions (continued)

Field	Description
0 seldipif	Select interface control. Value after Reset: 0b

33.5.216 PHY Test Interface Register 0 (HDMI_PHY_TST0)

PHY TX mapped text interface (control). For more information, refer to the DesignWare Cores HDMI TX PHY Databook.

- Address Offset: 0x3001
- Size: 8 bits
- Value after Reset: 0x00
- Access: Read/Write

Address: 12_0000h base + 3001h offset = 12_3001h

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved		testclr	testen	Reserved			testclk
Reset	0	0	0	0	0	0	0	0

HDMI_PHY_TST0 field descriptions

Field	Description
7–6 -	This field is reserved. Reserved
5 testclr	Enable TMDS drivers, bias and tmds digital logic. Value after Reset: 0b
4 testen	Reserved. Spare control pins. Value after Reset: 0b
3–1 -	This field is reserved. Reserved
0 testclk	Test clock signal. Value after Reset: 0b

33.5.217 PHY Test Interface Register 1 (HDMI_PHY_TST1)

PHY TX mapped text interface (data in). For more information, refer to the DesignWare Cores HDMI TX PHY Databook.

- Address Offset: 0x3002
- Size: 8 bits

NOTE

The I2C is designed to be compatible with the Philips™ I2C bus protocol. For information on system configuration, protocol, and restrictions, see the *I2C Bus Specification*, version 2.1, by Philips Semiconductors. The I2C supports Standard and Fast modes only.

35.4.2 Arbitration procedure

If multiple devices simultaneously request the bus, the bus clock is determined by a synchronization procedure in which the low period equals the longest clock-low period among the devices, and the high period equals the shortest. A data arbitration procedure determines the relative priority of competing devices.

A device loses arbitration if it sends logic high while another sends logic low; it immediately switches to Slave Receive mode and stops driving I2Cn_SDA. In this case, the transition from master to Slave mode does not generate a Stop condition. Meanwhile, hardware sets the arbitration lost bit in the I2C Status register (I2C_I2SR[IAL] to indicate loss of arbitration).

36.4.86 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_DI0_PIN03)

Address: 20E_0000h base + 168h offset = 20E_0168h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0											SION	0	MUX_MODE		
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

IOMUXC_SW_MUX_CTL_PAD_DI0_PIN03 field descriptions

Field	Description
31–5 Reserved	This read-only field is reserved and always has the value 0.
4 SION	Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 **ENABLED** — Force input path of pad DI0_PIN3. 0 **DISABLED** — Input Path is determined by functionality of the selected mux mode (regular).
3 Reserved	This read-only field is reserved and always has the value 0.
MUX_MODE	MUX Mode Select Field. Select 1 of 4 iomux modes to be used for pad: DI0_PIN3. 000 **ALT0** — Select signal IPU1_DI0_PIN03. 001 **ALT1** — Select signal IPU2_DI0_PIN03. 010 **ALT2** — Select signal AUD6_TXFS. 101 **ALT5** — Select signal GPIO4_IO19.

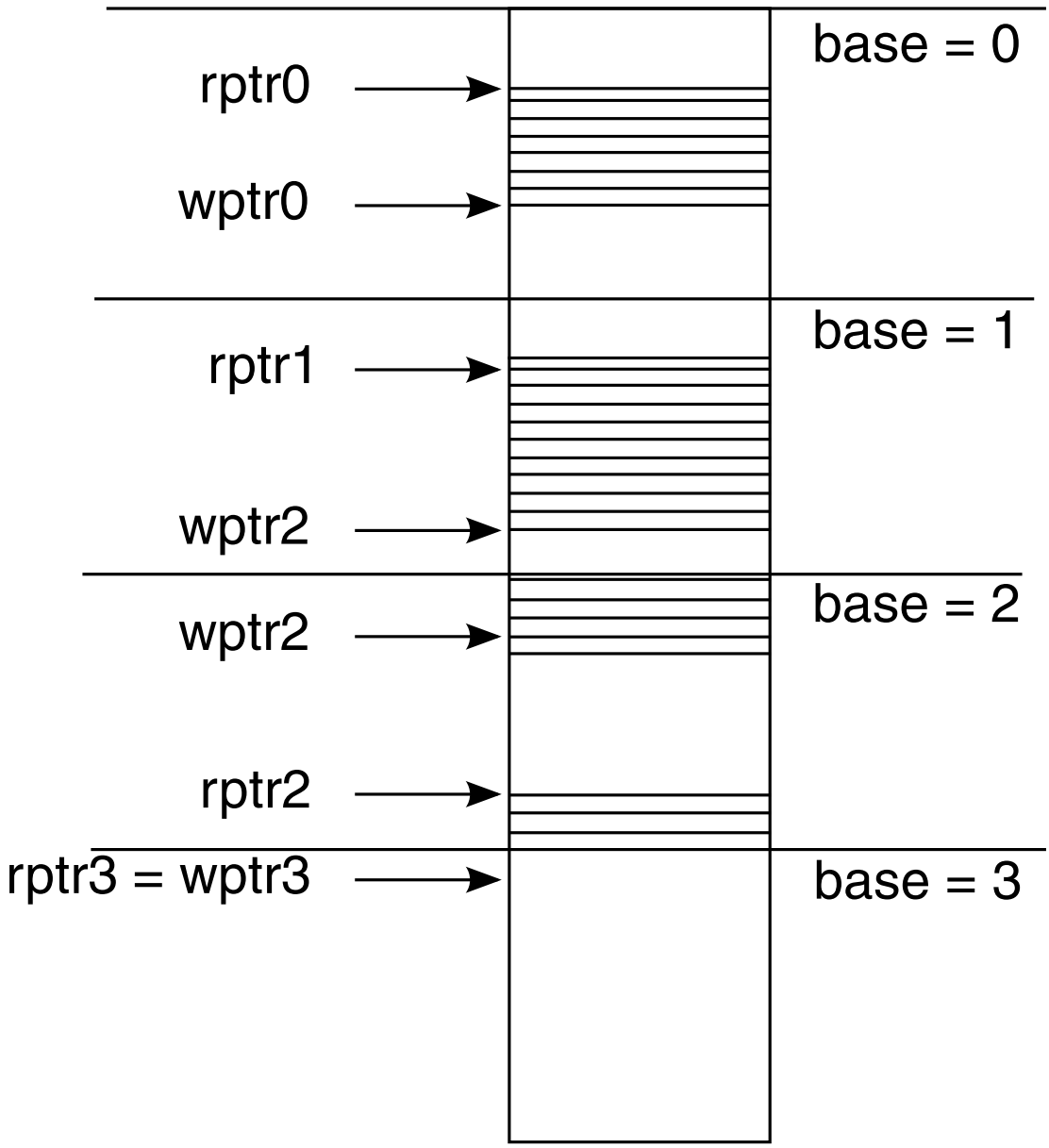


Figure 37-24. SMFC memory map when DMA channels 3,2,1,0 are enabled

37.4.4.2.1 SMFC Master interface.

SMFC Master interface is shown in the following figure.

Table 37-26. DC template's commands description (continued)

Command	COMMAND[41:0]																																														
	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
WROAR	S	1	1	0	0	1	1	1	af	0	0	0	0	0	0	0	0	0	0	0	0	0	MAPPPING					WAVEFORM				GLUELOGIC												SYNC			
	Adding Mapped Address to held data. Write to DI and hold in register af=0: No shift af=1: 8 bit right shift																																														
	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
HLODR	S	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	MAPPPING					0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
	Adding Mapped Data to held data and hold in register.																																														
	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
WRODR	S	1	1	0	0	1	1	0	0	M2	M1	M0	0	0	0	0	0	0	0	0	0	0	MAPPPING					WAVEFORM				GLUELOGIC												SYNC			
	Adding Mapped Data to held data. Write to DI and hold in register. M0: 0: a new data[7:0] before mapping 1: a previous access data [7:0] before mapping M1: 0: a new data[15:8] before mapping 1: a previous access data [15:8] before mapping M2: 0: a new data[31:16] before mapping 1: a previous access data [31:16] before mapping If (M2 = M1 = M0 = 0) than the command performs: Adding a new Mapped Data to a held data in an internal register and write it to display else a display's data will be combined from a new data and previous data according to M-flags. The combined data will be mapped according to MAPPING and sent to a display. Examples: previous_data = 0x89ABCDEF new_data = 0x12345678 held_data (previous_data after mapping) = 0x0000EF Current MAPPING mode: new_data & 0x00ffff00 Output: If M2 = M1 = M0 = 0) than: Output = new_data OR held_data = 0x3456EF If M0 = 0, M1= 1,M2 = 1 than: Output = MAPPING ({previous_data[31:8], new_data[7:0]}) = MAPPING(0x89ABCD78) = 0x00ABCD00)																																														

Table continues on the next page...

IPU memory map

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
260_0000	Configuration Register (IPU1_CONF)	32	R/W	0000_0000h	37.5.1/2915
260_0004	SISG Control 0 Register (IPU1_SISG_CTRL0)	32	R/W	0000_0000h	37.5.2/2918
260_0008	SISG Control 1 Register (IPU1_SISG_CTRL1)	32	R/W	0000_0000h	37.5.3/2919
260_000C	SISG Set<i> Register (IPU1_SISG_SET_i)	32	R/W	0000_0000h	37.5.4/2919
260_0024	SISG Clear <i> Register (IPU1_SISG_CLR_i)	32	R/W	0000_0000h	37.5.5/2920
260_003C	Interrupt Control Register 1 (IPU1_INT_CTRL_1)	32	R/W	0000_0000h	37.5.6/2920
260_0040	Interrupt Control Register 2 (IPU1_INT_CTRL_2)	32	R/W	0000_0000h	37.5.7/2924
260_0044	Interrupt Control Register 3 (IPU1_INT_CTRL_3)	32	R/W	0000_0000h	37.5.8/2927
260_0048	Interrupt Control Register 4 (IPU1_INT_CTRL_4)	32	R/W	0000_0000h	37.5.9/2931
260_004C	Interrupt Control Register 5 (IPU1_INT_CTRL_5)	32	R/W	0000_0000h	37.5.10/ 2934
260_0050	Interrupt Control Register 6 (IPU1_INT_CTRL_6)	32	R/W	0000_0000h	37.5.11/ 2939
260_0054	Interrupt Control Register 7 (IPU1_INT_CTRL_7)	32	R/W	0000_0000h	37.5.12/ 2942
260_0058	Interrupt Control Register 8 (IPU1_INT_CTRL_8)	32	R/W	0000_0000h	37.5.13/ 2944
260_005C	Interrupt Control Register 9 (IPU1_INT_CTRL_9)	32	R/W	0000_0000h	37.5.14/ 2946
260_0060	Interrupt Control Register 10 (IPU1_INT_CTRL_10)	32	R/W	0000_0000h	37.5.15/ 2948
260_0064	Interrupt Control Register 11 (IPU1_INT_CTRL_11)	32	R/W	0000_0000h	37.5.16/ 2950
260_0068	Interrupt Control Register 12 (IPU1_INT_CTRL_12)	32	R/W	0000_0000h	37.5.17/ 2953
260_006C	Interrupt Control Register 13 (IPU1_INT_CTRL_13)	32	R/W	0000_0000h	37.5.18/ 2955
260_0070	Interrupt Control Register 14 (IPU1_INT_CTRL_14)	32	R/W	0000_0000h	37.5.19/ 2959
260_0074	Interrupt Control Register15 (IPU1_INT_CTRL_15)	32	R/W	0000_0000h	37.5.20/ 2962
260_0078	SDMA Event Control Register 1 (IPU1_SDMA_EVENT_1)	32	R/W	0000_0000h	37.5.21/ 2966
260_007C	SDMA Event Control Register 2 (IPU1_SDMA_EVENT_2)	32	R/W	0000_0000h	37.5.22/ 2970
260_0080	SDMA Event Control Register 3 (IPU1_SDMA_EVENT_3)	32	R/W	0000_0000h	37.5.23/ 2973
260_0084	SDMA Event Control Register 4 (IPU1_SDMA_EVENT_4)	32	R/W	0000_0000h	37.5.24/ 2978
260_0088	SDMA Event Control Register 7 (IPU1_SDMA_EVENT_7)	32	R/W	0000_0000h	37.5.25/ 2981
260_008C	SDMA Event Control Register 8 (IPU1_SDMA_EVENT_8)	32	R/W	0000_0000h	37.5.26/ 2983

Table continues on the next page...

IPUx_INT_CTRL_14 field descriptions (continued)

Field	Description
13 IDMAC_TH_EN_45	Threshold crossing indication of Channel interrupt. This bit is the control Threshold crossing interrupt of Channel #n. *n* Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
12 IDMAC_TH_EN_44	Threshold crossing indication of Channel interrupt. This bit is the control Threshold crossing interrupt of Channel #n. *n* Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
11 IDMAC_TH_EN_43	Threshold crossing indication of Channel interrupt. This bit is the control Threshold crossing interrupt of Channel #n. *n* Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
10 IDMAC_TH_EN_42	Threshold crossing indication of Channel interrupt. This bit is the control Threshold crossing interrupt of Channel #n. *n* Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
9 IDMAC_TH_EN_41	Threshold crossing indication of Channel interrupt. This bit is the control Threshold crossing interrupt of Channel #n. *n* Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
8 IDMAC_TH_EN_40	Threshold crossing indication of Channel interrupt. This bit is the control Threshold crossing interrupt of Channel #n. *n* Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
7–2 Reserved	This read-only field is reserved and always has the value 0. 0 Interrupt is disabled. 1 Interrupt is enabled.
1 IDMAC_TH_EN_33	Threshold crossing indication of Channel interrupt. This bit is the control Threshold crossing interrupt of Channel #n. *n* Indicates the corresponding DMA channel number. 0 Interrupt is disabled. 1 Interrupt is enabled.
0 Reserved	This read-only field is reserved and always has the value 0.

Table continues on the next page...

Table 44-1. MMDC feature summary (continued)

Feature	Details

	• Supports buffered/non-buffered accesses (AWCACHE[0] = 0b means a non-bufferable access and AWCACHE[0] = 1b means a bufferable access). The rest of the CACHE options are not supported
	  • To keep data access coherency between write and read access of the same master, the response signal is sent as follows:
	  • Bufferable write access—BRESP will be sent when last data of the access has entered the MMDC.
	  • Non-bufferable write access—BRESP will be sent when the data was physically written into the external memory device.
	• Supports four exclusive monitors per configurable ID for only a single access with a size of up to 64 bits
	• Supports AXI responses as follows:
	  • Okay in case the access has been successful or exclusive access failure
	  • Slave error in case of security violation
	  • Exclusive okay in case the read or the write portion of an exclusive access has been successful

DDR calibration and delay-lines.	• Supports various calibration processes which can be performed either automatically (hardware) or manually (software) towards either CS0 or CS1. (At the end of the process the delay-lines will work with one set of results.) The following calibration processes are supported:
	  • ZQ calibration for external DDR device (in DDR3 through ZQ calibration command and in LPDDR2 through MRW command)
	  • Can be handled automatically for ZQ Short (periodically) and ZQ Long (at exit from self-refresh)
	  • Can be handled manually at ZQ INIT
	  • ZQ calibration for DDR I/O pads for calibrating the DDR driving strength
	  • The sequence can be handled automatically by hardware
	  • The sequence can be handled step by step manually by software
	  • Read data calibration. Adjustment of read DQS with read data byte.
	  • Read DQS gating calibration for DDR3 only. Adjustment of DQS gate with read preamble window.
	  • Write data calibration. Adjustment of write DQS with write data byte.
	  • Write leveling calibration. Adjustment of write DQS with CK (DDR differential clock).
	  • Read fine tuning. Adjustment of up to 7 delay-line units for each read data bit.
	  • Write fine tuning. Adjustment of up to 3 delay-line units for each read data bit.
	  • Periodic delay-line measurement for keeping its accuracy during refresh interval.
	  • Additional fine tuning delay lines to adjust DDR clock delay, DDR clock duty cycle, DQS duty cycle.

Power saving	• Support of dynamic voltage, frequency change and self-refresh mode entry through hardware and software negotiation with the system (request/acknowledge handshake)
	  • Upon hardware or software self-refresh request assertion, further AXI requests are blocked (even before the assertion of the acknowledge).
	  • During self-refresh mode the system may deassert the operating clock of the MMDC for power saving.
	  • During self-refresh mode the clock (CK) that is driven to the DDR device will be gated for power saving.
	• Supports automatic self-refresh and power down entry and exit
	  • In automatic self-refresh, the internal operating clock will be gated for power saving.
	• Supports fast and slow precharge power down in DDR3
	• Automatic active and precharge power down timer per chip select (one chip select can enter power down while the other is still working)

Table continues on the next page...

MMDCx_MPPDCMPR1 field descriptions (continued)

Field	Description
	NOTE: Before issuing the read access, the MMDC will invert the value of this field and drive it to the associated entry in the read comparison FIFO.

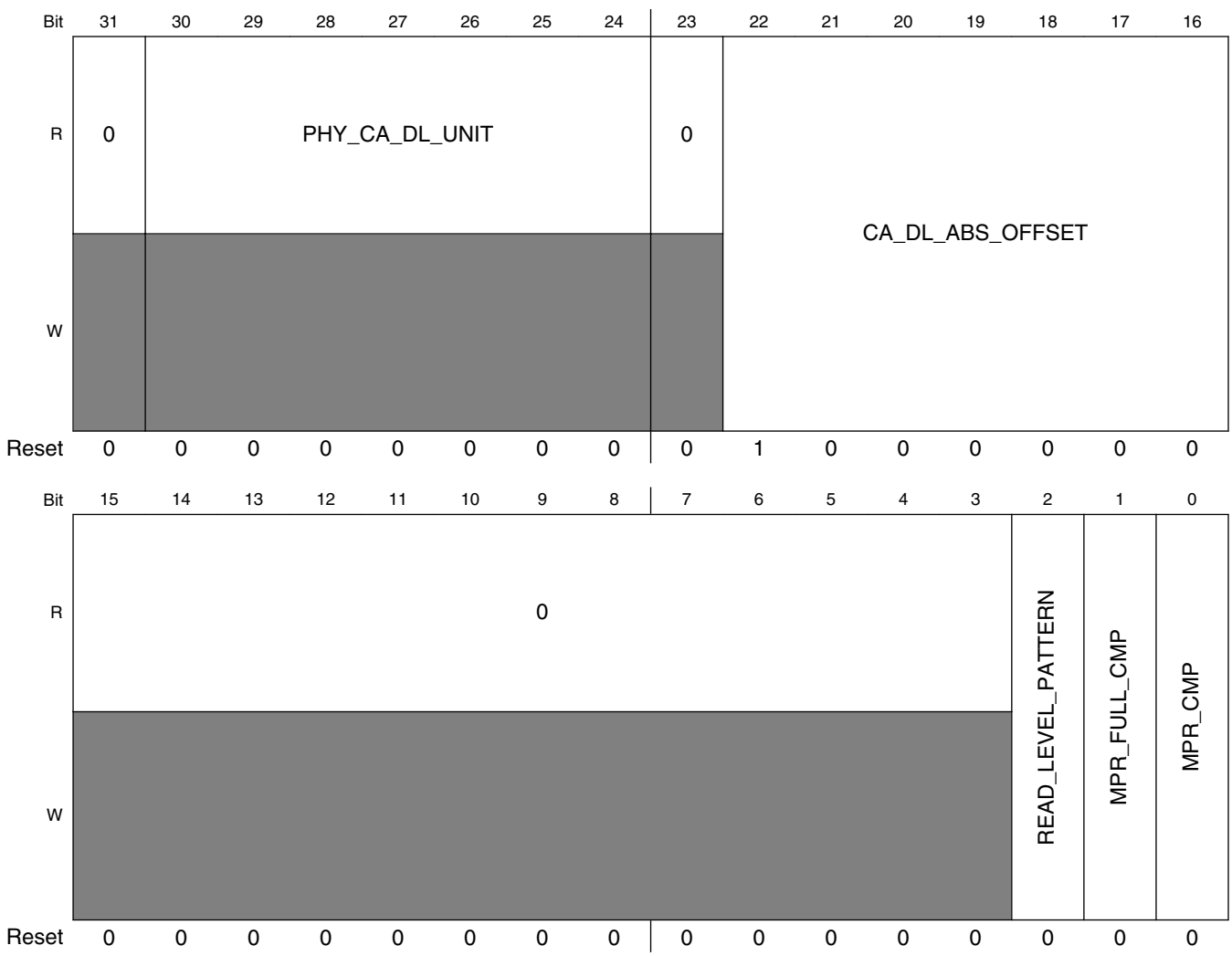
44.12.67 MMDC PHY Pre-defined Compare and CA delay-line Configuration Register (MMDCx_MPPDCMPR2)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2_2ch_x16, LP2_2ch_x32

Address: Base address + 890h offset



- Perform Hardware Reset. The program RAM, context RAM, data RAM and SDMA_CHNENBLn registers have unpredictable contents after this reset.
- Initialize SDMA_CHNENBLn registers to map DMA request events to desired channels.
- Configure SDMA_CHNPRIn registers to select priority for runnable channels. A non-zero priority is required for the channel to run.
- Configure the SDMA_CONFIG register to select DMA to SDMA core clock ratio .
- Set up channel control blocks and buffer descriptors in Arm platform to specify the loading of SDMA program RAM and channel contexts for each SDMA channel to be used. Reference Data Structures for Boot Code and Channel Scripts.
- Configure SDMA_MC0PTR register with base address of Arm platform Channel Control Block base address.
- Initialize SDMA_CHNENBLn registers to map DMA request events to associated channel. Reference Mapping DMA Requests to Pending Channels.
- Configure SDMA_CHNPRIn registers to set priority for each channel to be run.
- For each channel to be run, configure SDMA_HOSTOVR (HO) and SDMA_EVTOVR (EO) registers to select which events (hardware and/or software trigger events) must occur for the channel to be runnable. Reference Runnable Channels Evaluation.
- Set bit 0 of the SDMA_HSTART register to set HE[0] and allow Channel 0 to run (assumes EO[0] andDO[0] were both set in previous step). This will cause SDMA to load the program RAM and channel contexts configured previously.
- Wait for Channel 0 to finish running. This is indicated by HI[0]=1 in the SDMA_SDMA_INTR register, or by optional interrupt to the Arm platform.
- Set the LOCK bit in the SDMA_SDMA_LOCK register to prevent un-authorized uploads of data to SDMA RAM.
- Additional channel scripts can now be run by enabling the selected software or hardware trigger event according to Runnable Channels Evaluation.

55.4.9 SDMA Programming Model

This section describes the programming model for the SDMA RISC engine, including its processor, memory, and internal control registers.

All addresses are related to the internal SDMA memory map, which is completely different from the Arm platform memory maps. The Arm platform processor has no access to any hardware resource described, except when those resources are described in Arm Platform Memory Map and Control Register Summary. .

meaning that the start-split issued by the host controller was not received. This result should be interpreted by system software as if the transaction was completely skipped. The test for whether this is the last complete split can be performed by XORing C-mask with C-prog-mask. A zero result indicates that all complete-splits have been executed.

- MDATA (and Last). See above description for testing for Last. This can only occur when there is an error condition. Either there has been a babble condition on the full-speed link, which delayed the completion of the full-speed transaction, or software set up the *S-mask* and/or *C-mask*s incorrectly. The host controller must set *XactErr* bit to a one and the *Active* bit is set to a zero.
- NYET (and not Last). See above description for testing for Last. The complete-split transaction received a NYET response from the transaction translator. Do not update any transfer state (except for *C-prog-mask*) and stay in this state.
- MDATA (and not Last). The transaction translator responds with an MDATA when it has partial data for the split transaction. For example, the full-speed transaction data payload spans from micro-frame X to X+1 and during micro-frame X, the transaction translator will respond with an MDATA and the data accumulated up to the end of micro-frame X. The host controller advances the transfer state to reflect the number of bytes received.

If Test A succeeds, but Test B fails, it means that one or more of the complete-splits have been skipped. The host controller sets the *Missed Micro-Frame* status bit and sets the *Active* bit to a zero.

65.4.3.12.3.6 Complete-Split for Scheduling Boundary Cases 2a, 2b

Boundary cases 2a and 2b (INs only) (see Figure 65-25) require that the host controller use the transaction state context of the previous siTD to finish the split transaction. The table below enumerates the transaction state fields.

Table 65-50. Summary siTD Split Transaction State

Buffer State	Status	Execution Progress
Total Bytes To Transfer P (page select) Current Offset TP (transaction position) T-count (transaction count)	All bits in the status field	C-prog-mask

NOTE

TP and *T-count* are used only for Host to Device (OUT) endpoints.

USB_*n*ENDPTCTRL1 field descriptions

Field	Description
31–24 -	This field is reserved. Reserved
23 TXE	TX Endpoint Enable 0 Disabled [Default] 1 Enabled An Endpoint should be enabled only after it has been configured.
22 TXR	TX Data Toggle Reset (WS) Write 1 - Reset PID Sequence Whenever a configuration event is received for this Endpoint, software must write a one to this bit in order to synchronize the data PID's between the Host and device.
21 TXI	TX Data Toggle Inhibit 0 PID Sequencing Enabled. [Default] 1 PID Sequencing Disabled. This bit is only used for test and should always be written as zero. Writing a one to this bit causes this endpoint to ignore the data toggle sequence and always transmit DATA0 for a data packet.
20 -	This field is reserved. Reserved
19–18 TXT	TX Endpoint Type - Read/Write 00 Control 01 Isochronous 10 Bulk 11 Interrupt
17 TXD	TX Endpoint Data Source - Read/Write 0 Dual Port Memory Buffer/DMA Engine [DEFAULT] Should always be written as 0.
16 TXS	TX Endpoint Stall - Read/Write 0 End Point OK 1 End Point Stalled This bit will be cleared automatically upon receipt of a SETUP request if this Endpoint is configured as a Control Endpoint and this bit will continue to be cleared by hardware until the associated ENDPTSETUPSTAT bit is cleared. Software can write a one to this bit to force the endpoint to return a STALL handshake to the Host. This control will continue to STALL until this bit is either cleared by software or automatically cleared as above for control endpoints. **NOTE:** [CONTROL ENDPOINT TYPES ONLY]: there is a slight delay (50 clocks max) between the ENDPTSETUPSTAT begin cleared and hardware continuing to clear this bit. In most systems, it is unlikely the DCD software will observe this delay. However, should the DCD observe that the stall bit is not set after writing a one to it then follow this procedure: continually write this stall bit until it is set or until a new setup has been received by checking the associated endptsetupstat bit.
15–8 -	This field is reserved. Reserved

Table continues on the next page...

uSDHCx_INT_STATUS field descriptions (continued)

Field	Description
	Occurs when detecting a CRC error when transferring read data, which uses the DATA line, or when detecting the Write CRC status having a value other than 010. 1 Error 0 No Error
20 DTOE	Data Timeout Error Occurs when detecting one of following time-out conditions. • Busy time-out for R1b, R5b type • Busy time-out after Write CRC status • Read Data time-out. 1 Time out 0 No Error
19 CIE	Command Index Error Occurs if a Command Index error occurs in the command response. 1 Error 0 No Error
18 CEBE	Command End Bit Error Occurs when detecting that the end bit of a command response is 0. 1 End Bit Error Generated 0 No Error
17 CCE	Command CRC Error Command CRC Error is generated in two cases. • If a response is returned and the Command Timeout Error is set to 0 (indicating no time-out), this bit is set when detecting a CRC error in the command response. • The uSDHC detects a CMD line conflict by monitoring the CMD line when a command is issued. If the uSDHC drives the CMD line to 1, but detects 0 on the CMD line at the next SDCLK edge, then the uSDHC shall abort the command (Stop driving CMD line) and set this bit to 1. The Command Timeout Error shall also be set to 1 to distinguish CMD line conflict. 1 CRC Error Generated. 0 No Error
16 CTOE	Command Timeout Error Occurs only if no response is returned within 64 SDCLK cycles from the end bit of the command. If the uSDHC detects a CMD line conflict, in which case a Command CRC Error shall also be set (as shown in Interrupt Status (uSDHC_INT_STATUS)), this bit shall be set without waiting for 64 SDCLK cycles. This is because the command will be aborted by the uSDHC. 1 Time out 0 No Error
15 Reserved	This read-only field is reserved and always has the value 0.
14 TP	Tuning Pass:(only for SD3.0 SDR104 mode) Current CMD19 transfer is done successfully. That is, current sampling point is correct.

Table continues on the next page...