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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-FBGA, FCBGA
Supplier Device Package	624-FCBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6d7cvt08ae

Table 4-1. Pin Assignments (continued)

Pad Name	Mode	Signal	Pad Settings	Pad/Group Registers
			SRE - SLOW	
CSI_CLK0M		CSI_CLK0_N		
CSI_CLK0P		CSI_CLK0_P		
CSI_D0M		CSI_DATA0_N		
CSI_D0P		CSI_DATA0_P		
CSI_D1M		CSI_DATA1_N		
CSI_D1P		CSI_DATA1_P		
CSI_D2M		CSI_DATA2_N		
CSI_D2P		CSI_DATA2_P		
CSI_D3M		CSI_DATA3_N		
CSI_D3P		CSI_DATA3_P		
DI0_DISP_CLK	ALT0	IPU1_DI0_DISP_CLK	HYS - ENABLED PUS - 100K_OHM_PU PUE - PULL PKE - ENABLED ODE - DISABLED SPEED - MEDIUM DSE - 40_OHM SRE - SLOW	SW_PAD_CTL_PAD_DI0_DISP_CLK
	ALT1	IPU2_DI0_DISP_CLK		
	ALT5	GPIO4_IO16		
DI0_PIN2	ALT0	IPU1_DI0_PIN02	HYS - ENABLED PUS - 100K_OHM_PU PUE - PULL PKE - ENABLED ODE - DISABLED SPEED - MEDIUM DSE - 40_OHM SRE - SLOW	SW_PAD_CTL_PAD_DI0_PIN02
	ALT1	IPU2_DI0_PIN02		
	ALT2	AUD6_TXD		
	ALT5	GPIO4_IO18		
DI0_PIN3	ALT0	IPU1_DI0_PIN03	HYS - ENABLED PUS - 100K_OHM_PU PUE - PULL PKE - ENABLED ODE - DISABLED SPEED - MEDIUM DSE - 40_OHM SRE - SLOW	SW_PAD_CTL_PAD_DI0_PIN03
	ALT1	IPU2_DI0_PIN03		
	ALT2	AUD6_TXFS		
	ALT5	GPIO4_IO19		
DI0_PIN4	ALT0	IPU1_DI0_PIN04	HYS - ENABLED PUS - 100K_OHM_PU PUE - PULL	SW_PAD_CTL_PAD_DI0_PIN04
	ALT1	IPU2_DI0_PIN04		
	ALT2	AUD6_RXD		

Table continues on the next page...

Table 8-24. ECSPI IOMUX pin configuration (continued)

RDY	N/A[1]	N/A	N/A	N/A	N/A
SCLK	EIM_D16.alt1	CSI0_DAT8.alt2	DISP0_DAT0.alt2	EIM_D21.alt1	SD1_CLK.alt1
SS0	EIM_EB2.alt1	CSI0_DAT11.alt2	DISP0_DAT3.alt2	EIM_D20.alt1	SD1_DAT1.alt1
SS1	EIM_D19.alt1	EIM_LBA.alt1	DISP0_DAT4.alt2	EIM_A25.alt1	SD1_DAT2.alt1
SS2	EIM_D24.alt1	EIM_D24.alt4	DISP0_DAT5.alt2	EIM_D24.alt1	SD1_DAT3.alt1
SS3	EIM_D25.alt1	EIM_D25.alt4	DISP0_DAT6.alt2	EIM_D25.alt1	SD2_DAT3.alt1

1. The N/A in the ROM code indicates that the pins are not available or not used.

8.6 Program image

This section describes the data structures that are required to be included in the user's program image. The program image consists of:

- Image vector table—a list of pointers located at a fixed address that the ROM examines to determine where the other components of the program image are located.
- Boot data—a table that indicates the program image location, program image size in bytes, and the plugin flag.
- Device configuration data—IC configuration data.
- User code and data.

8.6.1 Image Vector Table and Boot Data

The Image Vector Table (IVT) is the data structure that the ROM reads from the boot device supplying the program image containing the required data components to perform a successful boot.

The IVT includes the program image entry point, a pointer to Device Configuration Data (DCD) and other pointers used by the ROM during the boot process.The ROM locates the IVT at a fixed address that is determined by the boot device connected to the Chip. The IVT offset from the base address and initial load region size for each boot device

HDMI_FC_DATMAN field descriptions (continued)

Field	Description
4 spd_tx	SPD packet
3 vsd_tx	VSD packet
2 iscr2_tx	ISRC2 packet
1 isr1_tx	ISRC1 packet
0 acp_tx	ACP packet

33.5.132 Frame Composer Data Island Auto Packet Scheduling Register 3 (HDMI_FC_DATAUTO3)

Configures the Frame Composer Automatic(1)/RDRB(0) data island packet insertion for AVI, GCP, AUDI and ACR packets. In Automatic mode, the packet will be inserted on Vblanking when first line with active Vsync appears.

- Address Offset: 0x10B7
- Size: 8 bits
- Value after Reset: 0x0F
- Access: Read/Write

Address: 12_0000h base + 10B7h offset = 12_10B7h

Bit	7	6	5	4	3	2	1	0
Read Write	Reserved				avi_auto	gcp_auto	audi_auto	acr_auto
Reset	0	0	0	0	1	1	1	1

HDMI_FC_DATAUTO3 field descriptions

Field	Description
7–4 -	This field is reserved. Reserved
3 avi_auto	Enable AVI packet insertion
2 gcp_auto	Enable GCP packet insertion
1 audi_auto	Enable AUDI packet insertion
0 acr_auto	Enable ACR packet insertion

36.4.9 GPR (IOMUXC_GPR8)

Address: 20E_0000h base + 20h offset = 20E_0020h

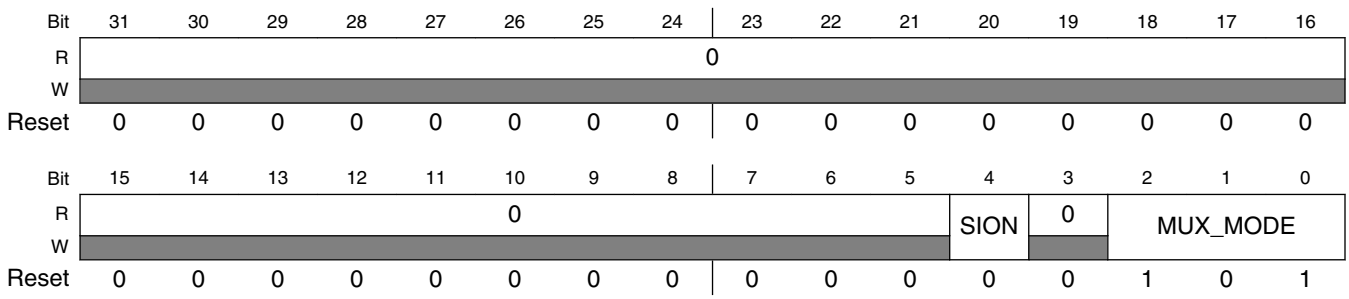
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	PCS_TX_SWING_LOW							PCS_TX_SWING_FULL							PCS_TX_DEEMPH_ GEN2_6DB						PCS_TX_DEEMPH_ GEN2_3P5DB						PCS_TX_DEEMPH_ GEN1							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IOMUXC_GPR8 field descriptions

Field	Description
31–25 PCS_TX_ SWING_LOW	PCIe_PHY - This static value sets the launch amplitude of the transmitter when pipe0_tx_swing is set to 1'b0 (default state). 7'hxx - TX launch amplitude swing_low value.
24–18 PCS_TX_ SWING_FULL	PCIe_PHY - This static value sets the Tx driver SWING_FULL value. 7'hxx - Gen2 TX SWING FULL value.
17–12 PCS_TX_ DEEMPH_ GEN2_6DB	PCIe_PHY - This static value sets the Tx driver de-emphasis value in the case where pipe0_tx_deemph is set to 1'b0 and the PHY is running at the Gen2 (6db) rate. 6'hxx - Gen2 (6db) De-emphasis value.
11–6 PCS_TX_ DEEMPH_ GEN2_3P5DB	PCIe_PHY - This static value sets the Tx driver de-emphasis value in the case where pipe0_tx_deemph is set to 1'b1 (the default setting) and the PHY is running at the Gen2 (3p5db) rate. 6'hxx - Gen2 De-emphasis value.
PCS_TX_ DEEMPH_GEN1	PCIe_PHY - This static value sets the Tx driver de-emphasis value in the case where pipe0_tx_deemph is set to 1'b1 (the default setting) and the PHY is running at the Gen1 rate. 6'hxx - Gen1 De-emphasis value.

36.4.31 Pad Mux Register (IOMUXC_SW_MUX_CTL_PAD_EIM_EB2_B)

Address: 20E_0000h base + 8Ch offset = 20E_008Ch



IOMUXC_SW_MUX_CTL_PAD_EIM_EB2_B field descriptions

Field	Description
31–5 Reserved	This read-only field is reserved and always has the value 0.
4 SION	Software Input On Field. Force the selected mux mode input path no matter of MUX_MODE functionality. 1 **ENABLED** — Force input path of pad EIM_EB2. 0 **DISABLED** — Input Path is determined by functionality of the selected mux mode (regular).
3 Reserved	This read-only field is reserved and always has the value 0.
MUX_MODE	MUX Mode Select Field. Select 1 of 7 iomux modes to be used for pad: EIM_EB2. NOTE: Pad EIM_EB2 is involved in Daisy Chain. 000 **ALT0** — Select signal EIM_EB2_B. 001 **ALT1** — Select signal ECSPI1_SS0. - Configure register IOMUXC_ECSPI1_SS0_SELECT_INPUT for mode ALT1. 011 **ALT3** — Select signal IPU2_CSI1_DATA19. - Configure register IOMUXC_IPU2_SENS1_DATA19_SELECT_INPUT for mode ALT3. 100 **ALT4** — Select signal HDMI_TX_DDC_SCL. - Configure register IOMUXC_HDMI_II2C_CLKIN_SELECT_INPUT for mode ALT4. 101 **ALT5** — Select signal GPIO2_IO30. 110 **ALT6** — Select signal I2C2_SCL. - Configure register IOMUXC_I2C2_SCL_IN_SELECT_INPUT for mode ALT6. 111 **ALT7** — Select signal SRC_BOOT_CFG30.

IOMUXC_SW_PAD_CTL_PAD_DI0_PIN02 field descriptions

Field	Description
31–17 Reserved	This read-only field is reserved and always has the value 0.
16 HYS	Hysteresis Enable Field Select one of next values for pad: DI0_PIN2. 0 **DISABLED** — CMOS input 1 **ENABLED** — Schmitt trigger input
15–14 PUS	Pull Up / Down Config. Field Select one of next values for pad: DI0_PIN2. 00 **100K_OHM_PD** — 100K Ohm Pull Down 01 **47K_OHM_PU** — 47K Ohm Pull Up 10 **100K_OHM_PU** — 100K Ohm Pull Up 11 **22K_OHM_PU** — 22K Ohm Pull Up
13 PUE	Pull / Keep Select Field Select one of next values for pad: DI0_PIN2. 0 **KEEP** — Keeper Enabled 1 **PULL** — Pull Enabled
12 PKE	Pull / Keep Enable Field Select one of next values for pad: DI0_PIN2. 0 **DISABLED** — Pull/Keeper Disabled 1 **ENABLED** — Pull/Keeper Enabled
11 ODE	Open Drain Enable Field Enables open drain of the pin. 0 **DISABLED** — Output is CMOS. 1 **ENABLED** — Output is Open Drain.
10–8 Reserved	This read-only field is reserved and always has the value 0.
7–6 SPEED	Speed Field Select one of next values for pad: DI0_PIN2. 00 **LOW** — 50 MHz (SRE=x) 01 **MEDIUM** — 100 MHz, if SRE=1: 100MHz @ 1.8V, 150MHz @ 3.3V 10 **MEDIUM** — 100 MHz, if SRE=1: 100MHz @ 1.8V, 150MHz @ 3.3V 11 **MAXIMUM** — 100 MHz, if SRE=1: 150MHz @ 1.8V, 200MHz @ 3.3V
5–3 DSE	Drive Strength Field Select one of next values for pad: DI0_PIN2. 000 **HIZ** — HI-Z 001 **260_OHM** — 150 Ohm @ 3.3V, 260 Ohm @ 1.8V 010 **130_OHM** — 75 Ohm @ 3.3V, 130 Ohm @ 1.8V 011 **90_OHM** — 50 Ohm @ 3.3V, 90 Ohm @ 1.8V

Table continues on the next page...

Table 37-15. Channel Parameters Memory for interleaved (continued)

				3'h3 = 16 Bits per pixel 3'h4 = 12 Bits per pixel 3'h5 = 08 Bits per pixel 3'h6 = 04 Bits per pixel
Decode Address Select	DEC_SEL	2 bits	W0[111:110]	Upon 4BPP, selects between two look-up tables DEC_SEL 00 = addresses 0 to 15 01 = addresses 64 to 79 10 = addresses 128 to 143 11 = addresses 192 to 207
Access Dimension	DIM	1 bit	W0[112]	DIM = 0 Access Dimension is 2d DIM = 1 Access Dimension is 1d
Scan Order	SO	1 bit	W0[113]	SO = 0 Scan order is progressive SO = 1 Scan order is interlaced
Band Mode	BNDM	3 bits	W0[116:114]	BNDM = 000 bands disable. BNDM = 001 bands enable. Band height = 4 lines. BNDM = 010 bands enable. Band height = 8 lines. BNDM = 011 bands enable. Band height = 16 lines. BNDM = 100 bands enable. Band height = 32 lines. BNDM = 101 bands enable. Band height = 64 lines. BNDM = 110 bands enable. Band height = 128 lines. BNDM = 111 bands enable. Band height = 256 When working in band mode, the channel's corresponding IDMAC_BNDM_EN bit has to be set.
Block Mode	BM	2 bits	W0[118:117]	BM = 00 block mode disable. BW = FW, BH = FH BM = 01 block mode enable. BW = 8, BH = 8 BM = 10 block mode enable. BW = 16, BH = 16 (this mode is reserved for future use) BM = 11 not used
Rotation	ROT	1 bit	W0[119]	ROT = 0 -> No rotation ROT = 1 -> 90 degree rotation clockwise

Table continues on the next page...

IPU memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
265_8154	DC Mapping Configuration Register 19 (IPU1_DC_MAP_CONF_19)	32	R/W	0000_0000h	37.5.353/ 3436
265_8158	DC Mapping Configuration Register 20 (IPU1_DC_MAP_CONF_20)	32	R/W	0000_0000h	37.5.354/ 3437
265_815C	DC Mapping Configuration Register 21 (IPU1_DC_MAP_CONF_21)	32	R/W	0000_0000h	37.5.355/ 3438
265_8160	DC Mapping Configuration Register 22 (IPU1_DC_MAP_CONF_22)	32	R/W	0000_0000h	37.5.356/ 3438
265_8164	DC Mapping Configuration Register 23 (IPU1_DC_MAP_CONF_23)	32	R/W	0000_0000h	37.5.357/ 3439
265_8168	DC Mapping Configuration Register 24 (IPU1_DC_MAP_CONF_24)	32	R/W	0000_0000h	37.5.358/ 3440
265_816C	DC Mapping Configuration Register 25 (IPU1_DC_MAP_CONF_25)	32	R/W	0000_0000h	37.5.359/ 3440
265_8170	DC Mapping Configuration Register 26 (IPU1_DC_MAP_CONF_26)	32	R/W	0000_0000h	37.5.360/ 3441
265_8174	DC User General Data Event 0 Register 0 (IPU1_DC_UGDE0_0)	32	R/W	0000_0000h	37.5.361/ 3442
265_8178	DC User General Data Event 0 Register 1 (IPU1_DC_UGDE0_1)	32	R/W	0000_0000h	37.5.362/ 3443
265_817C	DC User General Data Event 0 Register2 (IPU1_DC_UGDE0_2)	32	R/W	0000_0000h	37.5.363/ 3444
265_8180	DC User General Data Event 0 Register 3 (IPU1_DC_UGDE0_3)	32	R/W	0000_0000h	37.5.364/ 3444
265_8184	DC User General Data Event 1Register0 (IPU1_DC_UGDE1_0)	32	R/W	0000_0000h	37.5.365/ 3445
265_8188	DC User General Data Event 1 Register 1 (IPU1_DC_UGDE1_1)	32	R/W	0000_0000h	37.5.366/ 3446
265_818C	DC User General Data Event 1Register 2 (IPU1_DC_UGDE1_2)	32	R/W	0000_0000h	37.5.367/ 3447
265_8190	DC User General Data Event 1Register 3 (IPU1_DC_UGDE1_3)	32	R/W	0000_0000h	37.5.368/ 3447
265_8194	DC User General Data Event 2 Register 0 (IPU1_DC_UGDE2_0)	32	R/W	0000_0000h	37.5.369/ 3448
265_8198	DC User General Data Event 2 Register 1 (IPU1_DC_UGDE2_1)	32	R/W	0000_0000h	37.5.370/ 3449
265_819C	DC User General Data Event 2Register 2 (IPU1_DC_UGDE2_2)	32	R/W	0000_0000h	37.5.371/ 3450
265_81A0	DC User General Data Event 2Register 3 (IPU1_DC_UGDE2_3)	32	R/W	0000_0000h	37.5.372/ 3450
265_81A4	DC User General Data Event 3Register 0 (IPU1_DC_UGDE3_0)	32	R/W	0000_0000h	37.5.373/ 3451
265_81A8	DC User General Data Event 3Register 1 (IPU1_DC_UGDE3_1)	32	R/W	0000_0000h	37.5.374/ 3452

Table continues on the next page...

IPUx_INT_CTRL_10 field descriptions (continued)

Field	Description
	0 Interrupt is disabled. 1 Interrupt is enabled.
16 DC_TEARING_ERR_1_EN	Tearing Error #1 enable This bit enables the interrupt that is a result of tearing error while the anti tearing mechanism is activated for DC channel 1 0 Interrupt is disabled. 1 Interrupt is enabled.
15–4 Reserved	This read-only field is reserved and always has the value 0.
3 SMFC3_FRM_LOST_EN	Frame Lost of SMFC channel 3 interrupt enable bit This bit enables an interrupt that is a result of a Frame Lost of SMFC channel 3. 0 Interrupt is disabled. 1 Interrupt is enabled.
2 SMFC2_FRM_LOST_EN	Frame Lost of SMFC channel 2 interrupt enable bit This bit enables an interrupt that is a result of a Frame Lost of SMFC channel 2. 0 Interrupt is disabled. 1 Interrupt is enabled.
1 SMFC1_FRM_LOST_EN	Frame Lost of SMFC channel 1 interrupt enable bit This bit enables an interrupt that is a result of a Frame Lost of SMFC channel 1. 0 Interrupt is disabled. 1 Interrupt is enabled.
0 SMFC0_FRM_LOST_EN	Frame Lost of SMFC channel 0 interrupt enable bit This bit enables an interrupt that is a result of a Frame Lost of SMFC channel 0. 0 Interrupt is disabled. 1 Interrupt is enabled.

37.5.16 Interrupt Control Register 11 (IPUx_INT_CTRL_11)

This register contains part of IPU interrupts controls. The controls of the end-of-band indication (EOBND) of DMA Channels interrupts [31:0] can be found in this register.

- Hide VDOA_SYNC for all versions
- Show VDOA_SYNC for IPUv3H version.
- The table below tagged with other settings (like IPU3M_only) should be hidden in IPUv3H version.

37.5.341 DC Mapping Configuration Register 7 (IPUx_DC_MAP_CONF_7)

Address: Base address + 5_8124h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	0	MAPPING_PNTR_BYTE2_15							MAPPING_PNTR_BYTE1_15			MAPPING_PNTR_BYTE0_15				
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	MAPPING_PNTR_BYTE2_14							MAPPING_PNTR_BYTE1_14			MAPPING_PNTR_BYTE0_14				
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IPUx_DC_MAP_CONF_7 field descriptions

Field	Description
31 Reserved	This read-only field is reserved and always has the value 0.
30–26 MAPPING_ PNTR_BYTE2_ 15	Mapping pointer #15 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
25–21 MAPPING_ PNTR_BYTE1_ 15	Mapping pointer #15 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
20–16 MAPPING_ PNTR_BYTE0_ 15	Mapping pointer #15 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0
15 Reserved	This read-only field is reserved and always has the value 0.
14–10 MAPPING_ PNTR_BYTE2_ 14	Mapping pointer #14 for Byte 2 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #2
9–5 MAPPING_ PNTR_BYTE1_ 14	Mapping pointer #14 for Byte 1 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #1
MAPPING_ PNTR_BYTE0_ 14	Mapping pointer #14 for Byte 0 This field is a pointer to the set of MD_OFFSET_<i> and MD_MASK_<i> used for mapping byte #0

MIPI_HSI_AHB_MASTER_CONF field descriptions (continued)

Field	Description
DMA_INSERT_IDLE_NUM	These bits used to set the number of "IDLE" cycles when DMA_MODE == 2'b0x.

42.5.42 TX Break Length Register (MIPI_HSI_TX_BREAK_LEN)

This register used to set tx break length

Address: 220_8000h base + 22Ch offset = 220_822Ch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	Reserved																										COUNT					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1

MIPI_HSI_TX_BREAK_LEN field descriptions

Field	Description
31–6 Reserved	This field is reserved. Reserved, always set to zero.
COUNT	The tx break length count. 6'h00 64 6'h01 1 6'h3f 63

Address: Base address + 430h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	SBS_ADDR																															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MMDCx_MASBS0 field descriptions

Field	Description
SBS_ADDR	Step By Step Address. These bits reflect the address of the pending request in case of step by step mode.

44.12.29 MMDC Core Step By Step Address Attributes Register (MMDCx_MASBS1)

Supported Mode Of Operations:

For Channel 0: All

For Channel 1: LP2_2ch_x16, LP2_2ch_x32

Address: Base address + 434h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	SBS_AXI_ID															
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	SBS_LEN			SBS_BUFF	SBS_BURST		SBS_SIZE		SBS_PROT		SBS_LOCK		SBS_TYPE		SBS_VLD	
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MMDCx_MASBS1 field descriptions

Field	Description
31–16 SBS_AXI_ID	Step By Step AXI ID. These bits reflect the AXI ID of the pending request in case of step by step mode.
15–13 SBS_LEN	Step By Step Length. These bits reflect the AXI LENGTH of the pending request in case of step by step mode. 000 burst of length 1 001 burst of length 2 111 burst of length 8
12 SBS_BUFF	Step By Step Buffered. This bit reflect the AXI CACHE[0] of the pending request in case of step by step mode. Relevant only for write requests

Table continues on the next page...

48.12.29 VCn Non-Posted Buffer Depth (PCIE_PL_VC*n*NPBD)

Offset: 0x700 + 0xAC + C*n (n=[1:7])

Address: 1FF_C000h base + 7B8h offset + (12d × i), where i=0d to 6d

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R	Reserved						VCn_Non_Posted_Header_Queue_Depth									
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	Reserved		VCn_Non_Posted_Data_Queue_Depth													
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PCIE_PL_VC*n*NPBD field descriptions

Field	Description
31–26 -	This field is reserved. Reserved
25–16 VCn_Non_Posted_Header_Queue_Depth	VCn Non-Posted Header Queue Depth Sets the number of entries in the Non-Posted header queue for VCn when using the segmented-buffer configuration. Not writable through the DBI
15–14 -	This field is reserved. Reserved
VCn_Non_Posted_Data_Queue_Depth	VCn Non-Posted Data Queue Depth Sets the number of entries in the Non-Posted data queue for VCn when using the segmented-buffer configuration. Not writable through the DBI

51.7.6 PWM Counter Register (PWMx_PWMCNR)

The read-only pulse-width modulator counter register (PWM_PWMCNR) contains the current count value and can be read at any time without disturbing the counter.

Address: Base address + 14h offset

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0																COUNT															
W																																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PWMx_PWMCNR field descriptions

Field	Description
31–16 Reserved	This field is reserved. This read-only field is reserved and always has the value 0.
COUNT	Counter Value. These bits are the counter register value and denotes the current count state the counter register is in.

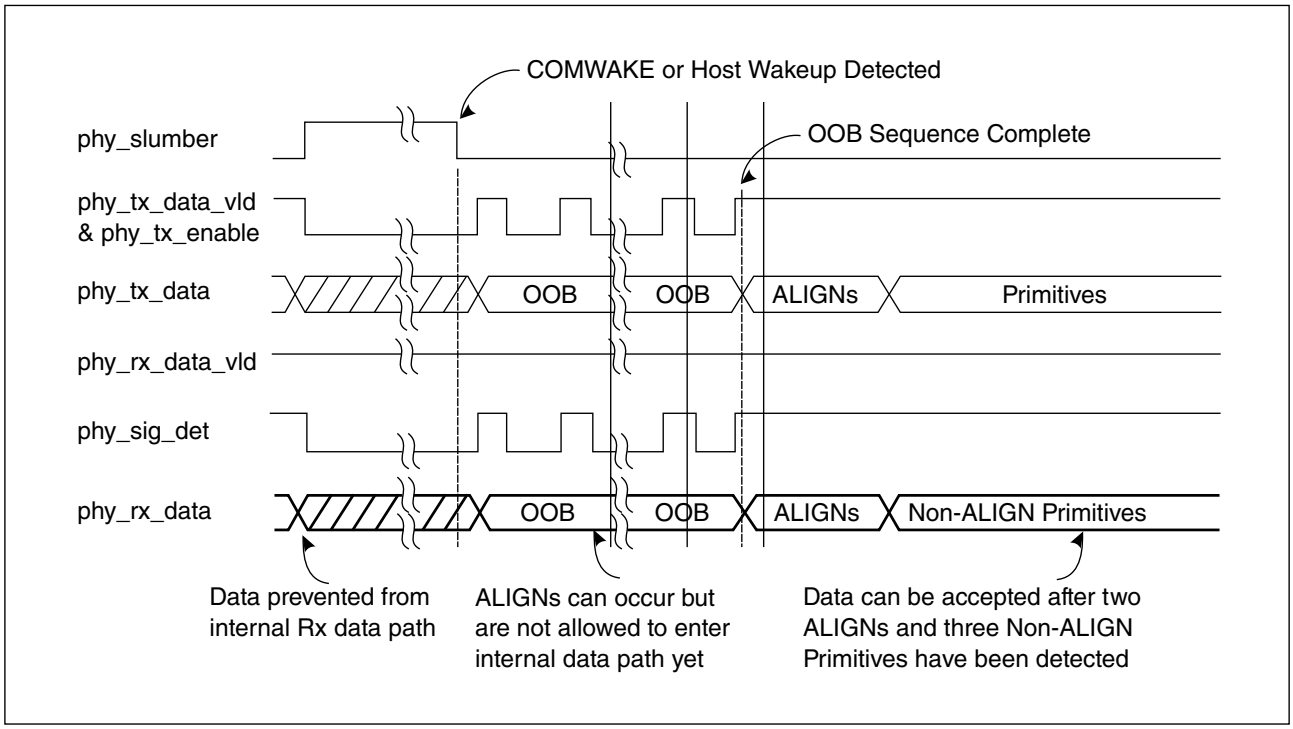


Figure 53-15. Power Mode Example: Rx and Tx In Link

53.3.4.6 Port Power Control Module

The Port Power Control Module (PCM) implements the following functions:

- Monitors Transport, Link and PHY ready/not ready conditions, as well as Device and Host power requests.
- Systematically controls the Link and Transport Layer transitions into and out of offline conditions (system reset, COMRESET and power modes).
- Allows clk_asic0 and clk_rbc0 to be stopped during Slumber and Partial power modes.

The PCM main function is to allow disabling clk_asic0 and clk_rbc0 in SATA power down modes.

CAUTION

Clocks supplied to the core should never glitch at any time, including before, during, and after initialization and power modes. Clock glitch protection should be performed outside the core for any clocks that might glitch.

000 - GReg[0]

001 - GReg[1]

010 - GReg[2]

011 - GReg[3]

100 - GReg[4]

101 - GReg[5]

110 - GReg[6]

111 - GReg[7]

55.5.2.51 XORI (Exclusive OR with Immediate)

Operation:

GReg[r] ← GReg[r] ^ immediate

Assembler:

Syntax: xori r,immediate

Example: xor 7,5

XORs GReg[5] and decimal value 5 and stores the result in GReg[7]

CPU Flags: Unaffected

Cycles: 1

Description: Performs an eXclusive OR between a 0-extended 8-bit immediate value and a General Register; stores the result in the General Register. The immediate value is the low-order byte of the instruction and has a maximum value of 255 (0xFF).

Instruction Format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	r	r	r	i	i	i	i	i	i	i	i

Instruction Fields:

rrr - register field:

000 - GReg[0]

001 - GReg[1]

010 - GReg[2]

011 - GReg[3]

64.4.3.9 Programmable CTS_B Deassertion

The CTS_B output can also be programmed to deassert when the RxFIFO reaches a certain level. Setting the CTS trigger level (UCR4[15:10]) at any value less than 32 deasserts the CTS_B pin on detection of the valid start bit of the N + 1 character (where N is the trigger level setting). However, the receiver continues to receive characters until the RxFIFO is full.

64.4.3.10 TX_DATA - UART Transmit

This is the transmitter serial output. When operating in RS-232/RS-485 mode, NRZ encoded data is transmitted, and the data can be inverted (controlled by INVT (UCR3[1])) before transmitted. When operating in infrared mode, a 3/16 bit-period pulse is output for each 0 bit transmitted, and no pulse is output for each 1 bit transmitted.

For RS-232/RS-485 applications, this pin must be connected to an RS-232/RS-485 transmitter. The operation of this output is the same regardless of whether the UART is in DTE or DCE mode. See Figure 64-3.

UART memory map (continued)

Absolute address (hex)	Register name	Width (in bits)	Access	Reset value	Section/ page
21F_0000	UART Receiver Register (UART4_URXD)	32	R	0000_0000h	64.15.1/ 5211
21F_0040	UART Transmitter Register (UART4_UTXD)	32	W	0000_0000h	64.15.2/ 5213
21F_0080	UART Control Register 1 (UART4_UCR1)	32	R/W	0000_0000h	64.15.3/ 5214
21F_0084	UART Control Register 2 (UART4_UCR2)	32	R/W	0000_0001h	64.15.4/ 5216
21F_0088	UART Control Register 3 (UART4_UCR3)	32	R/W	0000_0700h	64.15.5/ 5219
21F_008C	UART Control Register 4 (UART4_UCR4)	32	R/W	0000_8000h	64.15.6/ 5221
21F_0090	UART FIFO Control Register (UART4_UFCR)	32	R/W	0000_0801h	64.15.7/ 5223
21F_0094	UART Status Register 1 (UART4_USR1)	32	R/W	0000_2040h	64.15.8/ 5225
21F_0098	UART Status Register 2 (UART4_USR2)	32	R/W	0000_4028h	64.15.9/ 5228
21F_009C	UART Escape Character Register (UART4_UESC)	32	R/W	0000_002Bh	64.15.10/ 5230
21F_00A0	UART Escape Timer Register (UART4_UTIM)	32	R/W	0000_0000h	64.15.11/ 5231
21F_00A4	UART BRM Incremental Register (UART4_UBIR)	32	R/W	0000_0000h	64.15.12/ 5231
21F_00A8	UART BRM Modulator Register (UART4_UBMR)	32	R/W	0000_0000h	64.15.13/ 5232
21F_00AC	UART Baud Rate Count Register (UART4_UBRC)	32	R	0000_0004h	64.15.14/ 5232
21F_00B0	UART One Millisecond Register (UART4_ONEMS)	32	R/W	0000_0000h	64.15.15/ 5233
21F_00B4	UART Test Register (UART4_UTS)	32	R/W	0000_0060h	64.15.16/ 5234
21F_00B8	UART RS-485 Mode Control Register (UART4_UMCR)	32	R/W	0000_0000h	64.15.17/ 5235
21F_4000	UART Receiver Register (UART5_URXD)	32	R	0000_0000h	64.15.1/ 5211
21F_4040	UART Transmitter Register (UART5_UTXD)	32	W	0000_0000h	64.15.2/ 5213
21F_4080	UART Control Register 1 (UART5_UCR1)	32	R/W	0000_0000h	64.15.3/ 5214
21F_4084	UART Control Register 2 (UART5_UCR2)	32	R/W	0000_0001h	64.15.4/ 5216
21F_4088	UART Control Register 3 (UART5_UCR3)	32	R/W	0000_0700h	64.15.5/ 5219

Table continues on the next page...

67.4.7 Card Insertion and Removal Detection

The uSDHC uses either the DATA3 pin or the CD_B pin to detect card insertion or removal. When there is no card on the MMC/SD bus, the DATA3 will be pulled to a low voltage level by default.

When any card is inserted to or removed from the socket, the uSDHC detects the logic value changes on the DATA3 pin and generates an interrupt. When the DATA3 pin is not used for card detection (for example, it is implemented in GPIO), the CD_B pin must be connected for card detection. Whether DATA3 is configured for card detection or not, the CD_B pin is always a reference for card detection. Whether the DATA3 pin or the CD_B pin is used to detect card insertion, the uSDHC will send an interrupt (if enabled) to inform the Host system that a card is inserted.

67.4.8 Power Management and Wake Up Events

When there is no operation between the uSDHC and the card through the SD bus, the user can completely disable the ipg_clk and ipg_perclk in the chip level clock control module to save power. When the user needs to use the uSDHC to communicate with the card, it can enable the clock and start the operation.

In some circumstances, when the clocks to the uSDHC are disabled, for instance, when the system is in low power mode, there are some events for which the user needs to enable the clock and handle the event. These events are called wakeup interrupts. The uSDHC can generate these interrupt even when there are no clocks enabled. The three interrupts which can be used as wake up events are:

1. Card Removal Interrupt
2. Card Insertion Interrupt
3. Interrupt from SDIO card

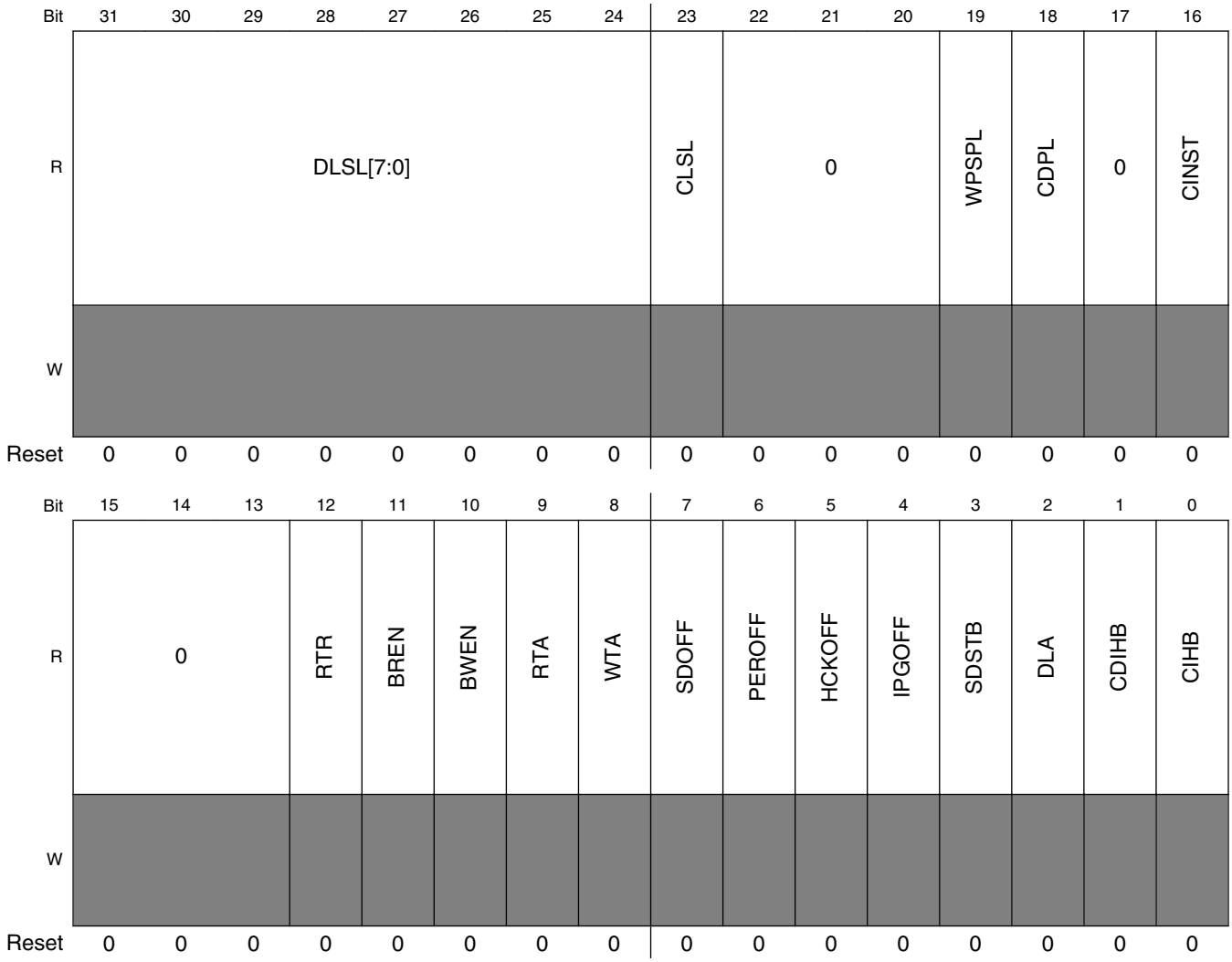
The uSDHC offers a power management feature. By clearing the clock enabled bits in the System Control Register, the clocks are gated in the low position to the uSDHC. For maximum power saving, the user can disable all the clocks to the uSDHC when there is no operation in progress.

These three wake up events (or wakeup interrupts) can also be used to wake up the system from low-power modes.

NOTE

To make the interrupt a wakeup event, when all the clocks to the uSDHC are disabled or when the whole system is in low power mode, the corresponding wakeup enabled bit needs to be

Address: Base address + 24h offset



uSDHCx_PRES_STATE field descriptions

Field	Description
31–24 DLSL[7:0]	DATA[7:0] Line Signal Level This status is used to check the DATA line level to recover from errors, and for debugging.This is especially useful in detecting the busy signal level from DATA0. The reset value is affected by the external pull-up / pull-down resistors. By default, the read value of this bit field after reset is 8'b11110111, when DATA3 is pulled down and the other lines are pulled up. DATA7 Data 7 line signal level DATA6 Data 6 line signal level DATA5 Data 5 line signal level DATA4 Data 4 line signal level DATA3 Data 3 line signal level DATA2 Data 2 line signal level DATA1 Data 1 line signal level DATA0 Data 0 line signal level

Table continues on the next page...