Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f105r8t6tr

2.3.6 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 20 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

2.3.7 Clocks and startup

System clock selection is performed on startup, however, the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 3-25 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

A single 25 MHz crystal can clock the entire system including the ethernet and USB OTG FS peripherals. Several prescalers and PLLs allow the configuration of the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz. The maximum allowed frequency of the low speed APB domain is 36 MHz. Refer to *Figure 59: USB O44TG FS + Ethernet solution on page 100*.

The advanced clock controller clocks the core and all peripherals using a single crystal or oscillator. In order to achieve audio class performance, an audio crystal can be used. In this case, the I^2S master clock can generate all standard sampling frequencies from 8 kHz to 96 kHz with less than 0.5% accuracy error. Refer to *Figure 60: USB OTG FS + I2S (Audio) solution on page 100*.

To configure the PLLs, refer to *Table 63 on page 101*, which provides PLL configurations according to the application type.

2.3.8 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1, USART2 (remapped), CAN2 (remapped) or USB OTG FS in device mode (DFU: device firmware upgrade). For remapped signals refer to *Table 5: Pin definitions*.

The USART peripheral operates with the internal 8 MHz oscillator (HSI), however the CAN and USB OTG FS can only function if an external 8 MHz, 14.7456 MHz or 25 MHz clock (HSE) is present.

For full details about the boot loader, refer to AN2606.

2.3.15 Timers and watchdogs

The STM32F105xx and STM32F107xx devices include an advanced-control timer, four general-purpose timers, two basic timers, two watchdog timers and a SysTick timer.

Table 4 compares the features of the general-purpose and basic timers.

Table 4. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TIMx (TIM2, TIM3, TIM4, TIM5)	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Advanced-control timer (TIM1)

The advanced control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

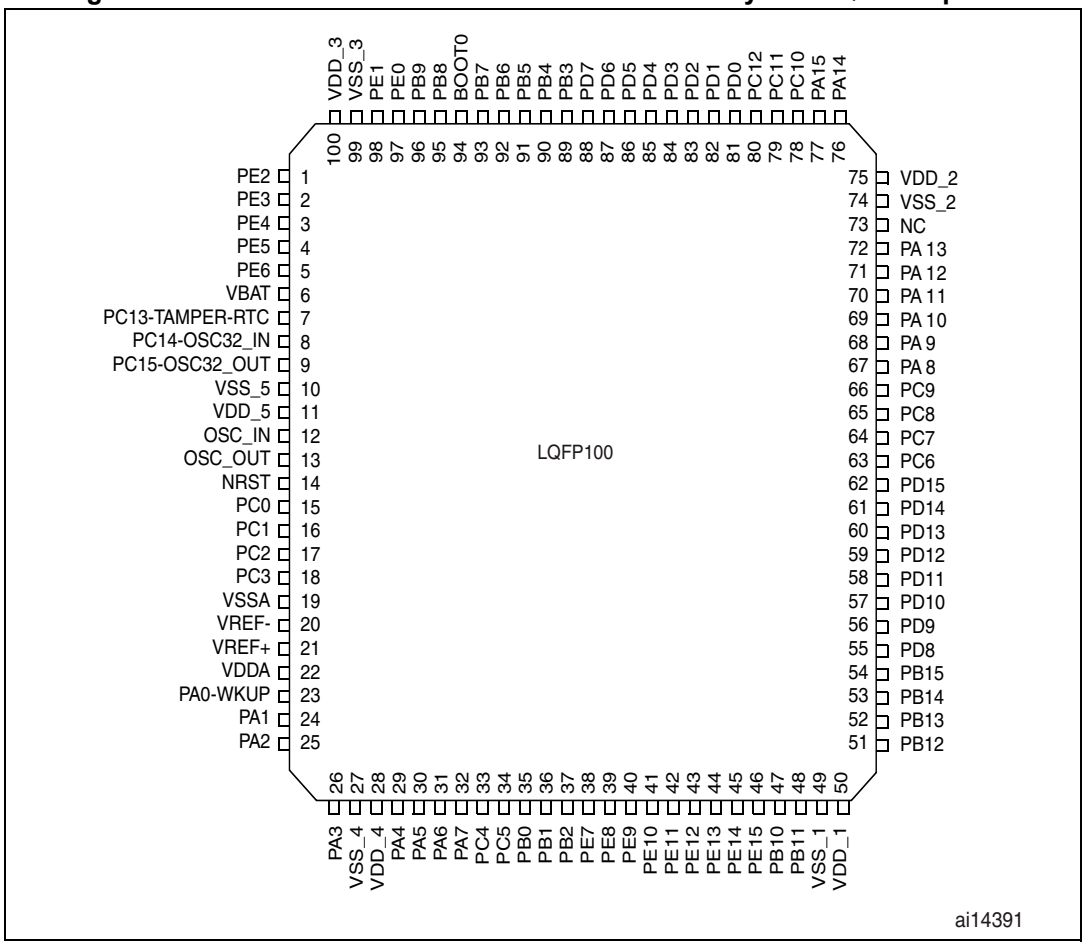
Many features are shared with those of the standard TIM timers which have the same architecture. The advanced control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are up to 4 synchronizable standard timers (TIM2, TIM3, TIM4 and TIM5) embedded in the STM32F105xx and STM32F107xx connectivity line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one pulse mode output. This gives up to 16 input captures / output compares / PWMs on the largest packages. They can work together with the Advanced Control timer via the Timer Link feature for synchronization or event chaining.

The counter can be frozen in debug mode.

Figure 3. STM32F105xx and STM32F107xx connectivity line LQFP100 pinout



5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 10. Operating condition at power-up / power down

Symbol	Parameter	Condition	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	-	µs/V
T_J	V_{DD} fall time rate		20	-	

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 11* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 11. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8(1)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	40	-	mV
$T_{RSTTEMPO}$(2)	Reset temporization	-	1	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.

5.3.4 Embedded reference voltage

The parameters given in *Table 12* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 12. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.16	1.20	1.26	V
		–40 °C < T_A < +85 °C	1.16	1.20	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	-	5.1	17.1(2)	µs
V_{RERINT}(2)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V ±10 mV	-	-	10	mV
T_{Coeff}(2)	Temperature coefficient	-	-	-	100	ppm/°C

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 9: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 13*, *Table 14* and *Table 15* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 17. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Run mode	External clock(3)	72 MHz	47.3	28.3	mA
			48 MHz	32	19.6	
			36 MHz	24.6	15.4	
			24 MHz	16.8	10.6	
			16 MHz	11.8	7.4	
			8 MHz	5.9	3.7	
			4 MHz	3.7	2.9	
			2 MHz	2.5	2	
			1 MHz	1.8	1.53	
			500 kHz	1.5	1.3	
			125 kHz	1.3	1.2	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	36 MHz	23.9	14.8	mA
			24 MHz	16.1	9.7	
			16 MHz	11.1	6.7	
			8 MHz	5.6	3.8	
			4 MHz	3.1	2.1	
			2 MHz	1.8	1.3	
			1 MHz	1.16	0.9	
			500 kHz	0.8	0.67	
			125 kHz	0.6	0.5	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 19. Peripheral current consumption (continued)

Peripheral		Typical consumption at 25 °C	Unit
APB2 (up to 72 MHz)	APB2-Bridge	3.47	µA/MHz
	GPIOA	6.39	
	GPIOB	6.39	
	GPIOC	6.11	
	GPIOD	6.39	
	GPIOE	6.11	
	SPI1	3.61	
	USART1	12.08	
	TIM1	23.47	
	ADC1(4)	18.21	

1. The BusMatrix is automatically active when at least one master is ON.(CPU, ETH-MAC, DMA1 or DMA2).
2. When I2S is enabled we have a consumption add equal to 0, 02 mA.
3. When DAC_OUT1 or DAC_OUT2 is enabled we have a consumption add equal to 0, 3 mA.
4. Specific conditions for measuring ADC current consumption: f_{HCLK} = 56 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/4$. When ADON bit in the ADC_CR2 register is set to 1, a current consumption of analog part equal to 0.6 mA must be added.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

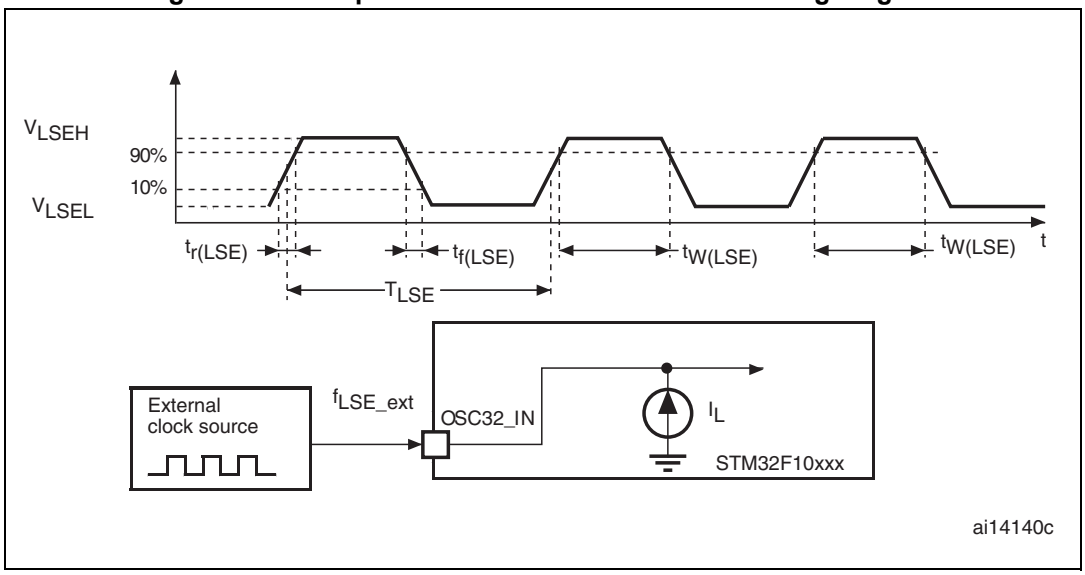
The characteristics given in *Table 20* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 9*.

Table 20. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External user clock source frequency(1)	-	1	8	50	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Figure 15. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 3 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 22*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 22. HSE 3-25 MHz oscillator characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	3		25	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	30	-	pF
i_2	HSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization, not tested in production.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Table 23. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{SU(LSE)}$ (4)	Startup time	V_{DD} is stabilized	T_A = 50 °C	-	1.5	-	s
			T_A = 25 °C	-	2.5	-	
			T_A = 10 °C	-	4	-	
			T_A = 0 °C	-	6	-	
			T_A = -10 °C	-	10	-	
			T_A = -20 °C	-	17	-	
			T_A = -30 °C	-	32	-	
			T_A = -40 °C	-	60	-	

1. Based on characterization, not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For C_{L1} and C_{L2} it is recommended to use high-quality external ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Figure 17). C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.
Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if you choose a resonator with a load capacitance of C_L = 6 pF, and C_{stray} = 2 pF, then $C_{L1} = C_{L2}$ = 8 pF.

Figure 17. Typical application with a 32.768 kHz crystal

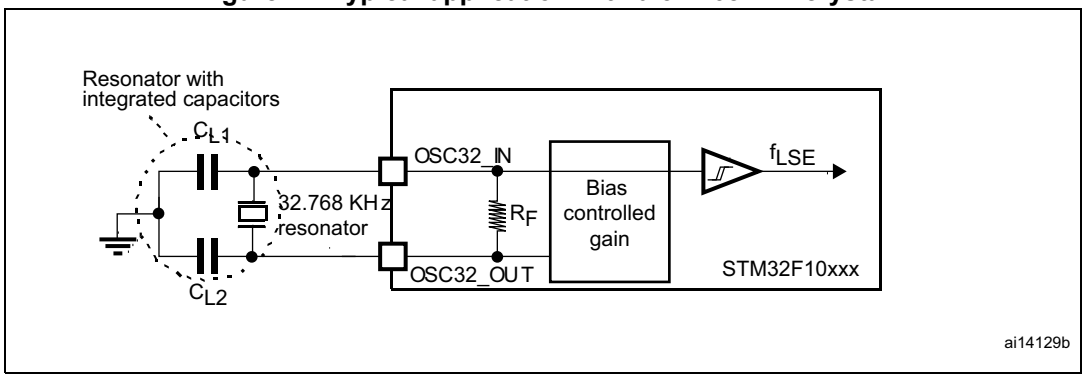


Table 32. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]		Unit
				8/48 MHz	8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP100 package compliant with IEC61967-2	0.1 to 30 MHz	9	9	dBµV
			30 to 130 MHz	26	13	
			130 MHz to 1GHz	25	31	
			EMI Level	4	4	-

5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 33. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to JESD22-C101	II	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 34. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

5.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product

operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 35*

Table 35. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

5.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 36* are derived from tests performed under the conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 36. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO input low level voltage	-	–0.3	-	0.28*(V_{DD}-2 V)+0.8 V	V
	IO FT(1) input low level voltage	-	–0.3	-	0.32*(V_{DD}-2V)+0.75 V	V
V_{IH}	Standard IO input high level voltage	-	0.41*(V_{DD}-2 V)+1.3 V	-	V_{DD}+0.3	V
	IO FT(1) input high level voltage	V_{DD} > 2 V	0.42*(V_{DD}-2 V)+1 V	-	5.5	V
		$V_{DD} \leq$ 2 V			5.2	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis(2)	-	200	-	-	mV
	IO FT Schmitt trigger voltage hysteresis(2)	-	5% V_{DD}(3)	-	-	mV

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/-20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 7*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 7*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 37* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 37. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(2)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port I_{IO} =+ 8mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (2)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4	-	
V_{OL}(1)(3)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH}(2)(3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–1.3	-	
V_{OL}(1)(3)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(2)(3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
3. Based on characterization data, not tested in production.

Table 44. I^2S characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master data: 16 bits, audio freq = 48 K		1.52	1.54	MHz
		Slave		0	6.5	
$t_{r(CK)}$ $t_{f(CK)}$	I^2S clock rise and fall time	capacitive load C_L = 50 pF		-	8	ns
$t_{w(CKH)}$ (1)	I^2S clock high time	Master f_{PCLK} = 16 MHz, audio freq = 48 K		317	320	
$t_{w(CKL)}$ (1)	I^2S clock low time			333	336	
$t_{v(WS)}$ (1)	WS valid time	Master mode		3	-	
$t_{h(WS)}$ (1)	WS hold time	Master mode	I2S2	0	-	
			I2S3	0	-	
$t_{su(WS)}$ (1)	WS setup time	Slave mode	I2S2	4	-	
			I2S3	9	-	
$t_{h(WS)}$ (1)	WS hold time	Slave mode		0	-	
DuCy(SCK)	I2S slave input clock duty cycle	Slave mode		30	70	%
$t_{su(SD\_MR)}$ (1)	Data input setup time	Master receiver	I2S2	8	-	ns
			I2S3	10	-	
$t_{su(SD\_SR)}$ (1)		Slave receiver	I2S2	3	-	
			I2S3	8	-	
$t_{h(SD\_MR)}$ (1)	Data input hold time	Master receiver	I2S2	2	-	
			I2S3	4	-	
$t_{h(SD\_SR)}$ (1)		Slave receiver	I2S2	2	-	
			I2S3	4	-	
$t_{v(SD\_ST)}$ (1)(3)	Data output valid time	Slave transmitter (after enable edge)	I2S2	23	-	
			I2S3	33	-	
$t_{h(SD\_ST)}$ (1)	Data output hold time	Slave transmitter (after enable edge)	I2S2	29	-	
			I2S3	27	-	
$t_{v(SD\_MT)}$ (1)	Data output valid time	Master transmitter (after enable edge)	I2S2	-	5	
			I2S3	-	2	
$t_{h(SD\_MT)}$ (1)	Data output hold time	Master transmitter (after enable edge)	I2S2	11	-	
			I2S3	4	-	

1. Based on design simulation and/or characterization results, not tested in production.

5.3.18 DAC electrical specifications

Table 56. DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	2.4	-	3.6	V	-
V_{REF+}	Reference supply voltage	2.4	-	3.6	V	V_{REF+} must always be below V_{DDA}
V_{SSA}	Ground	0	-	0	V	-
R_{LOAD}(1)	Resistive load with buffer ON	5	-	-	kΩ	-
R_O(1)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(1)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x155) to (0xEAB) at V_{REF+} = 2.4 V
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer OFF	-	-	V_{REF+} – 1LSB	V	
$I_{DDVREF+}$	DAC DC current consumption in quiescent mode (Standby mode)	-	-	220	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
I_{DDA}	DAC DC current consumption in quiescent mode (Standby mode)	-	-	380	µA	With no load, middle code (0x800) on the inputs
		-	-	480	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
DNL(2)	Differential non linearity Difference between two consecutive code-1LSB)	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration.
		-	-	±2	LSB	Given for the DAC in 12-bit configuration.
INL(2)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±1	LSB	Given for the DAC in 10-bit configuration.
		-	-	±4	LSB	Given for the DAC in 12-bit configuration.

Using the values obtained in *Table 61* T_{Jmax} is calculated as follows:

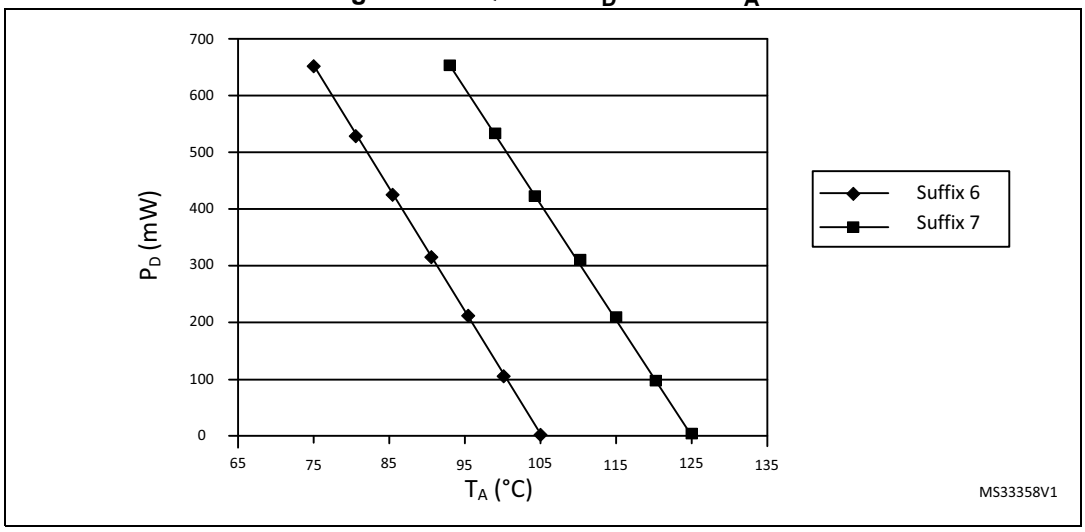
– For LQFP100, 46 °C/W

T_{Jmax} = 115 °C + (46 °C/W × 134 mW) = 115 °C + 6.2 °C = 121.2 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 62: Ordering information scheme*).

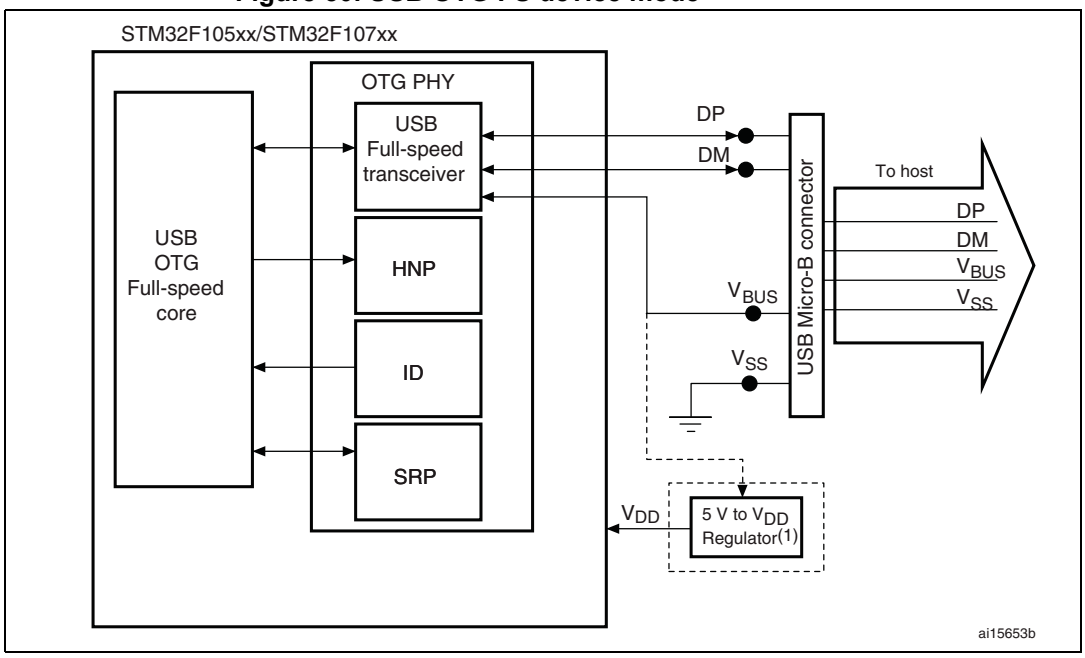
Figure 49. LQFP100 P_D max vs. T_A



Appendix A Application block diagrams

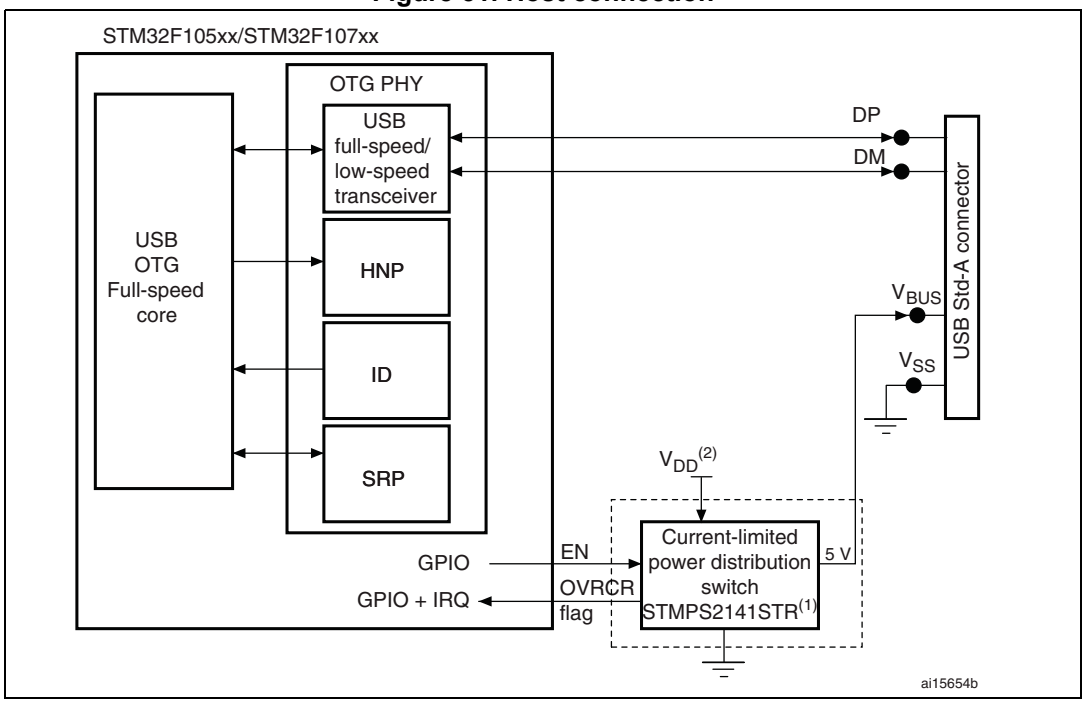
A.1 USB OTG FS interface solutions

Figure 50. USB OTG FS device mode



1. Use a regulator if you want to build a bus-powered device.

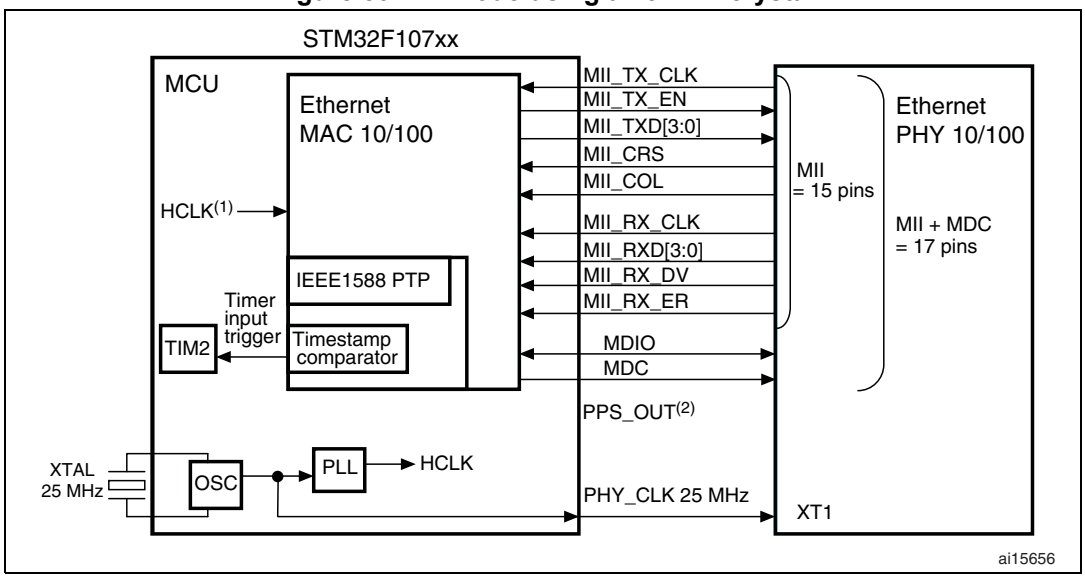
Figure 51. Host connection



1. STMPS2141STR needed only if the application has to support bus-powered devices.

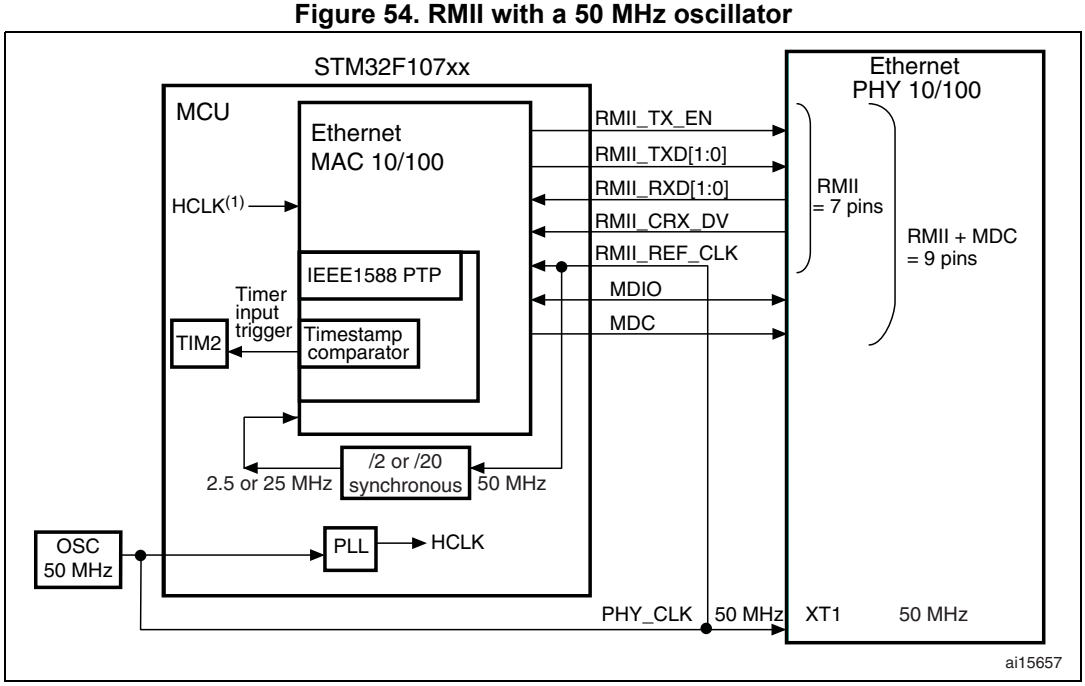
A.2 Ethernet interface solutions

Figure 53. MII mode using a 25 MHz crystal



1. HCLK must be greater than 25 MHz.
2. Pulse per second when using IEEE1588 PTP, optional signal.

Figure 54. RMII with a 50 MHz oscillator



1. HCLK must be greater than 25 MHz.

Table 65. Document revision history (continued)

Date	Revision	Changes
19-Jun-2009	3	*Section 2.3.8: Boot modes* and *Section 2.3.20: Ethernet MAC interface with dedicated DMA and IEEE 1588 support* updated. *Section 2.3.24: Remap capability* added. *Figure 1: STM32F105xx and STM32F107xx connectivity line block diagram* and *Figure 5: Memory map* updated. In *Table 5: Pin definitions*: – I2S3_WS, I2S3_CK and I2S3_SD default alternate functions added – small changes in signal names – *Note 6* modified – ETH_MII_PPS_OUT and ETH_RMII_PPS_OUT replaced by ETH_PPS_OUT – ETH_MII_MDIO and ETH_RMII_MDIO replaced by ETH_MDIO – ETH_MII_MDC and ETH_RMII_MDC replaced by ETH_MDC Figures: *Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled* and *Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled* removed. *Table 13: Maximum current consumption in Run mode, code with data processing running from Flash*, *Table 14: Maximum current consumption in Run mode, code with data processing running from RAM* and *Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM* are to be determined. *Figure 12* and *Figure 13* show typical curves. PLL1 renamed to PLL. I_{DD} supply current in Stop mode modified in *Table 16: Typical and maximum current consumptions in Stop and Standby modes*. *Figure 11: Typical current consumption in Stop mode with regulator in Run mode versus temperature at different VDD values*, *Figure 13: Typical current consumption in Standby mode versus temperature at different VDD values* and *Figure 13: Typical current consumption in Standby mode versus temperature at different VDD values* updated. *Table 17: Typical current consumption in Run mode, code with data processing running from Flash*, *Table 18: Typical current consumption in Sleep mode, code running from Flash or RAM* and *Table 19: Peripheral current consumption* updated. f_{HSE_ext} modified in *Table 20: High-speed external user clock characteristics*. Min PLL input clock (f_{PLL_IN}), f_{PLL_OUT} min and f_{PLL_VCO} min modified in *Table 27: PLL characteristics*. ACC_{HSI} max values modified in *Table 24: HSI oscillator characteristics*. *Table 31: EMS characteristics* and *Table 32: EMI characteristics* updated. *Table 43: SPI characteristics* updated. Modified: *Figure 28: I2S slave timing diagram (Philips protocol)(1)*, *Figure 29: I2S master timing diagram (Philips protocol)(1)* and *Figure 31: Ethernet SMI timing diagram*. BGA100 package removed. *Section 6.4: Thermal characteristics* added. Small text changes.

Table 65. Document revision history (continued)

Date	Revision	Changes
11-May-2010	5	Added BGA package. *Table 5: Pin definitions*: ETH_RMII_RXD0 and ETH_RMII_RXD1 added in remap column for PD9 and PD10, respectively. Note added to ETH_MII_RX_DV, ETH_MII_RXD0, ETH_MII_RXD1, ETH_MII_RXD2 and ETH_MII_RXD3 Updated *Table 36: I/O static characteristics on page 57* Added *Figure 18: Standard I/O input characteristics - CMOS port* to *Figure 21: 5 V tolerant I/O input characteristics - TTL port* Updated *Table 43: SPI characteristics on page 66*. Updated *Table 44: I2S characteristics on page 69*. Updated *Table 48: Ethernet DC electrical characteristics on page 72*. Updated *Table 49: Dynamic characteristics: Ethernet MAC signals for SMI on page 72*. Updated *Table 50: Dynamic characteristics: Ethernet MAC signals for RMII on page 73* Updated *Figure 59: USB O44TG FS + Ethernet solution on page 100*. Updated *Figure 60: USB OTG FS + I2S (Audio) solution on page 100*
01-Aug-2011	6	Changed SRAM size to 64 KB on all parts. Updated PD0 and PD1 description in *Table 5: Pin definitions on page 27* Updated footnotes below *Table 6: Voltage characteristics on page 36* and *Table 7: Current characteristics on page 36* Updated tw min in *Table 20: High-speed external user clock characteristics on page 47* Updated startup time in *Table 23: LSE oscillator characteristics (fLSE = 32.768 kHz) on page 50* Added *Section 5.3.12: I/O current injection characteristics on page 56* Updated *Table 36: I/O static characteristics on page 57* Add Interna code V to *Table 62: Ordering information scheme on page 94*
06-Mar-2014	7	Added a “Packing” entry to *Table 62: Ordering information scheme* including “Blank = tray” and “TR = Tape and reel”. Referenced 4 Figures: *Figure 41*, *Figure 49*, *Figure 59* and *Figure 60*. Updated the “Package” line with “BGA100” in *Table 2: STM32F105xx and STM32F107xx features and peripheral counts*.

Table 65. Document revision history (continued)

Date	Revision	Changes
06-Mar-2015	8	Updated *Table 40: LFBGA100 – 100-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data*, *Table 59: LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data* and *Table 60: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data* Updated *Figure 14: High-speed external clock source AC timing diagram*; *Figure 39: LFBGA100 - 10 x 10 mm low profile fine pitch ball grid array package outline*, *Figure 43: LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package outline*, *Figure 44: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint*, *Figure 46: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Figure 47: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint* Added *Figure 45: LQFP100 marking example (package top view)*, *Figure 48: LQFP64 marking example (package top view)*
3-Sept-2015	9	Updated: – *Table 19: Peripheral current consumption* – *Figure 44: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint* – *Table 58: LFBGA100 recommended PCB design rules (0.8 mm pitch BGA)*
22-Mar-2017	10	Updated: – *Table 5: Pin definitions* – *Section 6: Package information* Added: – *Figure 42: LFBGA100 marking example (package top view)*