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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f105rbt6

List of figures

Any of the standard timers can be used to generate PWM outputs. Each of the timers has independent DMA request generations.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.3.16 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.3.17 Universal synchronous/asynchronous receiver transmitters (USARTs)

The STM32F105xx and STM32F107xx connectivity line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART1 interface is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s.

USART1, USART2 and USART3 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

2.3.18 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC/SDHC[a] modes.

All SPIs can be served by the DMA controller.

2.3.19 Inter-integrated sound (I^2S)

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 96 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency with less than 0.5% accuracy error owing to the advanced clock controller (see *Section 2.3.7: Clocks and startup*).

Refer to the “Audio frequency precision” tables provided in the “Serial peripheral interface (SPI)” section of the STM32F10xxx reference manual.

2.3.20 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

Peripheral not available on STM32F105xx devices.

The STM32F107xx devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard media-independent interface (MII) or a reduced media-independent interface (RMII). The STM32F107xx requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). the PHY is connected to the STM32F107xx MII port using as many as 17 signals (MII) or 9 signals (RMII) and can be clocked using the 25 MHz (MII) or 50 MHz (RMII) output from the STM32F107xx.

The STM32F107xx includes the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors (see the STM32F105xx/STM32F107xx reference manual for details)
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support

a. SDHC = Secure digital high capacity.

- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes, that is 4 Kbytes in total
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 with the timestamp comparator connected to the TIM2 trigger input
- Triggers interrupt when system time becomes greater than target time

2.3.21 Controller area network (CAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). The 256 bytes of SRAM which are allocated for each CAN (512 bytes in total) are not shared with any other peripheral.

2.3.22 Universal serial bus on-the-go full-speed (USB OTG FS)

The STM32F105xx and STM32F107xx connectivity line devices embed a USB OTG full-speed (12 Mb/s) device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- 1.25 KB of SRAM used exclusively by the endpoints (not shared with any other peripheral)
- 4 bidirectional endpoints
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected
- the SOF output can be used to synchronize the external audio DAC clock in isochronous mode
- in accordance with the USB 2.0 Specification, the supported transfer speeds are:
  - in Host mode: full speed and low speed
  - in Device mode: full speed

2.3.23 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

I/Os on APB2 with up to 18 MHz toggling speed

3 Pinouts and pin description

Figure 2. STM32F105xx and STM32F107xx connectivity line BGA100 ballout top view

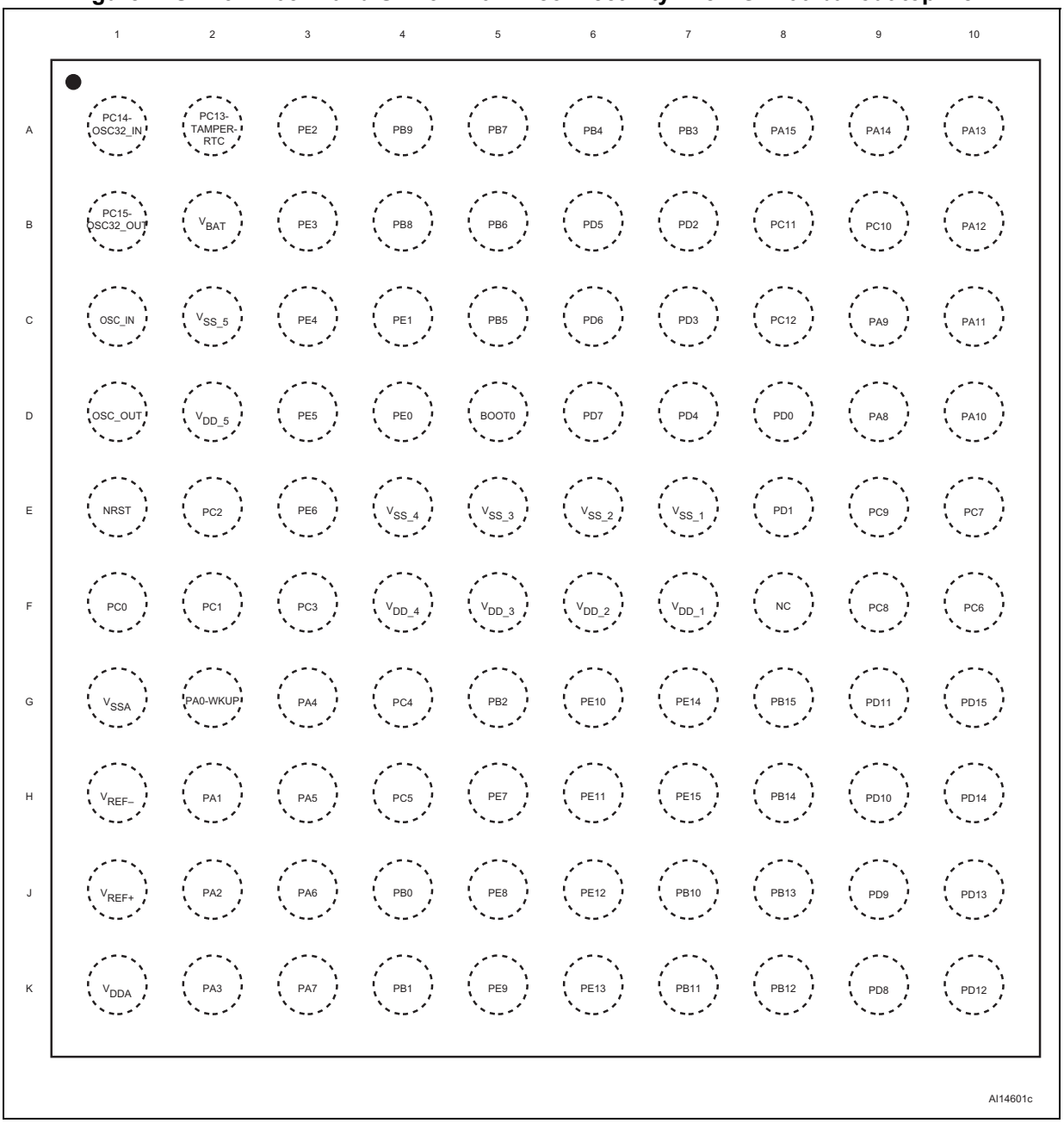


Figure 3. STM32F105xx and STM32F107xx connectivity line LQFP100 pinout

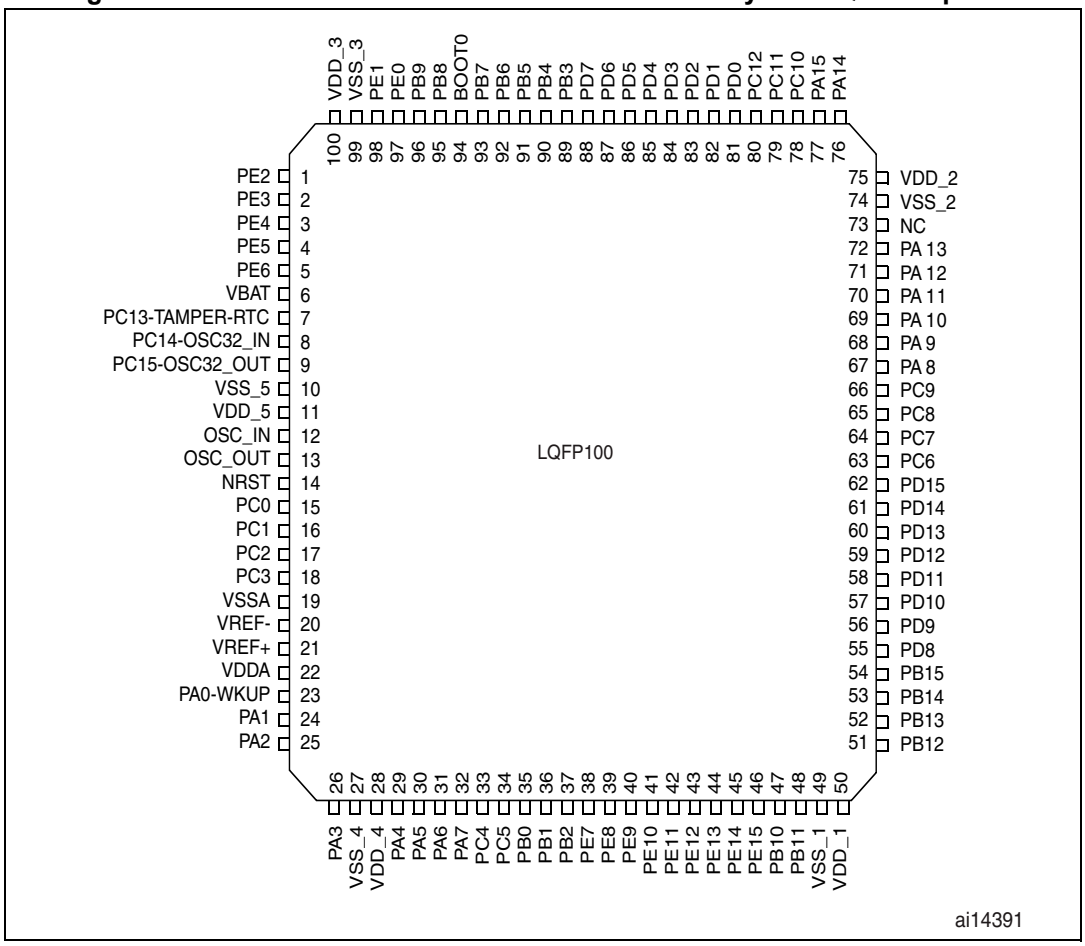


Table 5. Pin definitions (continued)

Pins			Pin name	Type[1]	I / O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
BGA100	LQFP64	LQFP100					Default	Remap
J9	-	56	PD9	I/O	FT	PD9	-	USART3_RX/ ETH_MII_RXD0/ ETH_RMII_RXD0
H9	-	57	PD10	I/O	FT	PD10	-	USART3_CK/ ETH_MII_RXD1/ ETH_RMII_RXD1
G9	-	58	PD11	I/O	FT	PD11	-	USART3_CTS/ ETH_MII_RXD2
K10	-	59	PD12	I/O	FT	PD12	-	TIM4_CH1 / USART3_RTS/ ETH_MII_RXD3
J10	-	60	PD13	I/O	FT	PD13	-	TIM4_CH2
H10	-	61	PD14	I/O	FT	PD14	-	TIM4_CH3
G10	-	62	PD15	I/O	FT	PD15	-	TIM4_CH4
F10	37	63	PC6	I/O	FT	PC6	I2S2_MCK/	TIM3_CH1
E10	38	64	PC7	I/O	FT	PC7	I2S3_MCK	TIM3_CH2
F9	39	65	PC8	I/O	FT	PC8	-	TIM3_CH3
E9	40	66	PC9	I/O	FT	PC9	-	TIM3_CH4
D9	41	67	PA8	I/O	FT	PA8	USART1_CK/OTG_FS_SOF / TIM1_CH1[8]/MCO	-
C9	42	68	PA9	I/O	FT	PA9	USART1_TX[7]/ TIM1_CH2[7]/ OTG_FS_VBUS	-
D10	43	69	PA10	I/O	FT	PA10	USART1_RX[7]/ TIM1_CH3[7]/OTG_FS_ID	-
C10	44	70	PA11	I/O	FT	PA11	USART1_CTS / CAN1_RX / TIM1_CH4[7]/OTG_FS_DM	-
B10	45	71	PA12	I/O	FT	PA12	USART1_RTS / OTG_FS_DP / CAN1_TX[7] / TIM1_ETR[7]	-
A10	46	72	PA13	I/O	FT	JTMS-SWDIO	-	PA13
F8	-	73	Not connected					-
E6	47	74	V_{SS_2}	S	-	V_{SS_2}	-	-
F6	48	75	V_{DD_2}	S	-	V_{DD_2}	-	-
A9	49	76	PA14	I/O	FT	JTCK-SWCLK	-	PA14

5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 6: Voltage characteristics*, *Table 7: Current characteristics*, and *Table 8: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five volt tolerant pin	V_{SS} –0.3	V_{DD} +4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.11: Absolute maximum ratings (electrical sensitivity)*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 7: Current characteristics* for the maximum allowed injected current values.

Table 7. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	–25	
$I_{INJ(PIN)}$(2)	Injected current on five volt tolerant pins(3)	-5/+0	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See *Note: on page 76*.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 6: Voltage characteristics* for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 6: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 8. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

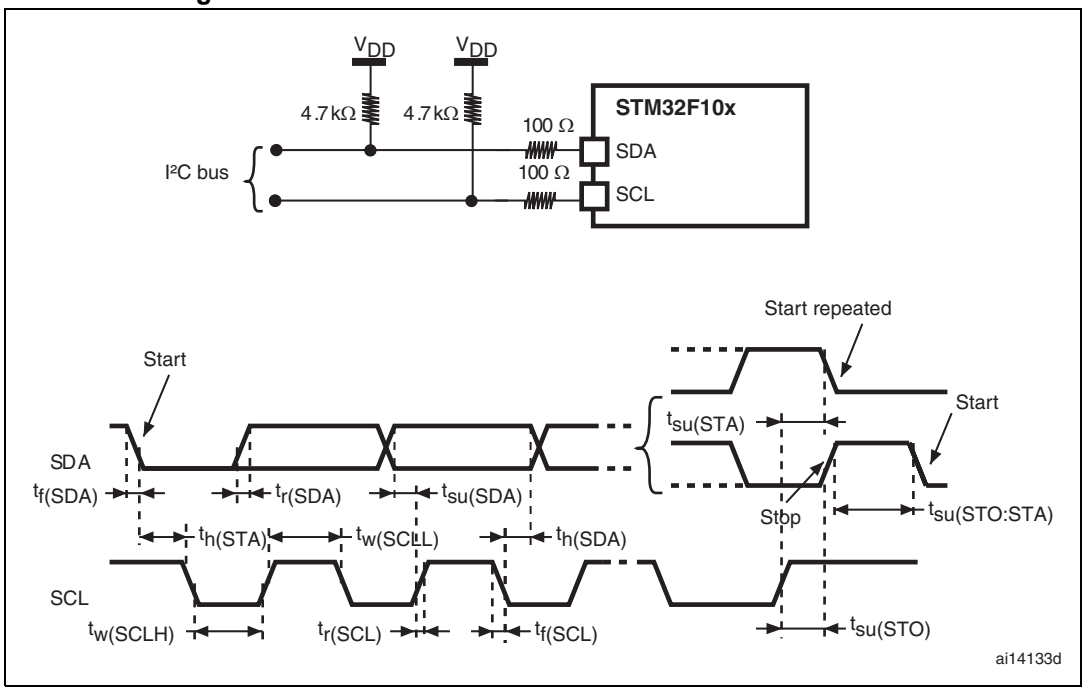
5.3.1 General operating conditions

Table 9. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	
f_{PCLK2}	Internal APB2 clock frequency	-	0	72	
V_{DD}	Standard operating voltage	-	2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	Must be the same potential as V_{DD}(2)	2	3.6	V
	Analog operating voltage (ADC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.8	3.6	V
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(3)	LFBGA100	-	500	mW
		LQFP100	-	434	
		LQFP64	-	444	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(4)	LQFP100	-	434	mW
		LQFP64	-	444	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(5)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low power dissipation(5)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. When the ADC is used, refer to *Table 52: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.
3. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max.
5. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max.

Figure 24. I²C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 42. SCL frequency (f_{PCLK1}= 36 MHz.,V_{DD} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

I^2S - SPI interface characteristics

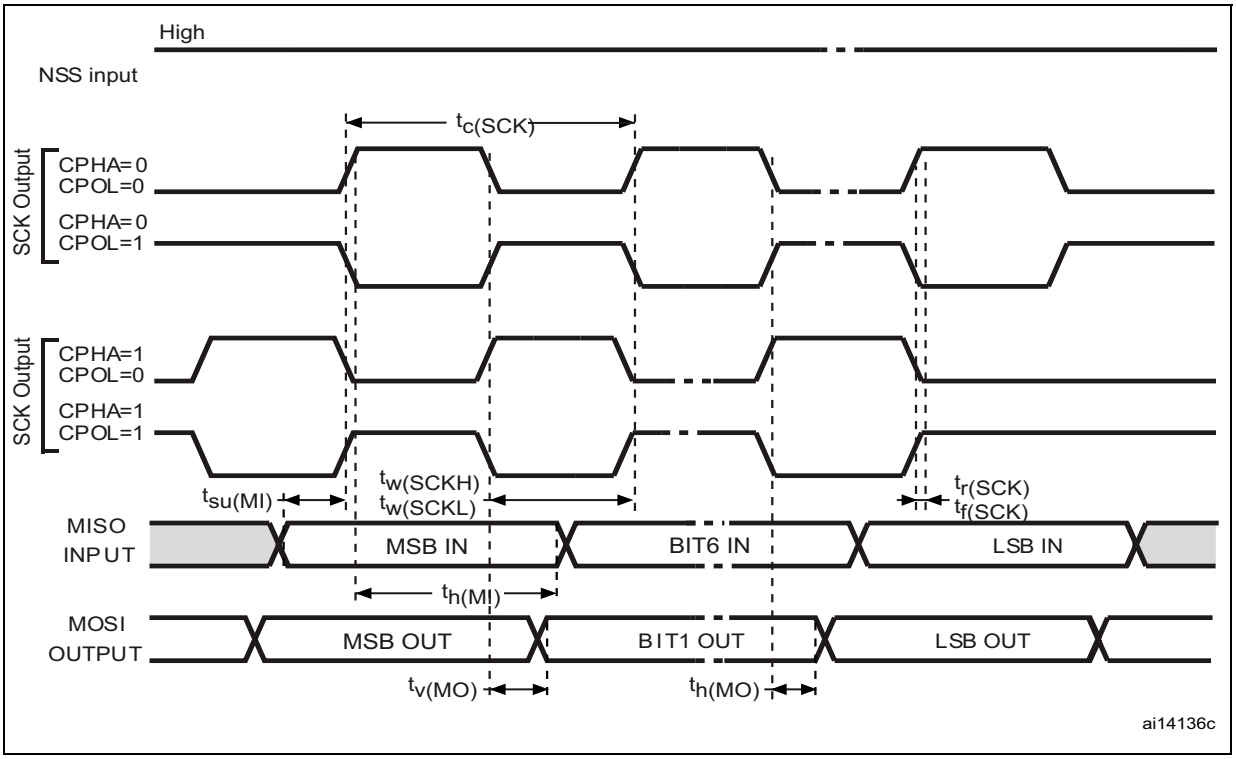
Unless otherwise specified, the parameters given in *Table 43* for SPI or in *Table 44* for I^2S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

Refer to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I^2S).

Table 43. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode	4 t_{PCLK}	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2 t_{PCLK}	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	50	60	
$t_{su(MI)}$	Data input setup time	Master mode	4	-	
$t_{su(SI)}$		Slave mode	5	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	
$t_{h(SI)}$		Slave mode	5	-	
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK} = 20 MHz	-	3*t_{PCLK}	
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	-	34	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	8	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	32	-	
$t_{h(MO)}$		Master mode (after enable edge)	10	-	

Figure 27. SPI timing diagram - master mode(1)



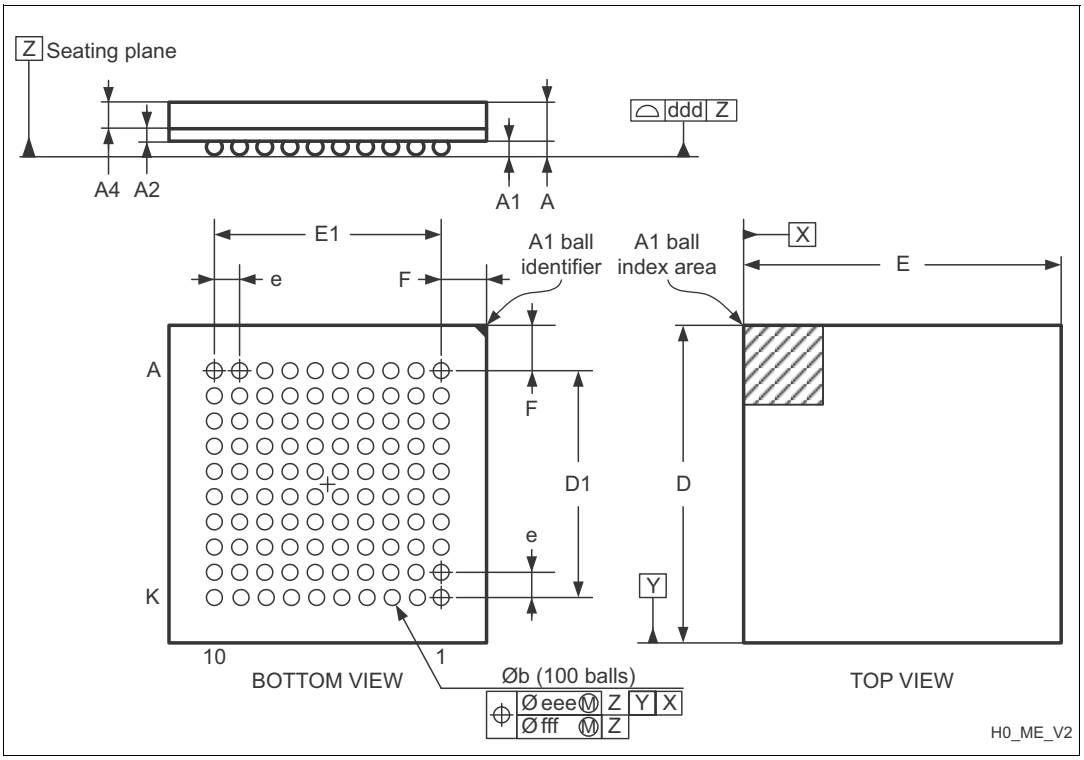
1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

6.1 LFBGA100 package information

Figure 39. LFBGA100 - 10 x 10 mm low profile fine pitch ball grid array package outline

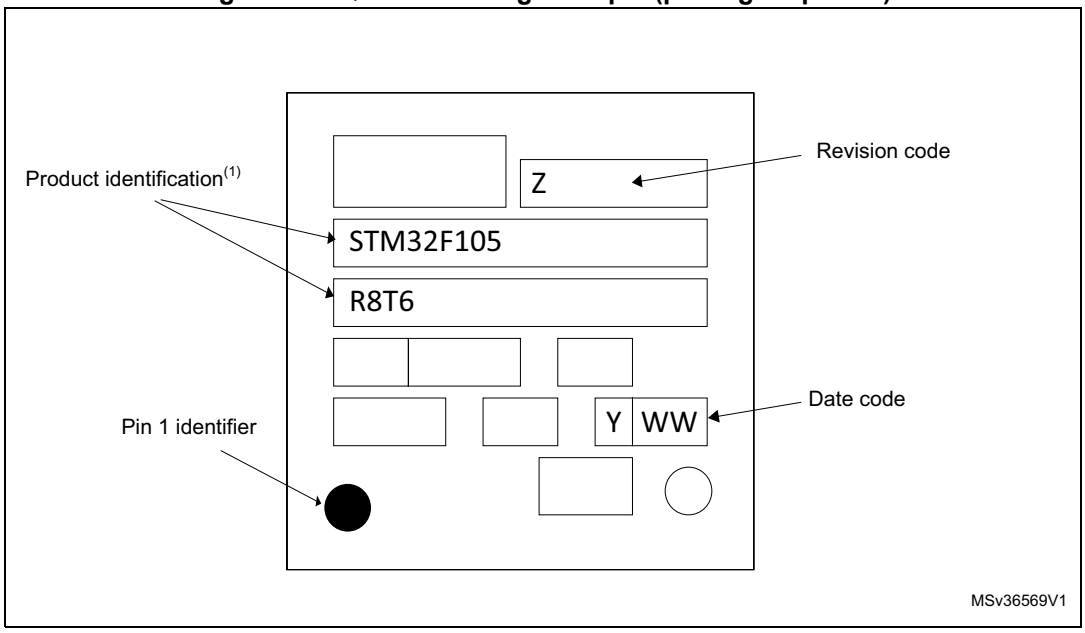


Device marking for LQFP64

The following figure shows the device marking for the LQFP64 package.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 48.LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6.4 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 9: General operating conditions on page 37*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 61. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	°C/W
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	
Θ_{JA}	**Thermal resistance junction-ambient** LFBGA100 - 10 × 10 mm / 0.8 mm pitch	40	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	

6.4.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

Using the values obtained in *Table 61* T_{Jmax} is calculated as follows:

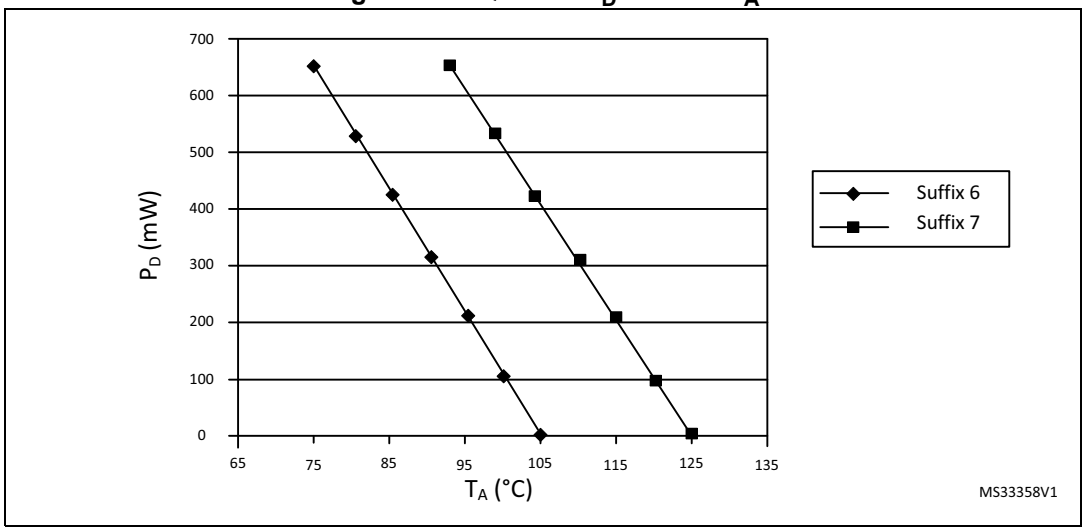
– For LQFP100, 46 °C/W

T_{Jmax} = 115 °C + (46 °C/W × 134 mW) = 115 °C + 6.2 °C = 121.2 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 62: Ordering information scheme*).

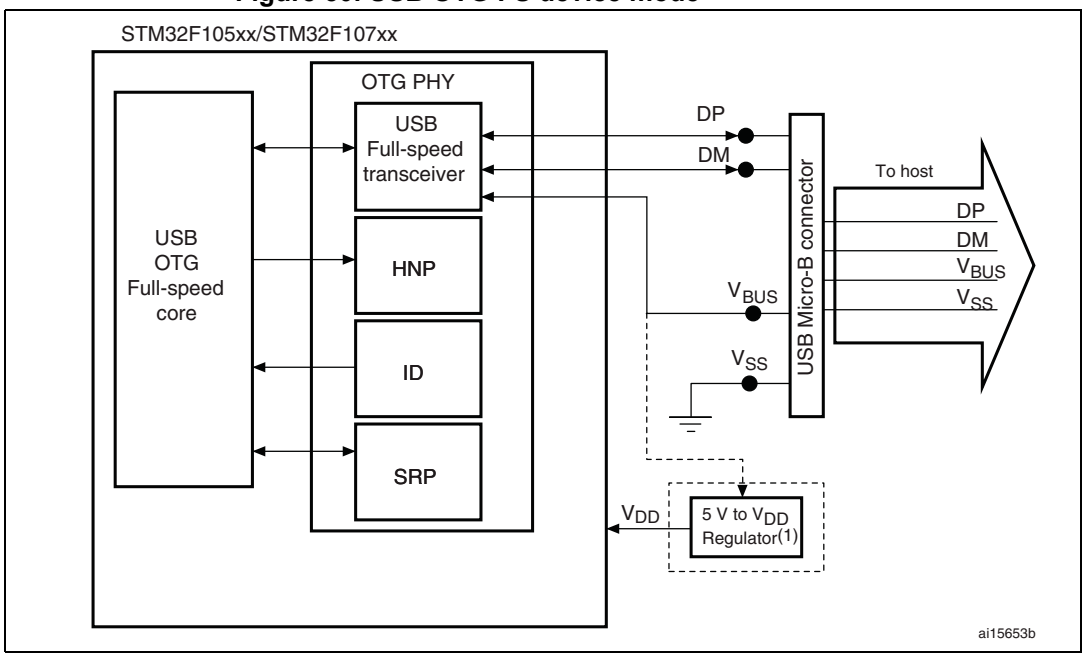
Figure 49. LQFP100 P_D max vs. T_A



Appendix A Application block diagrams

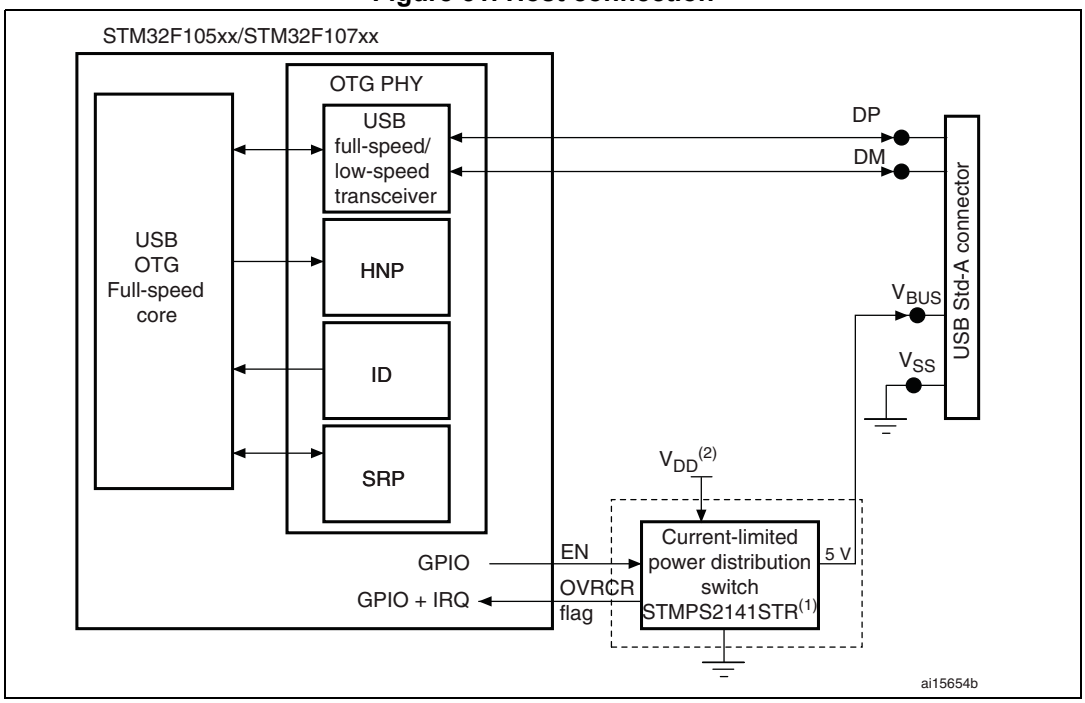
A.1 USB OTG FS interface solutions

Figure 50. USB OTG FS device mode



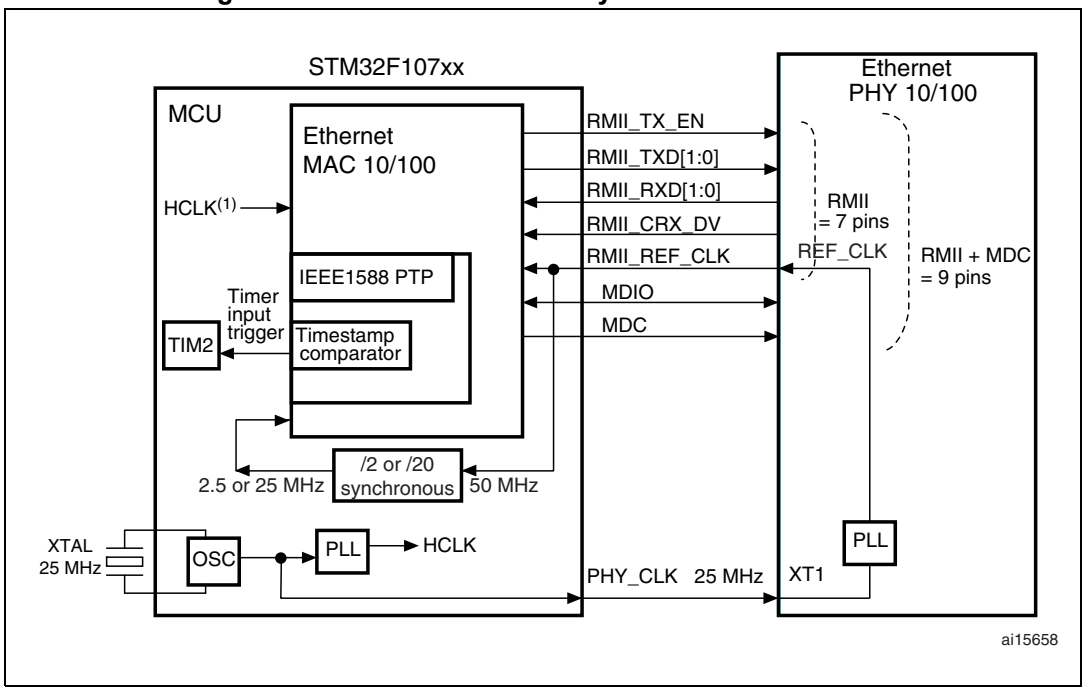
1. Use a regulator if you want to build a bus-powered device.

Figure 51. Host connection



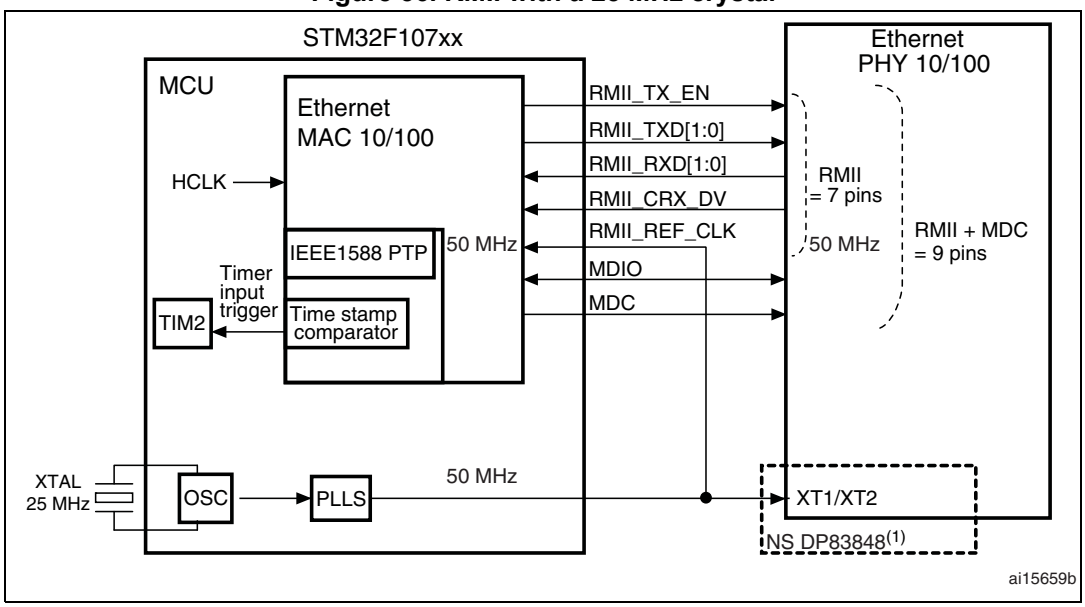
1. STMPS2141STR needed only if the application has to support bus-powered devices.

Figure 55. RMII with a 25 MHz crystal and PHY with PLL



1. HCLK must be greater than 25 MHz.

Figure 56. RMII with a 25 MHz crystal



1. The NS DP83848 is recommended as the input jitter requirement of this PHY. It is compliant with the output jitter specification of the MCU.

Table 63. PLL configurations

Application	Crystal value in MHz (XT1)	PREDIV2	PLL2MUL	PLLSRC	PREDIV1	PLLMUL	USB prescaler (PLLVCO output)	PLL3MUL	I2Sn clock input	MCO (main clock output)
Ethernet only	25	/5	PLL2ON x8	PLL2	/5	PLLON x9	NA	PLL3ON x10	NA	XT1 (MII) PLL3 (RMII)
Ethernet + OTG	25	/5	PLL2ON x8	PLL2	/5	PLLON x9	/3	PLL3ON x10	NA	XT1 (MII) PLL3 (RMII)
Ethernet + OTG + basic audio	25	/5	PLL2ON x8	PLL2	/5	PLLON x9	/3	PLL3ON x10	PLL	XT1 (MII) PLL3 (RMII)
Ethernet + OTG + Audio class I^2S(1)	14.7456	/4	PLL2ON x12	PLL2	/4	PLLON x6.5	/3	PLL3ON x20	PLL3 VCO Out	NA ETH PHY must use its own crystal
OTG only	8	NA	PLL2OFF	XT1	/1	PLLON x9	/3	PLL3OFF	NA	NA
OTG + basic audio	8	NA	PLL2OFF	XT1	/1	PLLON x9	/3	PLL3OFF	PLL	NA
OTG + Audio class I^2S(1)	14.7456	/4	PLL2ON x12	PLL2	/4	PLLON x6.5	/3	PLL3ON x20	PLL3 VCO Out	NA
Audio class I^2S only(1)	14.7456	/4	PLL2ON x12	PLL2	/4	PLLON x6.5	NA	PLL3ON x20	PLL3 VCO out	NA

1. SYSCLK is set to be at 72 MHz except in this case where SYSCLK is at 71.88 MHz.

Table 64 give the I_{DD} run mode values that correspond to the conditions specified in *Table 63*.