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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f105rbt6tr

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2.3.6 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 20 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

2.3.7 Clocks and startup

System clock selection is performed on startup, however, the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 3-25 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

A single 25 MHz crystal can clock the entire system including the ethernet and USB OTG FS peripherals. Several prescalers and PLLs allow the configuration of the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz. The maximum allowed frequency of the low speed APB domain is 36 MHz. Refer to *Figure 59: USB O44TG FS + Ethernet solution on page 100*.

The advanced clock controller clocks the core and all peripherals using a single crystal or oscillator. In order to achieve audio class performance, an audio crystal can be used. In this case, the I^2S master clock can generate all standard sampling frequencies from 8 kHz to 96 kHz with less than 0.5% accuracy error. Refer to *Figure 60: USB OTG FS + I2S (Audio) solution on page 100*.

To configure the PLLs, refer to *Table 63 on page 101*, which provides PLL configurations according to the application type.

2.3.8 Boot modes

At startup, boot pins are used to select one of three boot options:

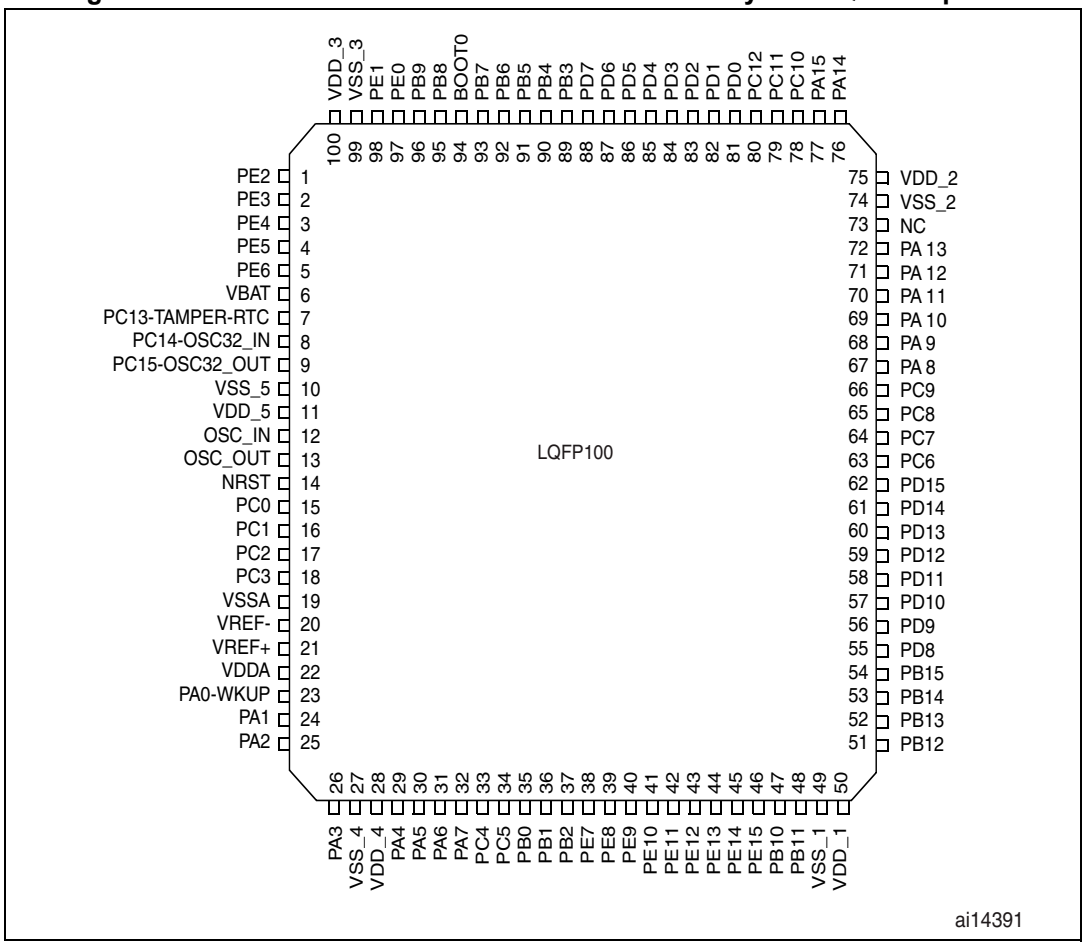
- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1, USART2 (remapped), CAN2 (remapped) or USB OTG FS in device mode (DFU: device firmware upgrade). For remapped signals refer to *Table 5: Pin definitions*.

The USART peripheral operates with the internal 8 MHz oscillator (HSI), however the CAN and USB OTG FS can only function if an external 8 MHz, 14.7456 MHz or 25 MHz clock (HSE) is present.

For full details about the boot loader, refer to AN2606.

Figure 3. STM32F105xx and STM32F107xx connectivity line LQFP100 pinout



1. I = input, O = output, S = supply, HiZ = high impedance.
2. FT = 5 V tolerant. All I/Os are V_{DD} capable.
3. Function availability depends on the chosen device.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch, and so their use in output mode is limited: they can be used only in output 2 MHz mode with a maximum load of 30 pF and only one pin can be put in output mode at a time.
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
7. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
8. SPI2/I2S2 and I2C2 are not available when the Ethernet is being used.
9. For the LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 and BGA100 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.

Table 17. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Run mode	External clock(3)	72 MHz	47.3	28.3	mA
			48 MHz	32	19.6	
			36 MHz	24.6	15.4	
			24 MHz	16.8	10.6	
			16 MHz	11.8	7.4	
			8 MHz	5.9	3.7	
			4 MHz	3.7	2.9	
			2 MHz	2.5	2	
			1 MHz	1.8	1.53	
			500 kHz	1.5	1.3	
			125 kHz	1.3	1.2	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	36 MHz	23.9	14.8	mA
			24 MHz	16.1	9.7	
			16 MHz	11.1	6.7	
			8 MHz	5.6	3.8	
			4 MHz	3.1	2.1	
			2 MHz	1.8	1.3	
			1 MHz	1.16	0.9	
			500 kHz	0.8	0.67	
			125 kHz	0.6	0.5	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

5.3.7 Internal clock source characteristics

The parameters given in *Table 24* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

High-speed internal (HSI) RC oscillator

Table 24. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	8		MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register(2)		-	-	1(3)	%
		Factory-calibrated(4)	T_A = –40 to 105 °C	–2	-	2.5	%
			T_A = –10 to 85 °C	–1.5	-	2.2	%
			T_A = 0 to 70 °C	–1.3	-	2	%
			T_A = 25 °C	–1.1	-	1.8	%
$t_{su(HSI)}$(4)	HSI oscillator startup time	-		1	-	2	µs
$I_{DD(HSI)}$(4)	HSI oscillator power consumption	-		-	80	100	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Refer to application note AN2868 “STM32F10xxx internal RC oscillator (HSI) calibration” available from the ST website *www.st.com*.
3. Guaranteed by design, not tested in production.
4. Based on characterization, not tested in production.

Low-speed internal (LSI) RC oscillator

Table 25. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	30	40	60	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.65	1.2	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in *Table 26* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

A device reset allows normal operations to be resumed.

The test results are given in *Table 31*. They are based on the EMS levels and classes defined in application note AN1709.

Table 31. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 72 MHz, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 72 MHz, conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

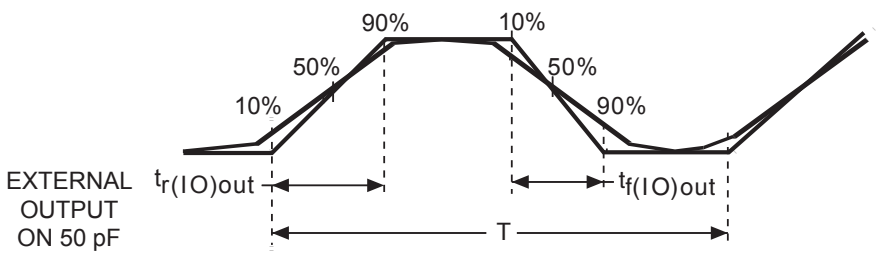
Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC61967-2 standard which specifies the test board and the pin loading.

Figure 22. I/O AC characteristics definition



Maximum frequency is achieved if (t_r + t_f) < (2/3)T and if the duty cycle is (45-55%) when loaded by 50 pF

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5.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 36*).

Unless otherwise specified, the parameters given in *Table 39* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 39. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	–0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	V_{DD} > 2.7 V	300	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

I^2S - SPI interface characteristics

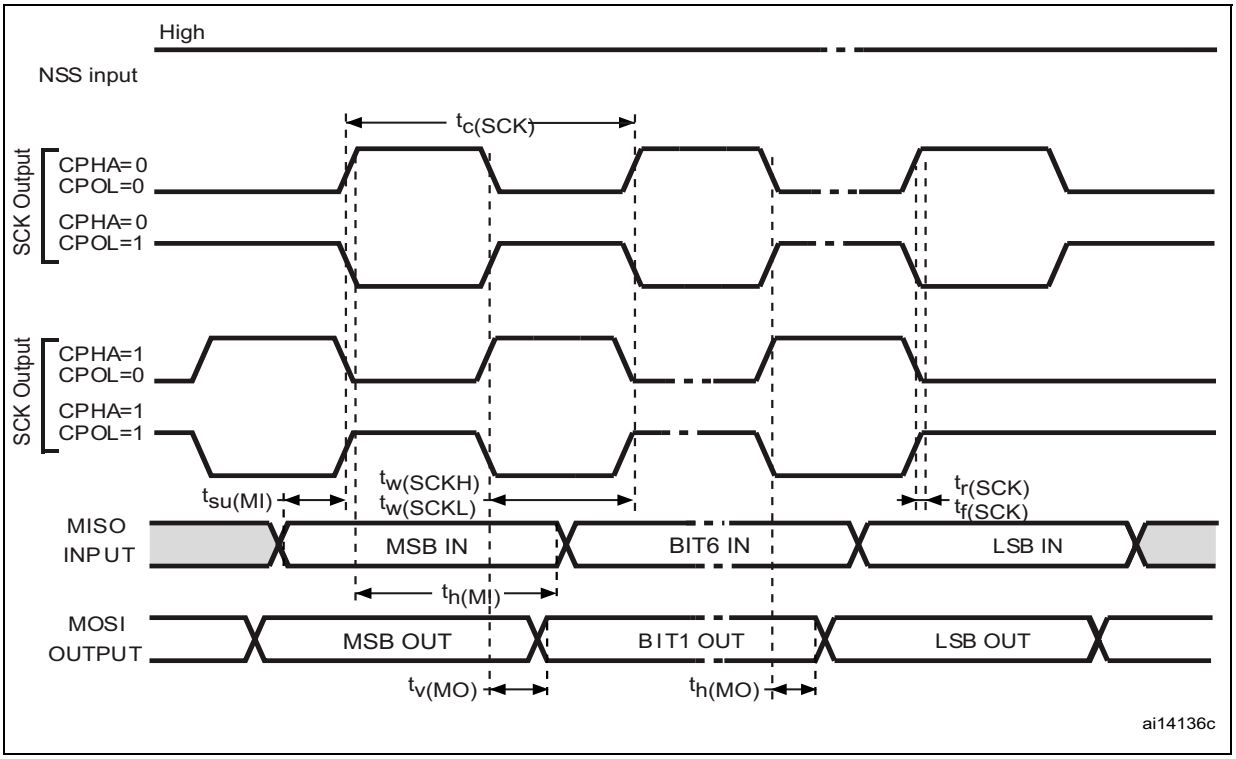
Unless otherwise specified, the parameters given in *Table 43* for SPI or in *Table 44* for I^2S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

Refer to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I^2S).

Table 43. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode	4 t_{PCLK}	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2 t_{PCLK}	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	50	60	
$t_{su(MI)}$	Data input setup time	Master mode	4	-	
$t_{su(SI)}$		Slave mode	5	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	
$t_{h(SI)}$		Slave mode	5	-	
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK} = 20 MHz	-	3*t_{PCLK}	
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	-	34	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	8	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	32	-	
$t_{h(MO)}$		Master mode (after enable edge)	10	-	

Figure 27. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 50 gives the list of Ethernet MAC signals for the RMII and *Figure 32* shows the corresponding timing diagram.

Figure 32. Ethernet RMII timing diagram

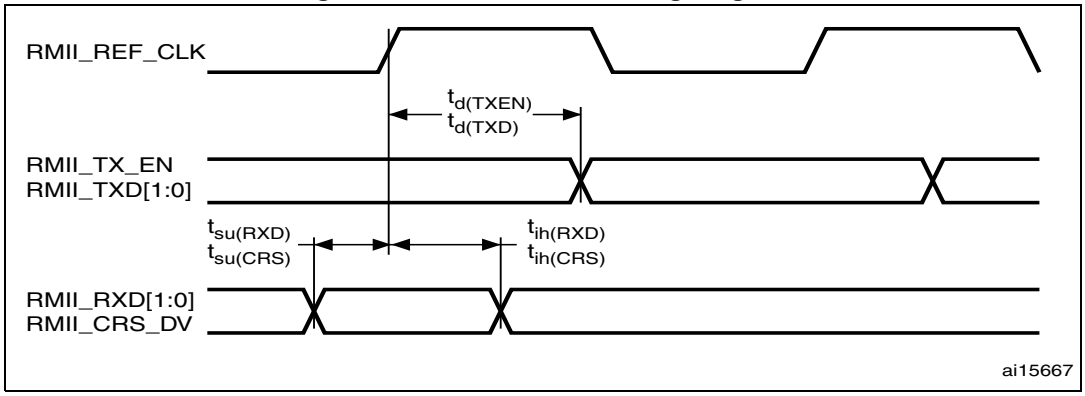


Table 50. Dynamic characteristics: Ethernet MAC signals for RMII

Symbol	Rating	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	4	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	2	-	-	ns
$t_{su(DV)}$	Carrier sense set-up time	4	-	-	ns
$t_{ih(DV)}$	Carrier sense hold time	2	-	-	ns
$t_{d(TXEN)}$	Transmit enable valid delay time	8	10	16	ns
$t_{d(TXD)}$	Transmit data valid delay time	7	10	16	ns

Table 51 gives the list of Ethernet MAC signals for MII and *Figure 32* shows the corresponding timing diagram.

Figure 33. Ethernet MII timing diagram

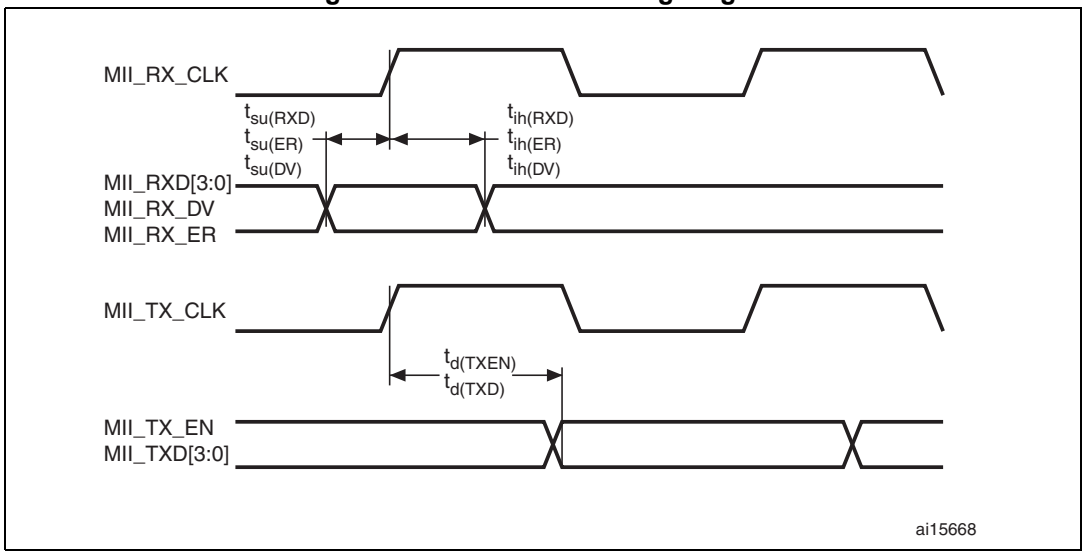


Table 51. Dynamic characteristics: Ethernet MAC signals for MII

Symbol	Rating	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	10	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	10	-	-	ns
$t_{su(DV)}$	Data valid setup time	10	-	-	ns
$t_{ih(DV)}$	Data valid hold time	10	-	-	ns
$t_{su(ER)}$	Error setup time	10	-	-	ns
$t_{ih(ER)}$	Error hold time	10	-	-	ns
$t_{d(TXEN)}$	Transmit enable valid delay time	14	16	18	ns
$t_{d(TXD)}$	Transmit data valid delay time	13	16	20	ns

CAN (controller area network) interface

Refer to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (CANTX and CANRX).

5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 52* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 9*.

Note: It is recommended to perform a calibration after each power-up.

Table 52. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin	-	-	160(1)	220(1)	µA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(2)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 53* for details	-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$

Table 54. ADC accuracy - limited test conditions(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 V to 3.6 V T_A = 25 °C Measurements made after ADC calibration	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	

1. ADC DC accuracy values are measured after internal calibration.
2. Based on characterization, not tested in production.

Table 55. ADC accuracy(1) (2)

Symbol	Parameter	Test conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

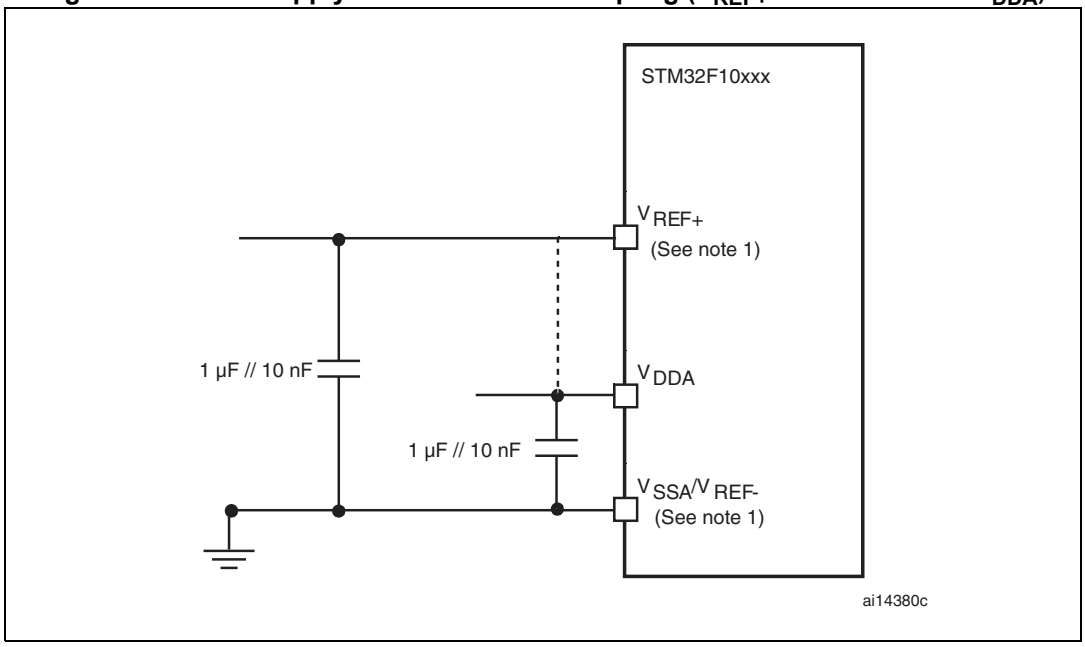
1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
3. Based on characterization, not tested in production.

Note: ADC accuracy vs. negative injection current: Injecting a negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative currents.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.

General PCB design guidelines

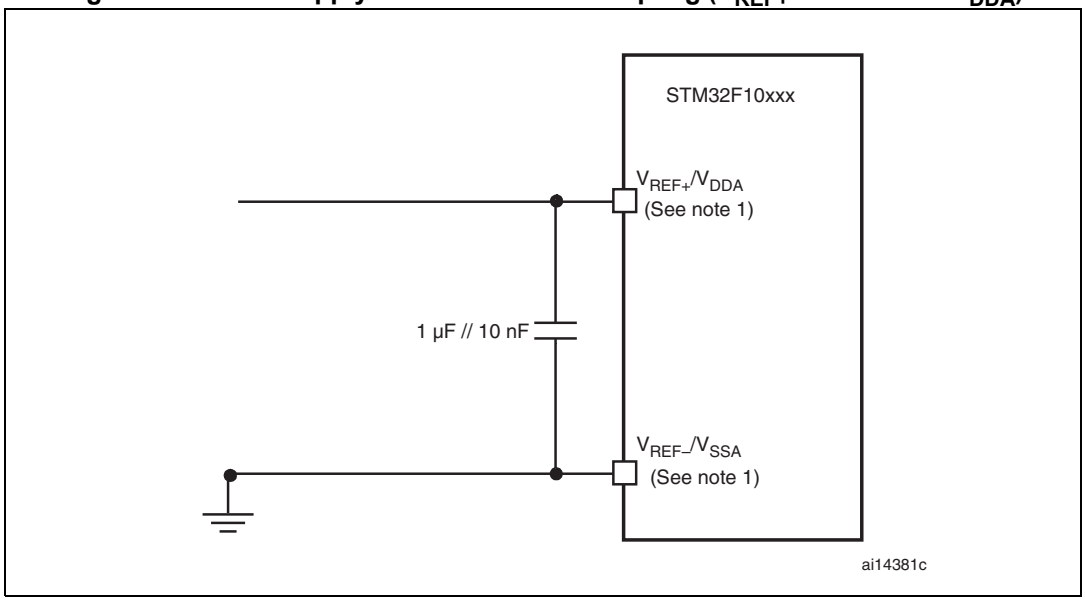
Power supply decoupling should be performed as shown in *Figure 36* or *Figure 37*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 36. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and $V_{REF–}$ inputs are available only on 100-pin packages.

Figure 37. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and $V_{REF–}$ inputs are available only on 100-pin packages.

Figure 40. LFBGA100 – 100-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Typ	Min	Max
A	-	-	1.700	-	-	0.0669
A1	0.270	-	-	0.0106	-	-
A2	-	0.300	-	-	0.0118	-
A4	-	-	0.800	-	-	0.0315
b	0.450	0.500	0.550	0.0177	0.0197	0.0217
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	7.200	-	-	0.2835	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	7.200	-	-	0.2835	-
e	-	0.800	-	-	0.0315	-
F	-	1.400	-	-	0.0551	-
ddd	-	-	0.120	-	-	0.0047
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 41. LFBGA100 – 100-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package recommended footprint

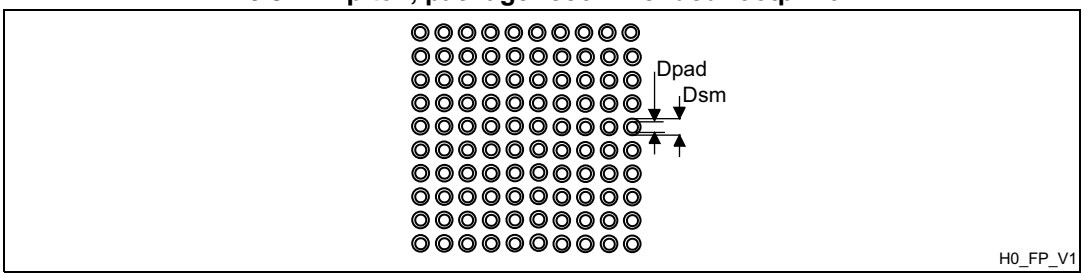


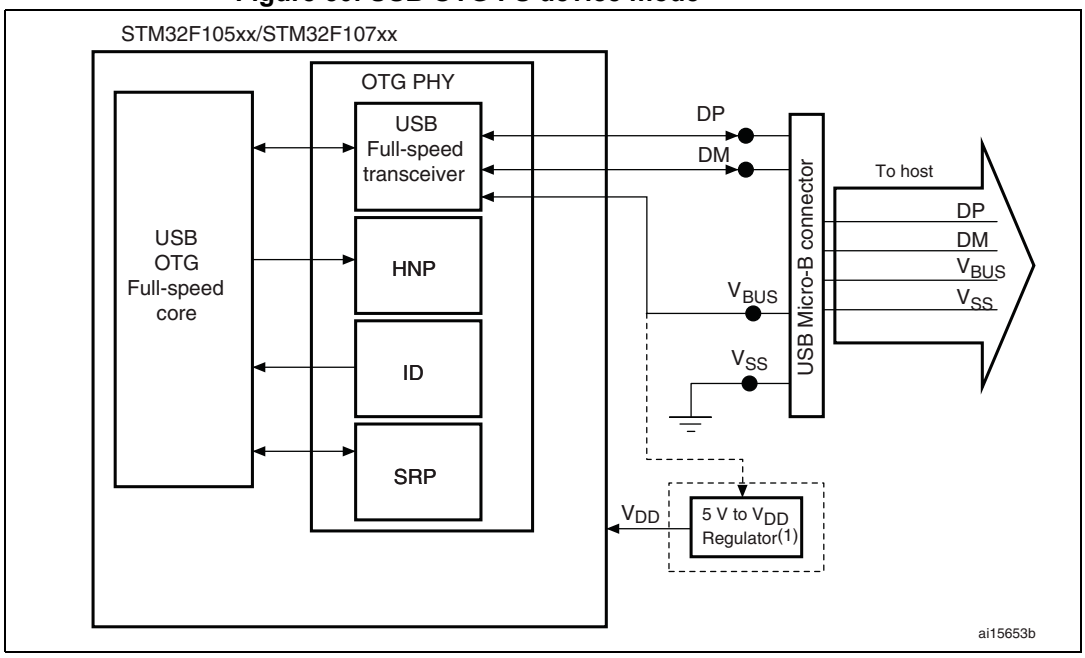
Table 58. LFBGA100 recommended PCB design rules (0.8 mm pitch BGA)

Dimension	Recommended values
Pitch	0.8
Dpad	0.500 mm
Dsm	0.570 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.500 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

Appendix A Application block diagrams

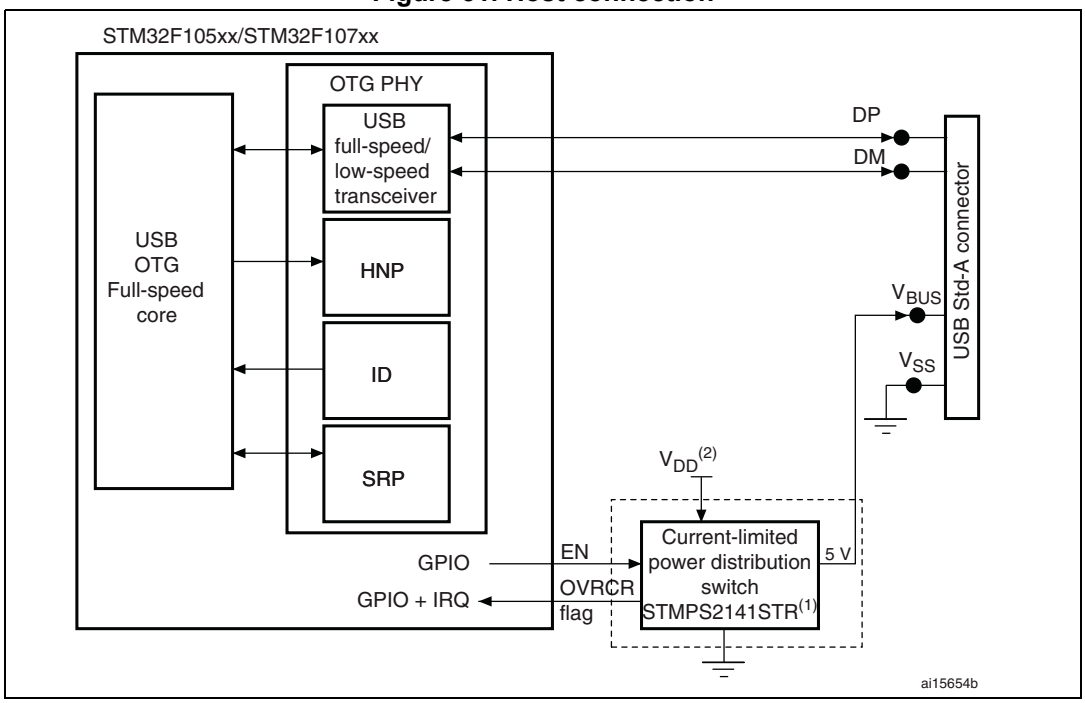
A.1 USB OTG FS interface solutions

Figure 50. USB OTG FS device mode



1. Use a regulator if you want to build a bus-powered device.

Figure 51. Host connection

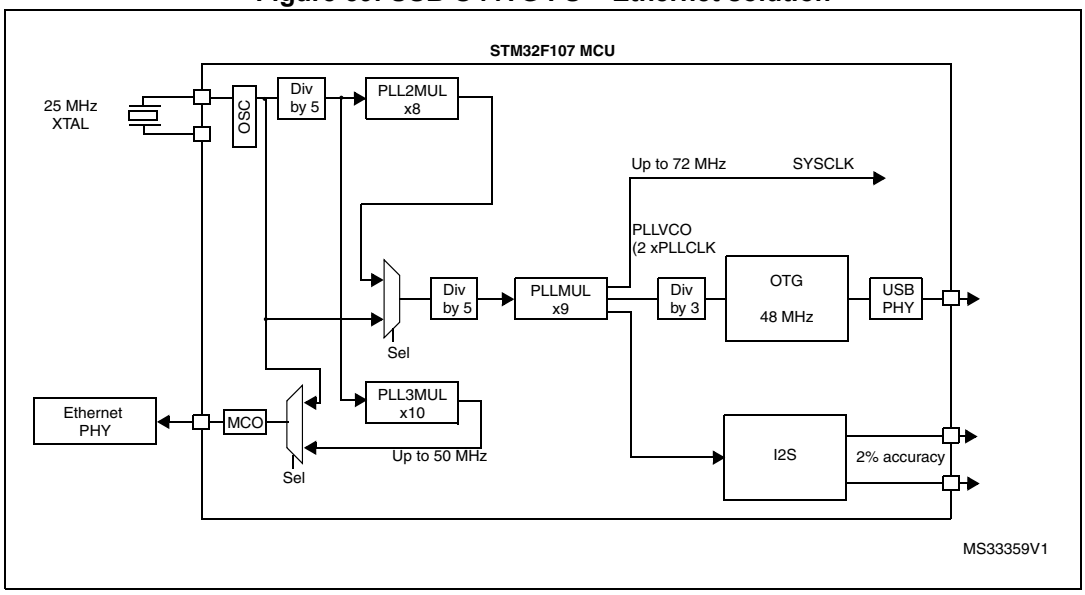


1. STMPS2141STR needed only if the application has to support bus-powered devices.

A.4 USB OTG FS interface + Ethernet/I²S interface solutions

With the clock tree implemented on the STM32F107xx, only one crystal is required to work with both the USB (host/device/OTG) and the Ethernet (MII/RMII) interfaces. *Figure 59* illustrate the solution.

Figure 59. USB O44TG FS + Ethernet solution



With the clock tree implem1ented on the STM32F107xx, only one crystal is required to work with both the USB (host/device/OTG) and the I²S (Audio) interfaces. *Figure 60* illustrate the solution.

Figure 60. USB OTG FS + I²S (Audio) solution

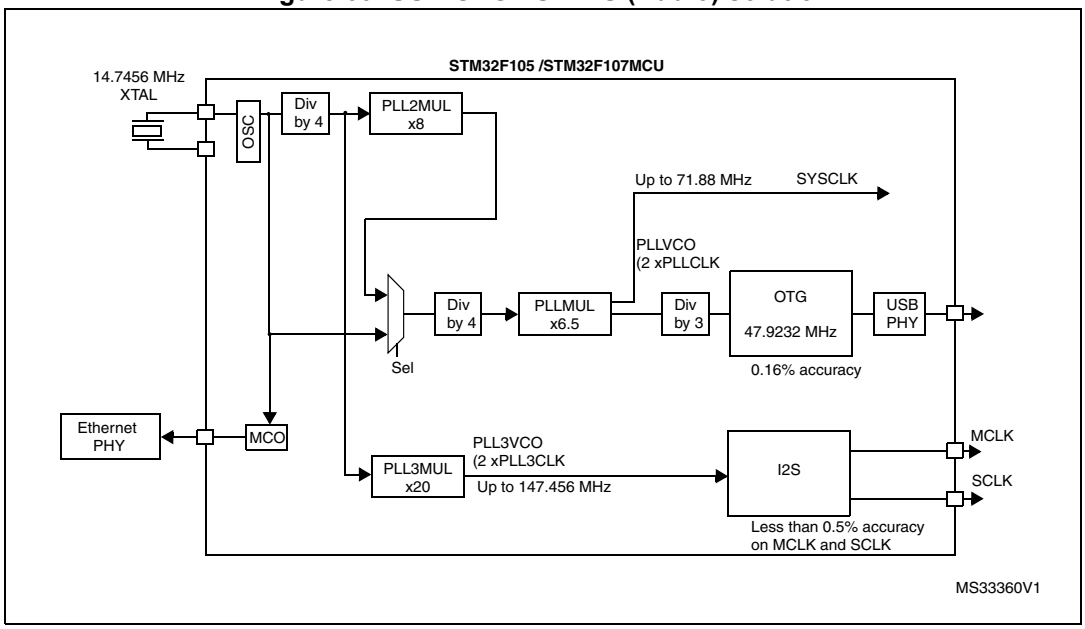


Table 63. PLL configurations

Application	Crystal value in MHz (XT1)	PREDIV2	PLL2MUL	PLLSRC	PREDIV1	PLLMUL	USB prescaler (PLLVCO output)	PLL3MUL	I2Sn clock input	MCO (main clock output)
Ethernet only	25	/5	PLL2ON x8	PLL2	/5	PLLON x9	NA	PLL3ON x10	NA	XT1 (MII) PLL3 (RMII)
Ethernet + OTG	25	/5	PLL2ON x8	PLL2	/5	PLLON x9	/3	PLL3ON x10	NA	XT1 (MII) PLL3 (RMII)
Ethernet + OTG + basic audio	25	/5	PLL2ON x8	PLL2	/5	PLLON x9	/3	PLL3ON x10	PLL	XT1 (MII) PLL3 (RMII)
Ethernet + OTG + Audio class I^2S(1)	14.7456	/4	PLL2ON x12	PLL2	/4	PLLON x6.5	/3	PLL3ON x20	PLL3 VCO Out	NA ETH PHY must use its own crystal
OTG only	8	NA	PLL2OFF	XT1	/1	PLLON x9	/3	PLL3OFF	NA	NA
OTG + basic audio	8	NA	PLL2OFF	XT1	/1	PLLON x9	/3	PLL3OFF	PLL	NA
OTG + Audio class I^2S(1)	14.7456	/4	PLL2ON x12	PLL2	/4	PLLON x6.5	/3	PLL3ON x20	PLL3 VCO Out	NA
Audio class I^2S only(1)	14.7456	/4	PLL2ON x12	PLL2	/4	PLLON x6.5	NA	PLL3ON x20	PLL3 VCO out	NA

1. SYSCLK is set to be at 72 MHz except in this case where SYSCLK is at 71.88 MHz.

Table 64 give the I_{DD} run mode values that correspond to the conditions specified in *Table 63*.