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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG |
| Peripherals | DMA, POR, PWM, Voltage Detect, WDT |
| Number of I/O | 51 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f105rct6v |

# Contents

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# 2 Description

The STM32F105xx and STM32F107xx connectivity line family incorporates the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 256 Kbytes and SRAM 64 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, four general-purpose 16-bit timers plus a PWM timer, as well as standard and advanced communication interfaces: up to two $I^2C$s, three SPIs, two I2Ss, five USARTs, an USB OTG FS and two CANs. Ethernet is available on the STM32F107xx only.

The STM32F105xx and STM32F107xx connectivity line family operates in the –40 to +105 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F105xx and STM32F107xx connectivity line family offers devices in three different package types: from 64 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F105xx and STM32F107xx connectivity line microcontroller family suitable for a wide range of applications such as motor drives and application control, medical and handheld equipment, industrial applications, PLCs, inverters, printers, and scanners, alarm systems, video intercom, HVAC and home audio equipment.

## 2.1 Device overview

*Figure 1* shows the general block diagram of the device family.

**Table 2. STM32F105xx and STM32F107xx features and peripheral counts**

| Peripherals[1] | | STM32F105Rx | | | STM32F107Rx | | STM32F105Vx | | | STM32F107Vx | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Flash memory in Kbytes | | 64 | 128 | 256 | 128 | 256 | 64 | 128 | 256 | 128 | 256 |
| SRAM in Kbytes | | 64 | | | | | | | | | |
| Package | | LQFP64 | | | | | LQFP 100 | LQFP 100, BGA 100 | LQFP 100 | LQFP 100 | LQFP 100, BGA 100 |
| Ethernet | | No | | | Yes | | No | | | Yes | |
| Timers | General-purpose | 4 | | | | | | | | | |
| | Advanced-control | 1 | | | | | | | | | |
| | Basic | 2 | | | | | | | | | |

- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes, that is 4 Kbytes in total
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 with the timestamp comparator connected to the TIM2 trigger input
- Triggers interrupt when system time becomes greater than target time

### 2.3.21 Controller area network (CAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). The 256 bytes of SRAM which are allocated for each CAN (512 bytes in total) are not shared with any other peripheral.

### 2.3.22 Universal serial bus on-the-go full-speed (USB OTG FS)

The STM32F105xx and STM32F107xx connectivity line devices embed a USB OTG full-speed (12 Mb/s) device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- 1.25 KB of SRAM used exclusively by the endpoints (not shared with any other peripheral)
- 4 bidirectional endpoints
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected
- the SOF output can be used to synchronize the external audio DAC clock in isochronous mode
- in accordance with the USB 2.0 Specification, the supported transfer speeds are:
  - in Host mode: full speed and low speed
  - in Device mode: full speed

### 2.3.23 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

I/Os on APB2 with up to 18 MHz toggling speed

### 2.3.24 Remap capability

This feature allows the use of a maximum number of peripherals in a given application. Indeed, alternate functions are available not only on the default pins but also on other specific pins onto which they are remappable. This has the advantage of making board design and port usage much more flexible.

For details refer to *Table 5: Pin definitions*; it shows the list of remappable alternate functions and the pins onto which they can be remapped. See the STM32F10xxx reference manual for software considerations.

### 2.3.25 ADCs (analog-to-digital converters)

Two 12-bit analog-to-digital converters are embedded into STM32F105xx and STM32F107xx connectivity line devices and each ADC shares up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single shunt

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the standard timers (TIMx) and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

### 2.3.26 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference $V_{REF+}$

Eight DAC trigger inputs are used in the STM32F105xx and STM32F107xx connectivity line family. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

### 2.3.27 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < $V_{DDA}$ < 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

### 2.3.28 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

### 2.3.29 Embedded Trace Macrocell™

The ARM® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F10xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

# 3 Pinouts and pin description

**Figure 2. STM32F105xx and STM32F107xx connectivity line BGA100 ballout top view**

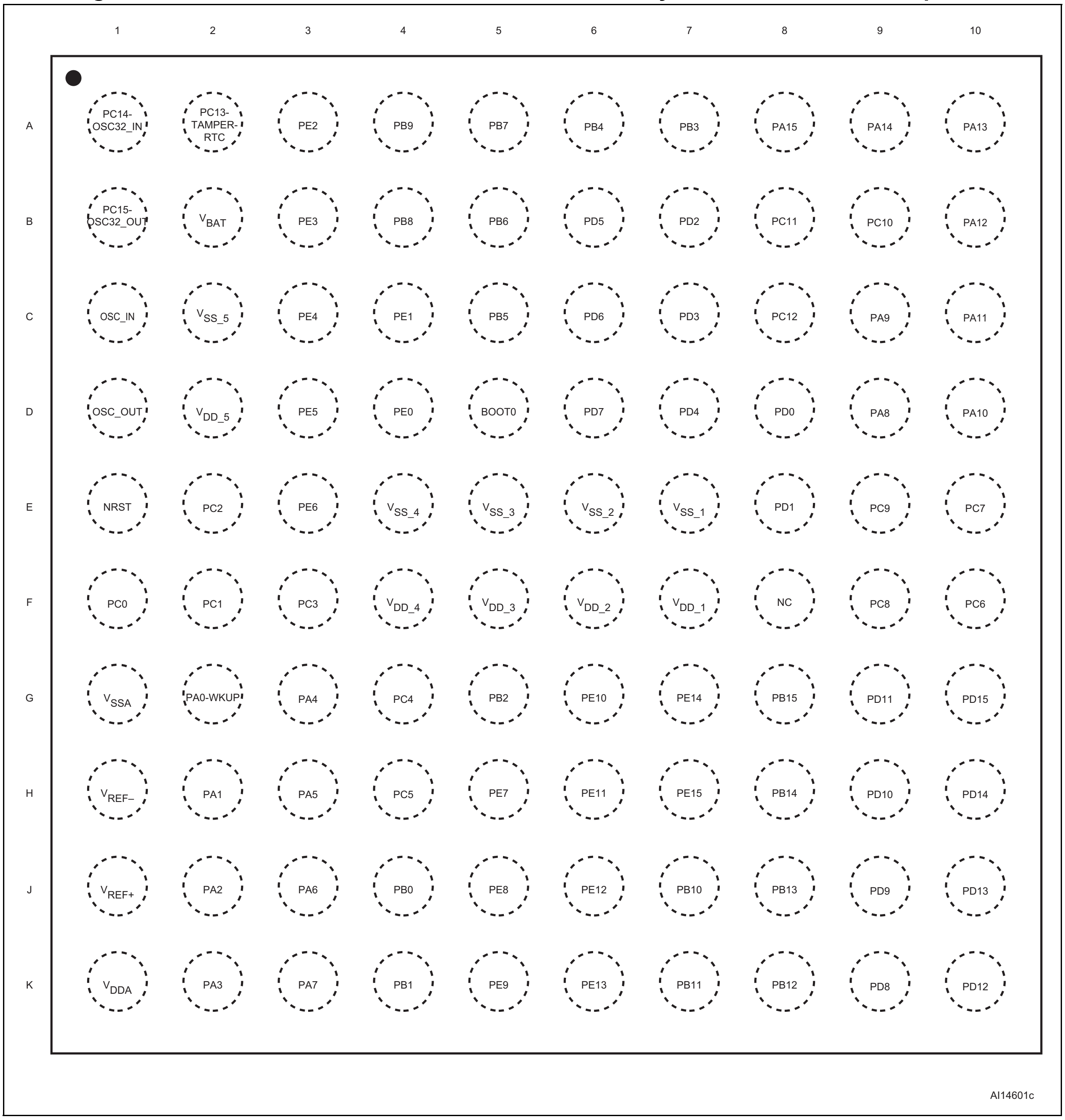


Table 5. Pin definitions (continued)

| Pins | | | Pin name | Type(1) | I / O Level(2) | Main function(3) (after reset) | Alternate functions(4) | |
|---|---|---|---|---|---|---|---|---|
| BGA100 | LQFP64 | LQFP100 | | | | | Default | Remap |
| H2 | 15 | 24 | PA1 | I/O | - | PA1 | USART2_RTS(7)/ ADC12_IN1/ TIM5_CH2 /TIM2_CH2(7)/ ETH_MII_RX_CLK/ ETH_RMII_REF_CLK | - |
| J2 | 16 | 25 | PA2 | I/O | - | PA2 | USART2_TX(7)/ TIM5_CH3/ADC12_IN2/ TIM2_CH3 (7)/ ETH_MII_MDIO/ ETH_RMII_MDIO | - |
| K2 | 17 | 26 | PA3 | I/O | - | PA3 | USART2_RX(7)/ TIM5_CH4/ADC12_IN3 / TIM2_CH4(7)/ ETH_MII_COL | - |
| E4 | 18 | 27 | $V_{SS\_4}$ | S | - | $V_{SS\_4}$ | - | - |
| F4 | 19 | 28 | $V_{DD\_4}$ | S | - | $V_{DD\_4}$ | - | - |
| G3 | 20 | 29 | PA4 | I/O | - | PA4 | SPI1_NSS(7)/DAC_OUT1 / USART2_CK(7) / ADC12_IN4 | SPI3_NSS/I2S3_WS |
| H3 | 21 | 30 | PA5 | I/O | - | PA5 | SPI1_SCK(7) / DAC_OUT2 / ADC12_IN5 | - |
| J3 | 22 | 31 | PA6 | I/O | - | PA6 | SPI1_MISO(7)/ADC12_IN6 / TIM3_CH1(7) | TIM1_BKIN |
| K3 | 23 | 32 | PA7 | I/O | - | PA7 | SPI1_MOSI(7)/ADC12_IN7 / TIM3_CH2(7)/ ETH_MII_RX_DV(8)/ ETH_RMII_CRS_DV | TIM1_CH1N |
| G4 | 24 | 33 | PC4 | I/O | - | PC4 | ADC12_IN14/ ETH_MII_RXD0(8)/ ETH_RMII_RXD0 | - |
| H4 | 25 | 34 | PC5 | I/O | - | PC5 | ADC12_IN15/ ETH_MII_RXD1(8)/ ETH_RMII_RXD1 | - |
| J4 | 26 | 35 | PB0 | I/O | - | PB0 | ADC12_IN8/TIM3_CH3/ ETH_MII_RXD2(8) | TIM1_CH2N |
| K4 | 27 | 36 | PB1 | I/O | - | PB1 | ADC12_IN9/TIM3_CH4(7)/ ETH_MII_RXD3(8) | TIM1_CH3N |
| G5 | 28 | 37 | PB2 | I/O | FT | PB2/BOOT1 | - | - |
| H5 | - | 38 | PE7 | I/O | FT | PE7 | - | TIM1_ETR |
| J5 | - | 39 | PE8 | I/O | FT | PE8 | - | TIM1_CH1N |

**Table 5. Pin definitions (continued)**

| Pins | | | Pin name | Type[1] | I / O Level[2] | Main function[3] (after reset) | Alternate functions[4] | |
|---|---|---|---|---|---|---|---|---|
| BGA100 | LQFP64 | LQFP100 | | | | | Default | Remap |
| J9 | - | 56 | PD9 | I/O | FT | PD9 | - | USART3_RX/ ETH_MII_RXD0/ ETH_RMII_RXD0 |
| H9 | - | 57 | PD10 | I/O | FT | PD10 | - | USART3_CK/ ETH_MII_RXD1/ ETH_RMII_RXD1 |
| G9 | - | 58 | PD11 | I/O | FT | PD11 | - | USART3_CTS/ ETH_MII_RXD2 |
| K10 | - | 59 | PD12 | I/O | FT | PD12 | - | TIM4_CH1 / USART3_RTS/ ETH_MII_RXD3 |
| J10 | - | 60 | PD13 | I/O | FT | PD13 | - | TIM4_CH2 |
| H10 | - | 61 | PD14 | I/O | FT | PD14 | - | TIM4_CH3 |
| G10 | - | 62 | PD15 | I/O | FT | PD15 | - | TIM4_CH4 |
| F10 | 37 | 63 | PC6 | I/O | FT | PC6 | I2S2_MCK/ | TIM3_CH1 |
| E10 | 38 | 64 | PC7 | I/O | FT | PC7 | I2S3_MCK | TIM3_CH2 |
| F9 | 39 | 65 | PC8 | I/O | FT | PC8 | - | TIM3_CH3 |
| E9 | 40 | 66 | PC9 | I/O | FT | PC9 | - | TIM3_CH4 |
| D9 | 41 | 67 | PA8 | I/O | FT | PA8 | USART1_CK/OTG_FS_SOF / TIM1_CH1[8]/MCO | - |
| C9 | 42 | 68 | PA9 | I/O | FT | PA9 | USART1_TX[7]/ TIM1_CH2[7]/ OTG_FS_VBUS | - |
| D10 | 43 | 69 | PA10 | I/O | FT | PA10 | USART1_RX[7]/ TIM1_CH3[7]/OTG_FS_ID | - |
| C10 | 44 | 70 | PA11 | I/O | FT | PA11 | USART1_CTS / CAN1_RX / TIM1_CH4[7]/OTG_FS_DM | - |
| B10 | 45 | 71 | PA12 | I/O | FT | PA12 | USART1_RTS / OTG_FS_DP / CAN1_TX[7] / TIM1_ETR[7] | - |
| A10 | 46 | 72 | PA13 | I/O | FT | JTMS-SWDIO | - | PA13 |
| F8 | - | 73 | Not connected | | | | | - |
| E6 | 47 | 74 | $V_{SS\_2}$ | S | - | $V_{SS\_2}$ | - | - |
| F6 | 48 | 75 | $V_{DD\_2}$ | S | - | $V_{DD\_2}$ | - | - |
| A9 | 49 | 76 | PA14 | I/O | FT | JTCK-SWCLK | - | PA14 |

**Table 15. Maximum current consumption in Sleep mode, code running from Flash or RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Max(1) | | Unit |
|---|---|---|---|---|---|---|
| | | | | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Sleep mode | External clock(2), all peripherals enabled | 72 MHz | 48.4 | 49 | mA |
| | | | 48 MHz | 33.9 | 34.4 | |
| | | | 36 MHz | 26.7 | 27.2 | |
| | | | 24 MHz | 19.3 | 19.8 | |
| | | | 16 MHz | 14.2 | 14.8 | |
| | | | 8 MHz | 8.7 | 9.1 | |
| | | External clock(2), all peripherals disabled | 72 MHz | 10.1 | 10.6 | |
| | | | 48 MHz | 8.3 | 8.75 | |
| | | | 36 MHz | 7.5 | 8 | |
| | | | 24 MHz | 6.6 | 7.1 | |
| | | | 16 MHz | 6 | 6.5 | |
| | | | 8 MHz | 2.5 | 3 | |

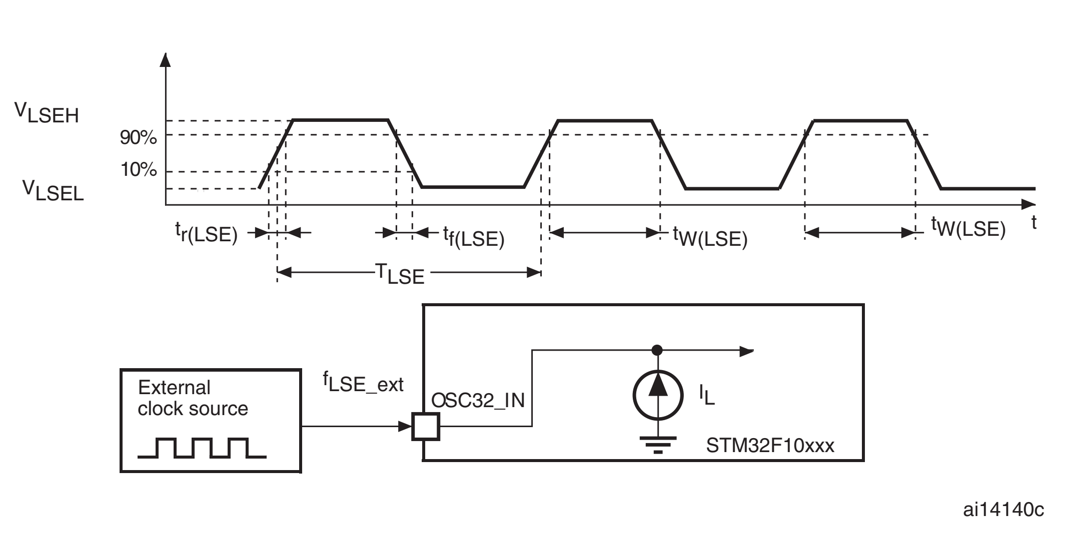
1. Based on characterization, tested in production at $V_{DD}$ max and $f_{HCLK}$ max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when $f_{HCLK}$ > 8 MHz.

**Table 16. Typical and maximum current consumptions in Stop and Standby modes**

| Symbol | Parameter | Conditions | Typ(1) | | | Max | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{DD}/V_{BAT}$ = 2.0 V | $V_{DD}/V_{BAT}$ = 2.4 V | $V_{DD}/V_{BAT}$ = 3.3 V | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Stop mode | Regulator in Run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | - | 32 | 33 | 600 | 1300 | µA |
| | | Regulator in Low Power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | - | 25 | 26 | 590 | 1280 | |
| | Supply current in Standby mode | Low-speed internal RC oscillator and independent watchdog ON | - | 3 | 3.8 | - | - | |
| | | Low-speed internal RC oscillator ON, independent watchdog OFF | - | 2.8 | 3.6 | - | - | |
| | | Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF | - | 1.9 | 2.1 | 5(2) | 6.5(2) | |
| $I_{DD\_VBAT}$ | Backup domain supply current | Low-speed oscillator and RTC ON | 1.1 | 1.2 | 1.4 | 2.1(2) | 2.3(2) | |

1. Typical values are measured at $T_A$ = 25 °C.
2. Based on characterization, not tested in production.

**Figure 15. Low-speed external clock source AC timing diagram**




## High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 3 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 22*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

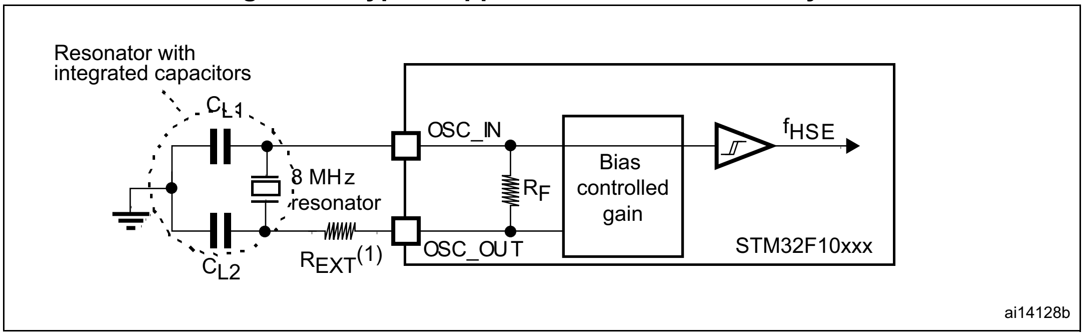
**Table 22. HSE 3-25 MHz oscillator characteristics(1) (2)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{OSC\_IN}$ | Oscillator frequency | - | 3 | | 25 | MHz |
| $R_F$ | Feedback resistor | - | - | 200 | - | kΩ |
| C | Recommended load capacitance versus equivalent serial resistance of the crystal ($R_S$)(3) | $R_S$ = 30 Ω | - | 30 | - | pF |
| $i_2$ | HSE driving current | $V_{DD}$ = 3.3 V, $V_{IN} = V_{SS}$ with 30 pF load | - | - | 1 | mA |
| $g_m$ | Oscillator transconductance | Startup | 25 | - | - | mA/V |
| $t_{SU(HSE)}$(4) | Startup time | $V_{DD}$ is stabilized | - | 2 | - | ms |

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization, not tested in production.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 16*). $C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing $C_{L1}$ and $C_{L2}$. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

**Figure 16. Typical application with an 8 MHz crystal**




1. $R_{EXT}$ value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 23*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 23. LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz) (1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_F$ | Feedback resistor | - | - | 5 | - | MΩ |
| C(2) | Recommended load capacitance versus equivalent serial resistance of the crystal ($R_S$)(3) | $R_S$ = 30 kΩ | - | - | 15 | pF |
| $I_2$ | LSE driving current | $V_{DD}$ = 3.3 V, $V_{IN}$ = $V_{SS}$ | - | - | 1.4 | µA |
| $g_m$ | Oscillator Transconductance | - | 5 | - | - | µA/V |

A device reset allows normal operations to be resumed.

The test results are given in *Table 31*. They are based on the EMS levels and classes defined in application note AN1709.

**Table 31. EMS characteristics**

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP100, $T_A$ = +25 °C, $f_{HCLK}$ = 72 MHz, conforms to IEC 61000-4-2 | 2B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP100, $T_A$ = +25 °C, $f_{HCLK}$ = 72 MHz, conforms to IEC 61000-4-4 | 4A |

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

#### Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

#### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC61967-2 standard which specifies the test board and the pin loading.

### $I^2S$ - SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 43* for SPI or in *Table 44* for $I^2S$ are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

Refer to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for $I^2S$).

**Table 43. SPI characteristics**

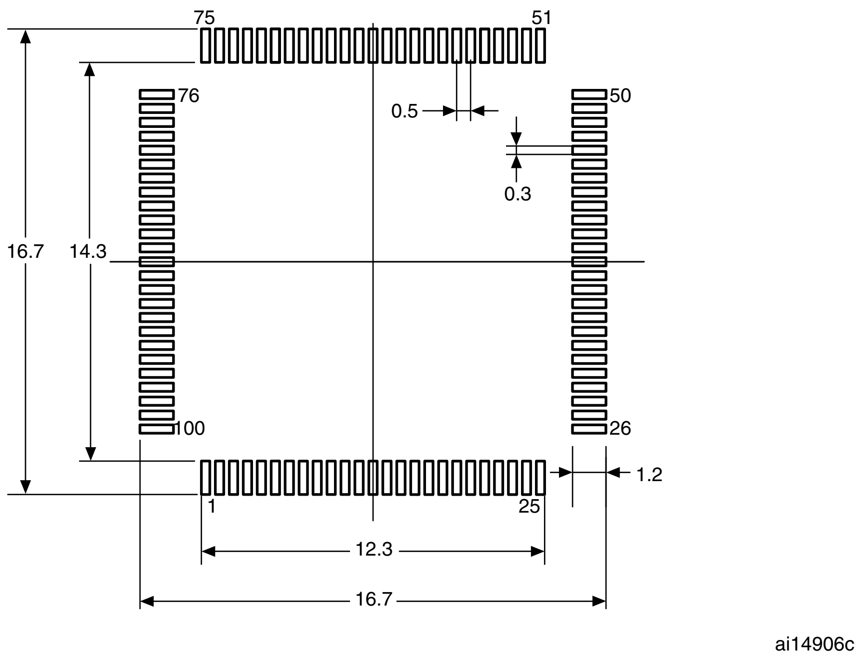
| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$ $1/t_{c(SCK)}$ | SPI clock frequency | Master mode | - | 18 | MHz |
| | | Slave mode | - | 18 | |
| $t_{r(SCK)}$ $t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load: C = 30 pF | - | 8 | ns |
| DuCy(SCK) | SPI slave input clock duty cycle | Slave mode | 30 | 70 | % |
| $t_{su(NSS)}$ | NSS setup time | Slave mode | 4 $t_{PCLK}$ | - | ns |
| $t_{h(NSS)}$ | NSS hold time | Slave mode | 2 $t_{PCLK}$ | - | |
| $t_{w(SCKH)}$ $t_{w(SCKL)}$ | SCK high and low time | Master mode, $f_{PCLK}$ = 36 MHz, presc = 4 | 50 | 60 | |
| $t_{su(MI)}$ | Data input setup time | Master mode | 4 | - | |
| $t_{su(SI)}$ | | Slave mode | 5 | - | |
| $t_{h(MI)}$ | Data input hold time | Master mode | 5 | - | |
| $t_{h(SI)}$ | | Slave mode | 5 | - | |
| $t_{a(SO)}$ | Data output access time | Slave mode, $f_{PCLK}$ = 20 MHz | - | $3*t_{PCLK}$ | |
| $t_{v(SO)}$ | Data output valid time | Slave mode (after enable edge) | - | 34 | |
| $t_{v(MO)}$ | Data output valid time | Master mode (after enable edge) | - | 8 | |
| $t_{h(SO)}$ | Data output hold time | Slave mode (after enable edge) | 32 | - | |
| $t_{h(MO)}$ | | Master mode (after enable edge) | 10 | - | |

Table 59. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| E3 | - | 12.000 | - | - | 0.4724 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0.0° | 3.5° | 7.0° | 0.0° | 3.5° | 7.0° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint



## 6.4 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 9: General operating conditions on page 37*.

The maximum chip-junction temperature, $T_J$ max, in degrees Celsius, may be calculated using the following equation:

$$T_J \max = T_A \max + (P_D \max \times \Theta_{JA})$$

Where:

- $T_A$ max is the maximum ambient temperature in °C,
- $\Theta_{JA}$ is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D$ max is the sum of $P_{INT}$ max and $P_{I/O}$ max ($P_D$ max = $P_{INT}$ max + $P_{I/O}$max),
- $P_{INT}$ max is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \max = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual $V_{OL}$ / $I_{OL}$ and $V_{OH}$ / $I_{OH}$ of the I/Os at low and high level in the application.

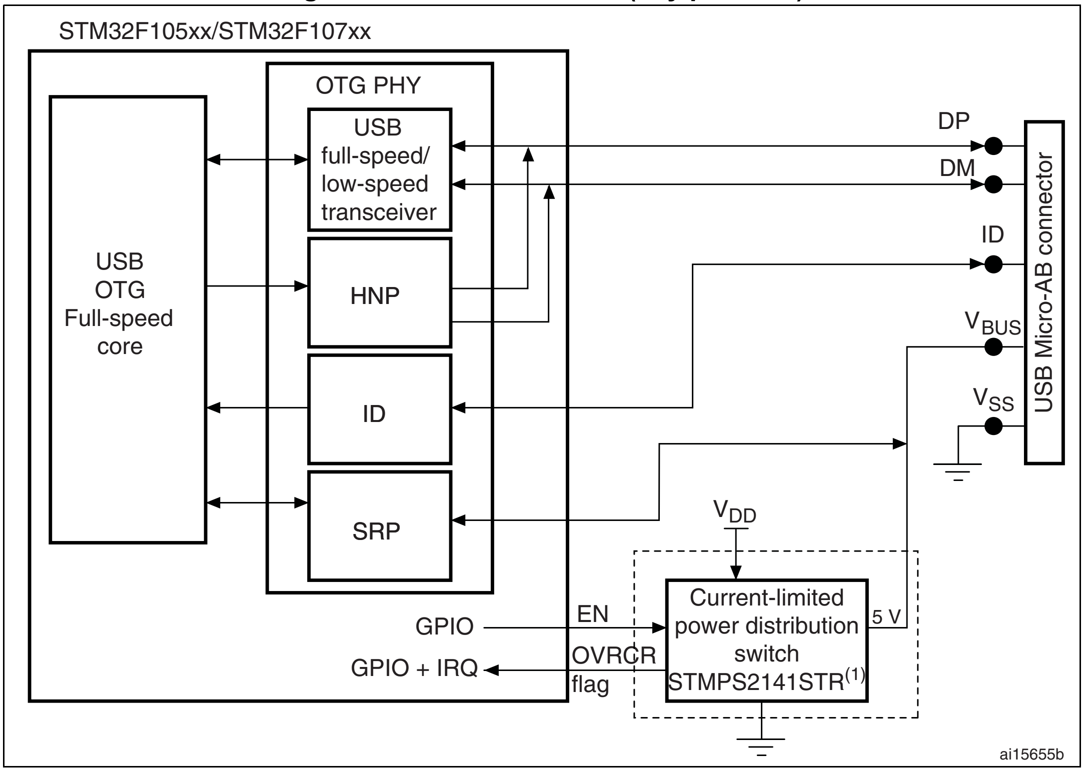
**Table 61. Package thermal characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | **Thermal resistance junction-ambient**<br>LQFP100 - 14 × 14 mm / 0.5 mm pitch | 46 | °C/W |
| | **Thermal resistance junction-ambient**<br>LQFP64 - 10 × 10 mm / 0.5 mm pitch | 45 | |
| $\Theta_{JA}$ | **Thermal resistance junction-ambient**<br>LFBGA100 - 10 × 10 mm / 0.8 mm pitch | 40 | °C/W |
| | **Thermal resistance junction-ambient**<br>LQFP100 - 14 × 14 mm / 0.5 mm pitch | 46 | |
| | **Thermal resistance junction-ambient**<br>LQFP64 - 10 × 10 mm / 0.5 mm pitch | 45 | |

### 6.4.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

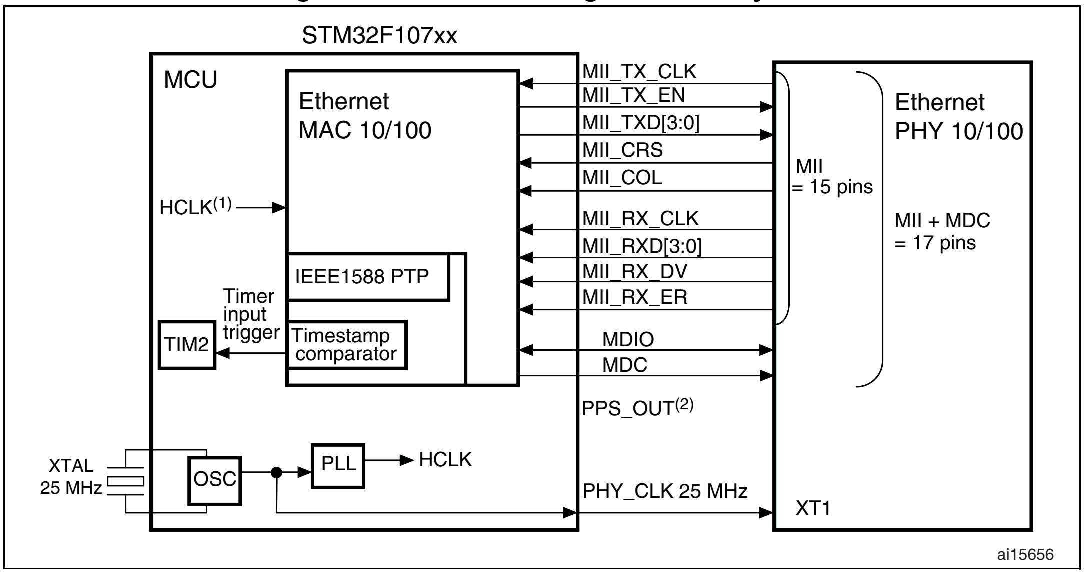
**Figure 52. OTG connection (any protocol)**




1. STMPS2141STR needed only if the application has to support bus-powered devices.

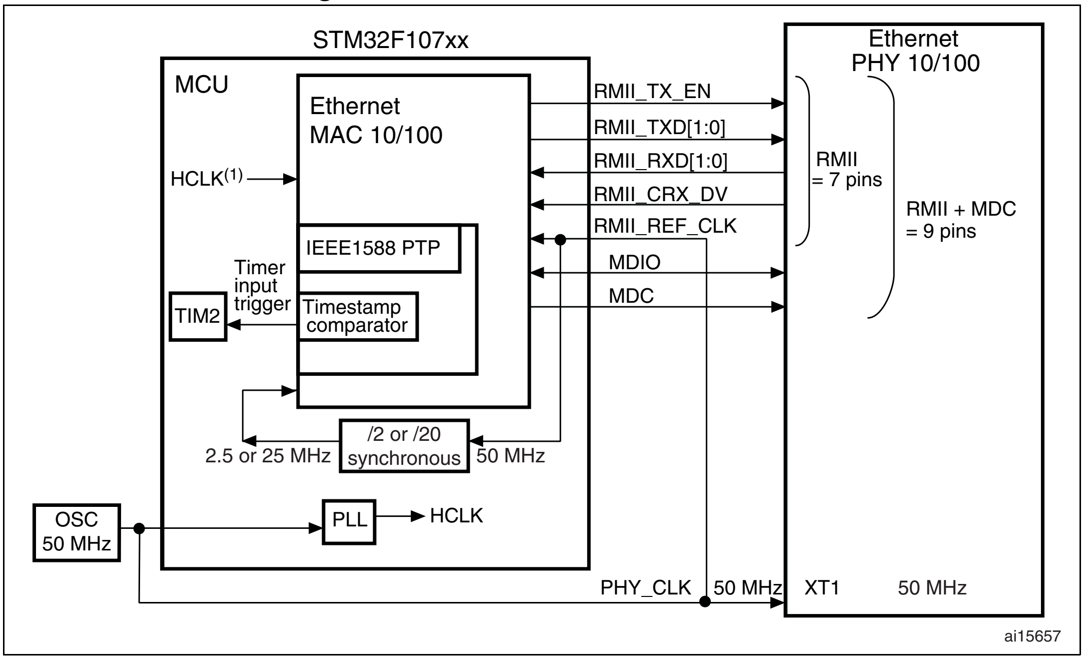
## A.2 Ethernet interface solutions

**Figure 53. MII mode using a 25 MHz crystal**




1. HCLK must be greater than 25 MHz.
2. Pulse per second when using IEEE1588 PTP, optional signal.

**Figure 54. RMII with a 50 MHz oscillator**




1. HCLK must be greater than 25 MHz.

Table 65. Document revision history (continued)

| Date | Revision | Changes |
|---|---|---|
| 14-Sep-2009 | 4 | Document status promoted from Preliminary data to full datasheet.<br>Number of DACs corrected in *Table 3: STM32F105xx and STM32F107xx family versus STM32F103xx family*.<br>*Note 5* added in *Table 5: Pin definitions*.<br>$V_{RERINT}$ and $T_{Coeff}$ added to *Table 12: Embedded internal reference voltage*.<br>Values added to *Table 13: Maximum current consumption in Run mode, code with data processing running from Flash*, *Table 14: Maximum current consumption in Run mode, code with data processing running from RAM* and *Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM*.<br>Typical $I_{DD\_VBAT}$ value added in *Table 16: Typical and maximum current consumptions in Stop and Standby modes*.<br>*Figure 10: Typical current consumption on VBAT with RTC on vs. temperature at different VBAT values* added.<br>Values modified in *Table 17: Typical current consumption in Run mode, code with data processing running from Flash* and *Table 18: Typical current consumption in Sleep mode, code running from Flash or RAM*.<br>$f_{HSE\_ext}$ min modified in *Table 20: High-speed external user clock characteristics*.<br>$C_{L1}$ and $C_{L2}$ replaced by C in *Table 22: HSE 3-25 MHz oscillator characteristics* and *Table 23: LSE oscillator characteristics (fLSE = 32.768 kHz)*, notes modified and moved below the tables. *Note 1* modified below *Figure 16: Typical application with an 8 MHz crystal*.<br>Conditions removed from *Table 26: Low-power mode wakeup timings*.<br>Standards modified in *Section 5.3.10: EMC characteristics on page 54*, conditions modified in *Table 31: EMS characteristics*.<br>Jitter maximum values added to *Table 27: PLL characteristics* and *Table 28: PLL2 and PLL3 characteristics*.<br>$R_{PU}$ and $R_{PD}$ modified in *Table 36: I/O static characteristics*.<br>Condition added for $V_{NF(NRST)}$ parameter in *Table 39: NRST pin characteristics*. Note removed and $R_{PD}$, $R_{PU}$ values added in *Table 46: USB OTG FS DC electrical characteristics*.<br>*Table 48: Ethernet DC electrical characteristics* added.<br>Parameter values added to *Table 49: Dynamic characteristics: Ethernet MAC signals for SMI*, *Table 50: Dynamic characteristics: Ethernet MAC signals for RMII* and *Table 51: Dynamic characteristics: Ethernet MAC signals for MII*.<br>$C_{ADC}$ and $R_{AIN}$ parameters modified in *Table 52: ADC characteristics*. $R_{AIN}$ max values modified in *Table 53: RAIN max for fADC = 14 MHz*.<br>*Table 56: DAC characteristics* modified. *Figure 38: 12-bit buffered /non-buffered DAC* added.<br>*Table 64: Applicative current consumption in Run mode, code with data processing running from Flash* added.<br>Small text changes. |