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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f105rct6w

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1 Introduction

This datasheet provides the description of the STM32F105xx and STM32F107xx connectivity line microcontrollers. For more details on the whole STMicroelectronics STM32F10xxx family, refer to *Section 2.2: Full compatibility throughout the family*.

The STM32F105xx and STM32F107xx datasheet should be read in conjunction with the STM32F10xxx reference manual.
For information on programming, erasing and protection of the internal Flash memory refer to the STM32F10xxx Flash programming manual.
The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core refer to the Cortex®-M3 Technical Reference Manual, available from the www.arm.com website.

Table 2. STM32F105xx and STM32F107xx features and peripheral counts (continued)

Peripherals[1]		STM32F105Rx	STM32F107Rx	STM32F105Vx	STM32F107Vx
Communication interfaces	SPI(I^2S)[2]	3(2)	3(2)	3(2)	3(2)
	I^2C	2	1	2	1
	USART	5			
	USB OTG FS	Yes			
	CAN	2			
GPIOs		51		80	
12-bit ADC Number of channels		2 16			
12-bit DAC Number of channels		2 2			
CPU frequency		72 MHz			
Operating voltage		2.0 to 3.6 V			
Operating temperatures		Ambient temperatures: –40 to +85 °C /–40 to +105 °C Junction temperature: –40 to + 125 °C			

1. Refer to *Table 5: Pin definitions* for peripheral availability when the I/O pins are shared by the peripherals required by the application.
2. The SPI2 and SPI3 interfaces give the flexibility to work in either the SPI mode or the I^2S audio mode.

Any of the standard timers can be used to generate PWM outputs. Each of the timers has independent DMA request generations.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.3.16 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.3.17 Universal synchronous/asynchronous receiver transmitters (USARTs)

The STM32F105xx and STM32F107xx connectivity line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART1 interface is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s.

Table 5. Pin definitions (continued)

Pins			Pin name	Type[1]	I / O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
BGA100	LQFP64	LQFP100					Default	Remap
A8	50	77	PA15	I/O	FT	JTDI	SPI3_NSS / I2S3_WS	TIM2_CH1_ETR / PA15 SPI1_NSS
B9	51	78	PC10	I/O	FT	PC10	UART4_TX	USART3_TX/ SPI3_SCK/I2S3_CK
B8	52	79	PC11	I/O	FT	PC11	UART4_RX	USART3_RX/ SPI3_MISO
C8	53	80	PC12	I/O	FT	PC12	UART5_TX	USART3_CK/ SPI3_MOSI/I2S3_SD
D8	-	81	PD0	I/O	FT	PD0	-	OSC_IN[9]/CAN1_RX
E8	-	82	PD1	I/O	FT	PD1	-	OSC_OUT[9]/CAN1_TX
B7	54	83	PD2	I/O	FT	PD2	TIM3_ETR / UART5_RX	
C7	-	84	PD3	I/O	FT	PD3	-	USART2_CTS
D7	-	85	PD4	I/O	FT	PD4	-	USART2_RTS
B6	-	86	PD5	I/O	FT	PD5	-	USART2_TX
C6	-	87	PD6	I/O	FT	PD6	-	USART2_RX
D6	-	88	PD7	I/O	FT	PD7	-	USART2_CK
A7	55	89	PB3	I/O	FT	JTDO	SPI3_SCK / I2S3_CK	PB3 / TRACESWO/ TIM2_CH2 / SPI1_SCK
A6	56	90	PB4	I/O	FT	NJTRST	SPI3_MISO	PB4 / TIM3_CH1/ SPI1_MISO
C5	57	91	PB5	I/O	-	PB5	I2C1_SMBA / SPI3_MOSI / ETH_MII_PPS_OUT / I2S3_SD ETH_RMII_PPS_OUT	TIM3_CH2/SPI1_MOSI/ CAN2_RX
B5	58	92	PB6	I/O	FT	PB6	I2C1_SCL[7]/TIM4_CH1[7]	USART1_TX/CAN2_TX
A5	59	93	PB7	I/O	FT	PB7	I2C1_SDA[7]/TIM4_CH2[7]	USART1_RX
D5	60	94	BOOT0	I	-	BOOT0	-	-
B4	61	95	PB8	I/O	FT	PB8	TIM4_CH3[7]/ ETH_MII_TXD3	I2C1_SCL/CAN1_RX
A4	62	96	PB9	I/O	FT	PB9	TIM4_CH4[7]	I2C1_SDA / CAN1_TX
D4	-	97	PE0	I/O	FT	PE0	TIM4_ETR	-
C4	-	98	PE1	I/O	FT	PE1	-	-
E5	63	99	V_{SS_3}	S	-	V_{SS_3}	-	-
F5	64	100	V_{DD_3}	S	-	V_{DD_3}	-	-

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

Figure 6. Pin loading conditions

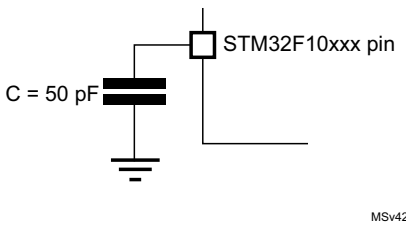


Figure 7. Pin input voltage

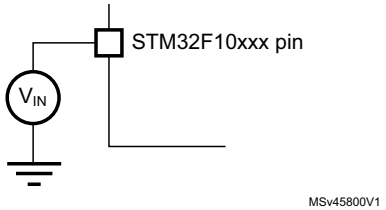


Table 13. Maximum current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled	72 MHz	68	68.4	mA
			48 MHz	49	49.2	
			36 MHz	38.7	38.9	
			24 MHz	27.3	27.9	
			16 MHz	20.2	20.5	
			8 MHz	10.2	10.8	
		External clock(2), all peripherals disabled	72 MHz	32.7	32.9	
			48 MHz	25	25.2	
			36 MHz	20.3	20.6	
			24 MHz	14.8	15.1	
			16 MHz	11.2	11.7	
			8 MHz	6.6	7.2	

1. Based on characterization, not tested in production.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 14. Maximum current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled	72 MHz	65.5	66	mA
			48 MHz	45.4	46	
			36 MHz	35.5	36.1	
			24 MHz	25.2	25.6	
			16 MHz	18	18.5	
			8 MHz	10.5	11	
		External clock(2), all peripherals disabled	72 MHz	31.4	31.9	
			48 MHz	27.8	28.2	
			36 MHz	17.6	18.3	
			24 MHz	13.1	13.8	
			16 MHz	10.2	10.9	
			8 MHz	6.1	7.8	

1. Based on characterization, tested in production at V_{DD} max, f_{HCLK} max..
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 18. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock(3)	72 MHz	28.2	6	mA
			48 MHz	19	4.2	
			36 MHz	14.7	3.4	
			24 MHz	10.1	2.5	
			16 MHz	6.7	2	
			8 MHz	3.2	1.3	
			4 MHz	2.3	1.2	
			2 MHz	1.7	1.16	
			1 MHz	1.5	1.1	
			500 kHz	1.3	1.05	
			125 kHz	1.2	1.05	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	36 MHz	13.7	2.6	
			24 MHz	9.3	1.8	
			16 MHz	6.3	1.3	
			8 MHz	2.7	0.6	
			4 MHz	1.6	0.5	
			2 MHz	1	0.46	
			1 MHz	0.8	0.44	
			500 kHz	0.6	0.43	
			125 kHz	0.5	0.42	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 19*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with one peripheral clocked on (with only the clock applied)
- ambient operating temperature and V_{DD} supply voltage conditions summarized in *Table 6*

Low-speed external user clock generated from an external source

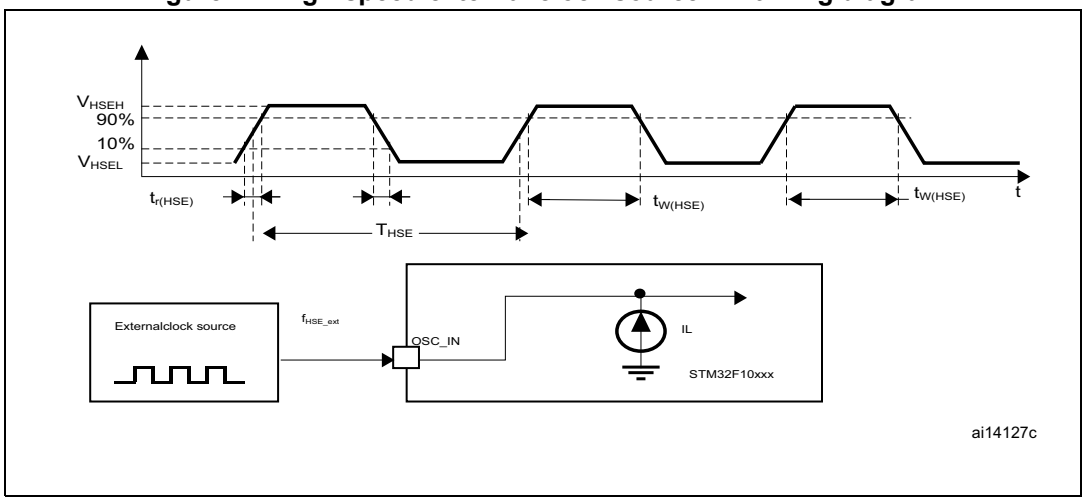
The characteristics given in *Table 21* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 9*.

Table 21. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-		32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	5		pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Figure 14. High-speed external clock source AC timing diagram



I^2S - SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 43* for SPI or in *Table 44* for I^2S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

Refer to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I^2S).

Table 43. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode	4 t_{PCLK}	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2 t_{PCLK}	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	50	60	
$t_{su(MI)}$	Data input setup time	Master mode	4	-	
$t_{su(SI)}$		Slave mode	5	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	
$t_{h(SI)}$		Slave mode	5	-	
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK} = 20 MHz	-	3*t_{PCLK}	
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	-	34	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	8	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	32	-	
$t_{h(MO)}$		Master mode (after enable edge)	10	-	

Table 50 gives the list of Ethernet MAC signals for the RMII and *Figure 32* shows the corresponding timing diagram.

Figure 32. Ethernet RMII timing diagram

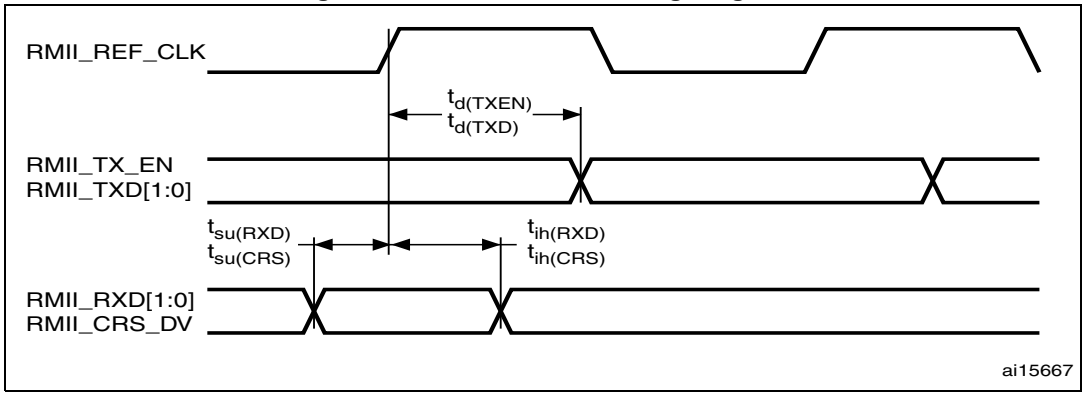
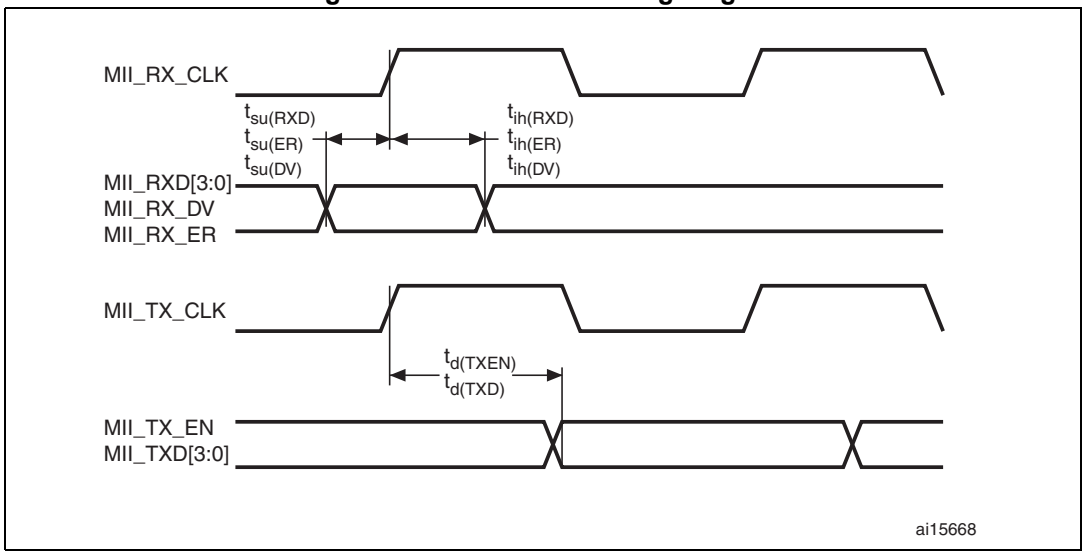


Table 50. Dynamic characteristics: Ethernet MAC signals for RMII

Symbol	Rating	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	4	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	2	-	-	ns
$t_{su(DV)}$	Carrier sense set-up time	4	-	-	ns
$t_{ih(DV)}$	Carrier sense hold time	2	-	-	ns
$t_{d(TXEN)}$	Transmit enable valid delay time	8	10	16	ns
$t_{d(TXD)}$	Transmit data valid delay time	7	10	16	ns

Table 51 gives the list of Ethernet MAC signals for MII and *Figure 32* shows the corresponding timing diagram.

Figure 33. Ethernet MII timing diagram



5.3.18 DAC electrical specifications

Table 56. DAC characteristics

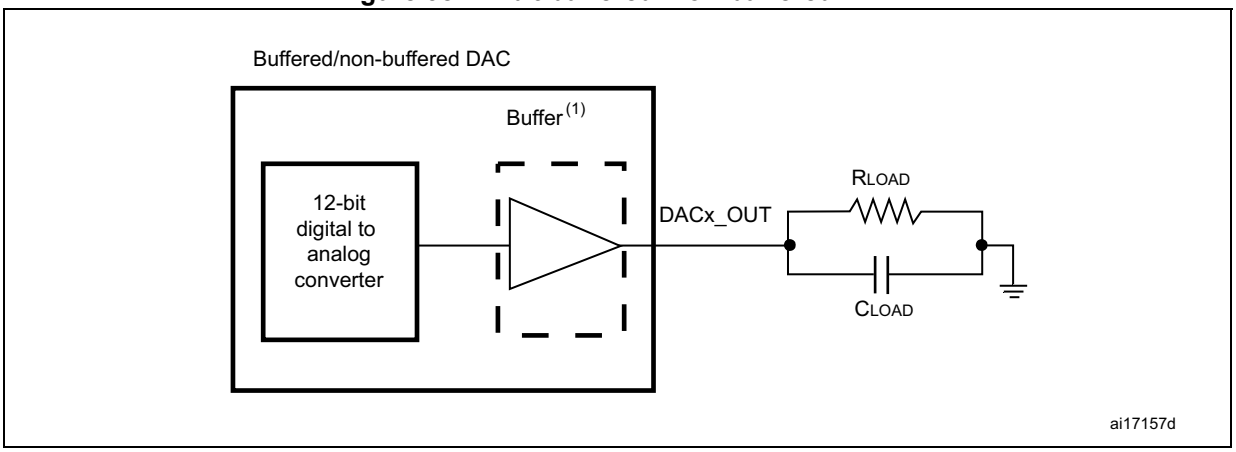
Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	2.4	-	3.6	V	-
V_{REF+}	Reference supply voltage	2.4	-	3.6	V	V_{REF+} must always be below V_{DDA}
V_{SSA}	Ground	0	-	0	V	-
R_{LOAD}(1)	Resistive load with buffer ON	5	-	-	kΩ	-
R_O(1)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(1)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x155) to (0xEAB) at V_{REF+} = 2.4 V
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer OFF	-	-	V_{REF+} – 1LSB	V	
$I_{DDVREF+}$	DAC DC current consumption in quiescent mode (Standby mode)	-	-	220	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
I_{DDA}	DAC DC current consumption in quiescent mode (Standby mode)	-	-	380	µA	With no load, middle code (0x800) on the inputs
		-	-	480	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
DNL(2)	Differential non linearity Difference between two consecutive code-1LSB)	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration.
		-	-	±2	LSB	Given for the DAC in 12-bit configuration.
INL(2)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±1	LSB	Given for the DAC in 10-bit configuration.
		-	-	±4	LSB	Given for the DAC in 12-bit configuration.

Table 56. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
Offset(2)	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$)	-	-	±10	mV	Given for the DAC in 12-bit configuration
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(2)	Gain error	-	-	±0.5	%	Given for the DAC in 12bit configuration
$t_{SETTLING}$(2)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	3	4	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
Update rate(2)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP}(2)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Guaranteed by design, not tested in production.
2. Guaranteed by characterization, not tested in production.

Figure 38. 12-bit buffered /non-buffered DAC



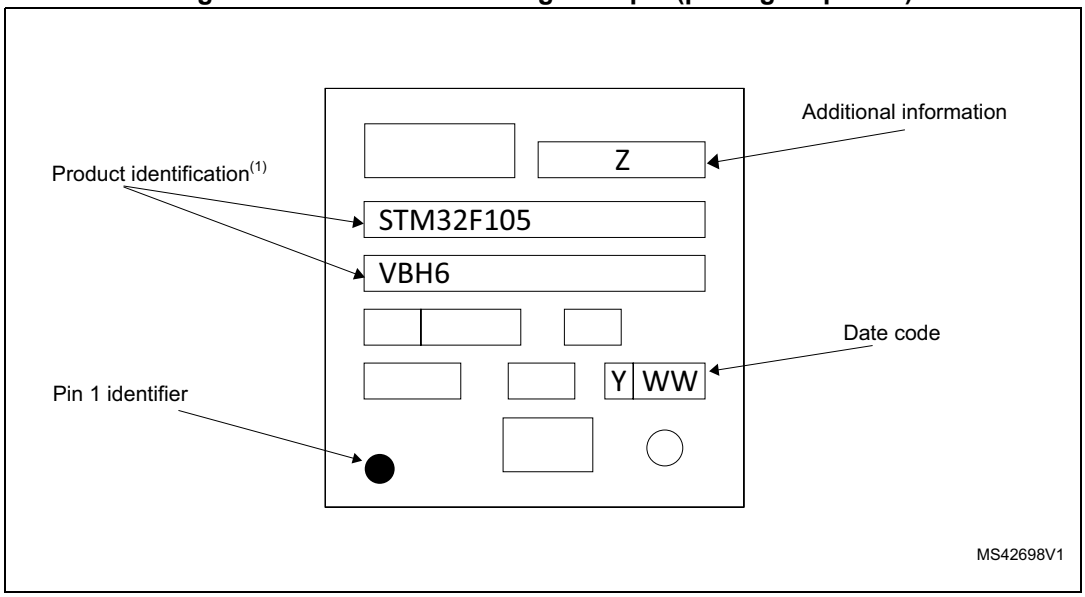
1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Device marking for LFBGA100

The following figure shows the device marking for the LQFP100 package.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 42. LFBGA100 marking example (package top view)



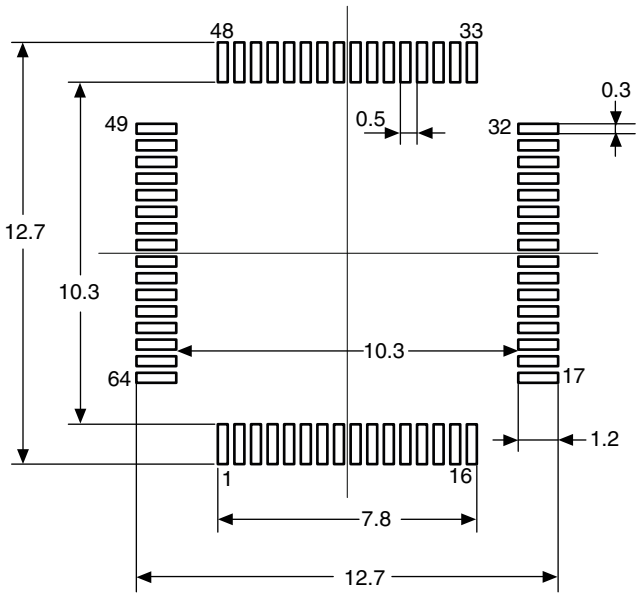
Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 60.LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

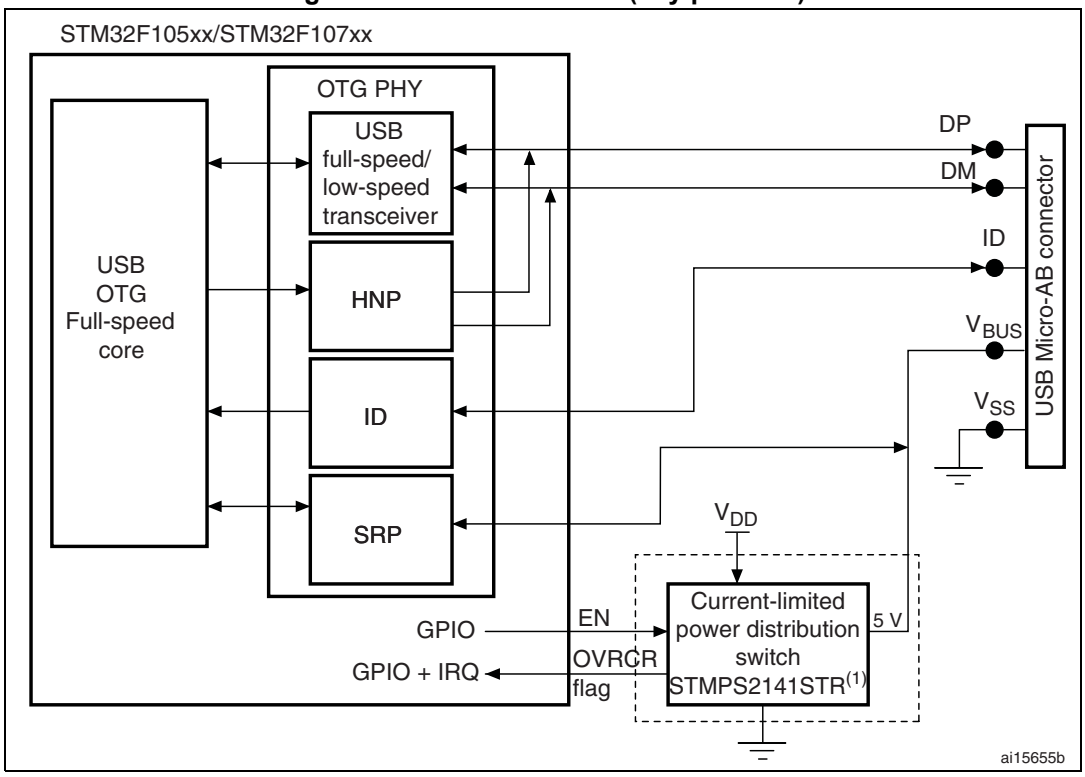
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 47.LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint



1. Dimensions are in millimeters.

Figure 52. OTG connection (any protocol)



1. STMPS2141STR needed only if the application has to support bus-powered devices.

Table 65. Document revision history (continued)

Date	Revision	Changes
19-Jun-2009	3	*Section 2.3.8: Boot modes* and *Section 2.3.20: Ethernet MAC interface with dedicated DMA and IEEE 1588 support* updated. *Section 2.3.24: Remap capability* added. *Figure 1: STM32F105xx and STM32F107xx connectivity line block diagram* and *Figure 5: Memory map* updated. In *Table 5: Pin definitions*: – I2S3_WS, I2S3_CK and I2S3_SD default alternate functions added – small changes in signal names – *Note 6* modified – ETH_MII_PPS_OUT and ETH_RMII_PPS_OUT replaced by ETH_PPS_OUT – ETH_MII_MDIO and ETH_RMII_MDIO replaced by ETH_MDIO – ETH_MII_MDC and ETH_RMII_MDC replaced by ETH_MDC Figures: *Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled* and *Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled* removed. *Table 13: Maximum current consumption in Run mode, code with data processing running from Flash*, *Table 14: Maximum current consumption in Run mode, code with data processing running from RAM* and *Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM* are to be determined. *Figure 12* and *Figure 13* show typical curves. PLL1 renamed to PLL. I_{DD} supply current in Stop mode modified in *Table 16: Typical and maximum current consumptions in Stop and Standby modes*. *Figure 11: Typical current consumption in Stop mode with regulator in Run mode versus temperature at different VDD values*, *Figure 13: Typical current consumption in Standby mode versus temperature at different VDD values* and *Figure 13: Typical current consumption in Standby mode versus temperature at different VDD values* updated. *Table 17: Typical current consumption in Run mode, code with data processing running from Flash*, *Table 18: Typical current consumption in Sleep mode, code running from Flash or RAM* and *Table 19: Peripheral current consumption* updated. f_{HSE_ext} modified in *Table 20: High-speed external user clock characteristics*. Min PLL input clock (f_{PLL_IN}), f_{PLL_OUT} min and f_{PLL_VCO} min modified in *Table 27: PLL characteristics*. ACC_{HSI} max values modified in *Table 24: HSI oscillator characteristics*. *Table 31: EMS characteristics* and *Table 32: EMI characteristics* updated. *Table 43: SPI characteristics* updated. Modified: *Figure 28: I2S slave timing diagram (Philips protocol)(1)*, *Figure 29: I2S master timing diagram (Philips protocol)(1)* and *Figure 31: Ethernet SMI timing diagram*. BGA100 package removed. *Section 6.4: Thermal characteristics* added. Small text changes.

Table 65. Document revision history (continued)

Date	Revision	Changes
14-Sep-2009	4	Document status promoted from Preliminary data to full datasheet. Number of DACs corrected in *Table 3: STM32F105xx and STM32F107xx family versus STM32F103xx family*. *Note 5* added in *Table 5: Pin definitions*. V_{RERINT} and T_{Coeff} added to *Table 12: Embedded internal reference voltage*. Values added to *Table 13: Maximum current consumption in Run mode, code with data processing running from Flash*, *Table 14: Maximum current consumption in Run mode, code with data processing running from RAM* and *Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM*. Typical I_{DD_VBAT} value added in *Table 16: Typical and maximum current consumptions in Stop and Standby modes*. *Figure 10: Typical current consumption on VBAT with RTC on vs. temperature at different VBAT values* added. Values modified in *Table 17: Typical current consumption in Run mode, code with data processing running from Flash* and *Table 18: Typical current consumption in Sleep mode, code running from Flash or RAM*. f_{HSE_ext} min modified in *Table 20: High-speed external user clock characteristics*. C_{L1} and C_{L2} replaced by C in *Table 22: HSE 3-25 MHz oscillator characteristics* and *Table 23: LSE oscillator characteristics (fLSE = 32.768 kHz)*, notes modified and moved below the tables. *Note 1* modified below *Figure 16: Typical application with an 8 MHz crystal*. Conditions removed from *Table 26: Low-power mode wakeup timings*. Standards modified in *Section 5.3.10: EMC characteristics on page 54*, conditions modified in *Table 31: EMS characteristics*. Jitter maximum values added to *Table 27: PLL characteristics* and *Table 28: PLL2 and PLL3 characteristics*. R_{PU} and R_{PD} modified in *Table 36: I/O static characteristics*. Condition added for $V_{NF(NRST)}$ parameter in *Table 39: NRST pin characteristics*. Note removed and R_{PD}, R_{PU} values added in *Table 46: USB OTG FS DC electrical characteristics*. *Table 48: Ethernet DC electrical characteristics* added. Parameter values added to *Table 49: Dynamic characteristics: Ethernet MAC signals for SMI*, *Table 50: Dynamic characteristics: Ethernet MAC signals for RMII* and *Table 51: Dynamic characteristics: Ethernet MAC signals for MII*. C_{ADC} and R_{AIN} parameters modified in *Table 52: ADC characteristics*. R_{AIN} max values modified in *Table 53: RAIN max for fADC = 14 MHz*. *Table 56: DAC characteristics* modified. *Figure 38: 12-bit buffered /non-buffered DAC* added. *Table 64: Applicative current consumption in Run mode, code with data processing running from Flash* added. Small text changes.

Table 65. Document revision history (continued)

Date	Revision	Changes
11-May-2010	5	Added BGA package. *Table 5: Pin definitions*: ETH_RMII_RXD0 and ETH_RMII_RXD1 added in remap column for PD9 and PD10, respectively. Note added to ETH_MII_RX_DV, ETH_MII_RXD0, ETH_MII_RXD1, ETH_MII_RXD2 and ETH_MII_RXD3 Updated *Table 36: I/O static characteristics on page 57* Added *Figure 18: Standard I/O input characteristics - CMOS port* to *Figure 21: 5 V tolerant I/O input characteristics - TTL port* Updated *Table 43: SPI characteristics on page 66*. Updated *Table 44: I2S characteristics on page 69*. Updated *Table 48: Ethernet DC electrical characteristics on page 72*. Updated *Table 49: Dynamic characteristics: Ethernet MAC signals for SMI on page 72*. Updated *Table 50: Dynamic characteristics: Ethernet MAC signals for RMII on page 73* Updated *Figure 59: USB O44TG FS + Ethernet solution on page 100*. Updated *Figure 60: USB OTG FS + I2S (Audio) solution on page 100*
01-Aug-2011	6	Changed SRAM size to 64 KB on all parts. Updated PD0 and PD1 description in *Table 5: Pin definitions on page 27* Updated footnotes below *Table 6: Voltage characteristics on page 36* and *Table 7: Current characteristics on page 36* Updated tw min in *Table 20: High-speed external user clock characteristics on page 47* Updated startup time in *Table 23: LSE oscillator characteristics (fLSE = 32.768 kHz) on page 50* Added *Section 5.3.12: I/O current injection characteristics on page 56* Updated *Table 36: I/O static characteristics on page 57* Add Interna code V to *Table 62: Ordering information scheme on page 94*
06-Mar-2014	7	Added a “Packing” entry to *Table 62: Ordering information scheme* including “Blank = tray” and “TR = Tape and reel”. Referenced 4 Figures: *Figure 41*, *Figure 49*, *Figure 59* and *Figure 60*. Updated the “Package” line with “BGA100” in *Table 2: STM32F105xx and STM32F107xx features and peripheral counts*.