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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f105rct7

Contents

1 Introduction

This datasheet provides the description of the STM32F105xx and STM32F107xx connectivity line microcontrollers. For more details on the whole STMicroelectronics STM32F10xxx family, refer to *Section 2.2: Full compatibility throughout the family*.

The STM32F105xx and STM32F107xx datasheet should be read in conjunction with the STM32F10xxx reference manual.
For information on programming, erasing and protection of the internal Flash memory refer to the STM32F10xxx Flash programming manual.
The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core refer to the Cortex®-M3 Technical Reference Manual, available from the www.arm.com website.

2 Description

The STM32F105xx and STM32F107xx connectivity line family incorporates the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 256 Kbytes and SRAM 64 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, four general-purpose 16-bit timers plus a PWM timer, as well as standard and advanced communication interfaces: up to two I^2Cs, three SPIs, two I2Ss, five USARTs, an USB OTG FS and two CANs. Ethernet is available on the STM32F107xx only.

The STM32F105xx and STM32F107xx connectivity line family operates in the –40 to +105 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F105xx and STM32F107xx connectivity line family offers devices in three different package types: from 64 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F105xx and STM32F107xx connectivity line microcontroller family suitable for a wide range of applications such as motor drives and application control, medical and handheld equipment, industrial applications, PLCs, inverters, printers, and scanners, alarm systems, video intercom, HVAC and home audio equipment.

2.1 Device overview

Figure 1 shows the general block diagram of the device family.

Table 2. STM32F105xx and STM32F107xx features and peripheral counts

Peripherals(1)		STM32F105Rx			STM32F107Rx		STM32F105Vx			STM32F107Vx	
Flash memory in Kbytes		64	128	256	128	256	64	128	256	128	256
SRAM in Kbytes		64									
Package		LQFP64					LQFP 100	LQFP 100, BGA 100	LQFP 100	LQFP 100	LQFP 100, BGA 100
Ethernet		No			Yes		No			Yes	
Timers	General-purpose	4									
	Advanced-control	1									
	Basic	2									

2.2 Full compatibility throughout the family

The STM32F105xx and STM32F107xx constitute the connectivity line family whose members are fully pin-to-pin, software and feature compatible.

The STM32F105xx and STM32F107xx are a drop-in replacement for the low-density (STM32F103x4/6), medium-density (STM32F103x8/B) and high-density (STM32F103xC/D/E) performance line devices, allowing the user to try different memory densities and peripherals providing a greater degree of freedom during the development cycle.

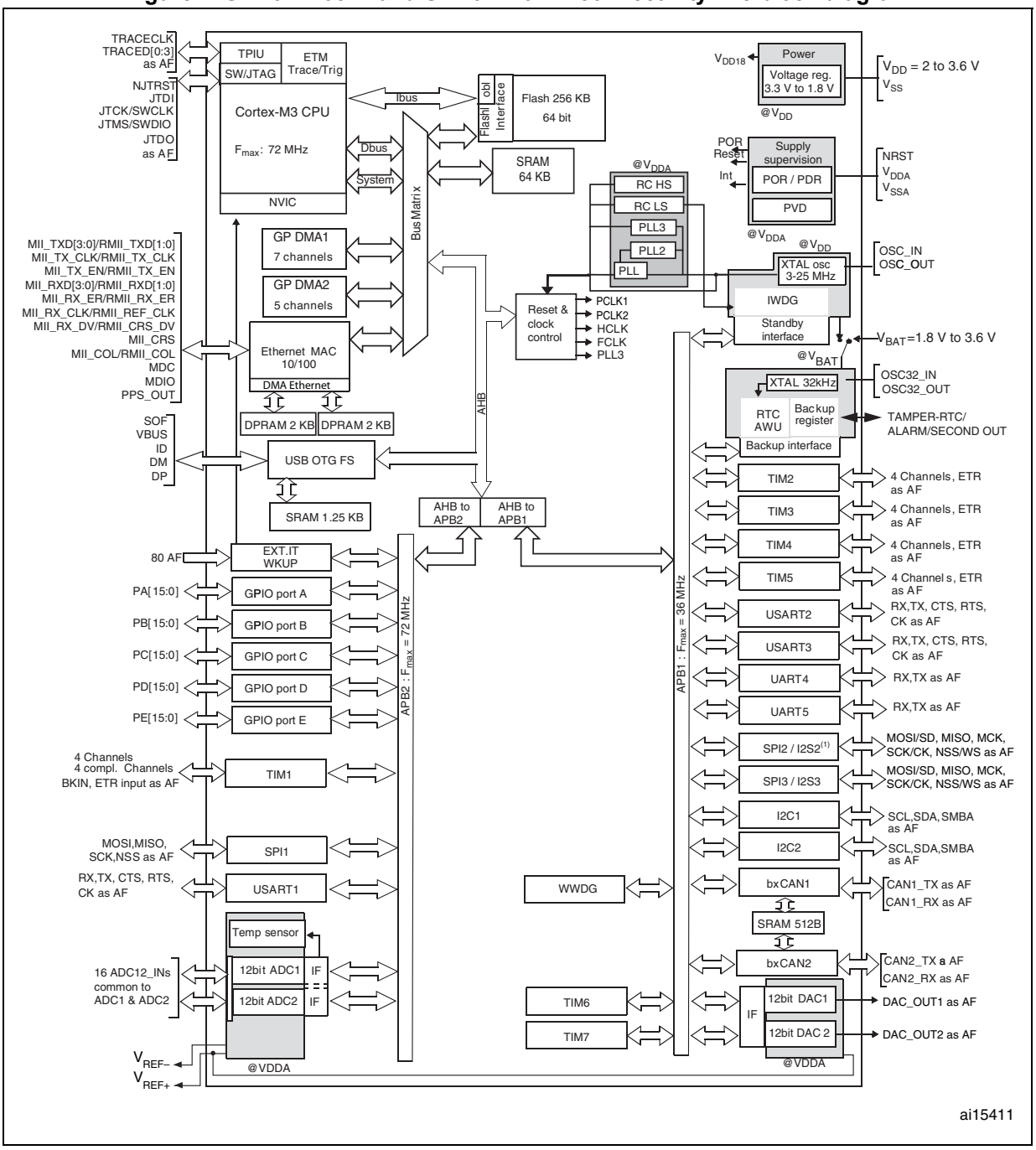
Table 3. STM32F105xx and STM32F107xx family versus STM32F103xx family(1)

<table>
<tr><th>STM32 device</th><th colspan="2">Low-density STM32F103xx devices</th><th colspan="3">Medium-density STM32F103xx devices</th><th colspan="3">High-density STM32F103xx devices</th><th colspan="3">STM32F105xx</th><th colspan="2">STM32F107xx</th></tr>
<tr><td>Flash size (KB)</td><td>16</td><td>32</td><td>32</td><td>64</td><td>128</td><td>256</td><td>384</td><td>512</td><td>64</td><td>128</td><td>256</td><td>128</td><td>256</td></tr>
<tr><td>RAM size (KB)</td><td>6</td><td>10</td><td>10</td><td>20</td><td>20</td><td>48</td><td>64</td><td>64</td><td>64</td><td>64</td><td>64</td><td>64</td><td>64</td></tr>
<tr><td>144 pins</td><td colspan="5" rowspan="2"></td><td colspan="3" rowspan="3">5 × USARTs
4 × 16-bit timers,
2 × basic timers, 3 × SPIs,
2 × I²Ss, 2 × I2Cs, USB,
CAN, 2 × PWM timers
3 × ADCs, 2 × DACs,
1 × SDIO, FSMC (100- and 144-pin packages(2))</td><td colspan="5"></td></tr>
<tr><td>100 pins</td><td colspan="3" rowspan="2">3 × USARTs
3 × 16-bit timers
2 × SPIs,
2 × I²Cs, USB, CAN,
1 × PWM timer
2 × ADCs</td><td colspan="3" rowspan="2">5 × USARTs,
4 × 16-bit timers,
2 × basic timers,
3 × SPIs,
2 × I²Ss,
2 × I2Cs,
USB OTG FS,
2 × CANs,
1 × PWM timer,
2 × ADCs,
2 × DACs</td><td colspan="2" rowspan="2">5 × USARTs,
4 × 16-bit timers,
2 × basic timers,
3 × SPIs,
2 × I²S,
1 × I2C,
USB OTG FS,
2 × CANs,
1 × PWM timer,
2 × ADCs,
2 × DACs,
Ethernet</td></tr>
<tr><td>64 pins</td><td colspan="2" rowspan="3">2 × USARTs
2 × 16-bit timers
1 × SPI, 1 × I²C, USB, CAN,
1 × PWM timer
2 × ADCs</td><td colspan="2" rowspan="3">2 × USARTs
2 × 16-bit timers
1 × SPI,
1 × I²C,
USB, CAN,
1 × PWM timer
2 × ADCs</td></tr>
<tr><td>48 pins</td><td colspan="3"></td></tr>
<tr><td>36 pins</td><td colspan="3"></td></tr>
</table>

1. Refer to *Table 5: Pin definitions* for peripheral availability when the I/O pins are shared by the peripherals required by the application.
2. Ports F and G are not available in devices delivered in 100-pin packages.

2.3 Overview

Figure 1. STM32F105xx and STM32F107xx connectivity line block diagram



1. T_A = –40 °C to +85 °C (suffix 6, see *Table 62*) or –40 °C to +105 °C (suffix 7, see *Table 62*), junction temperature up to 105 °C or 125 °C, respectively.
2. AF = alternate function on I/O port pin.

3 Pinouts and pin description

Figure 2. STM32F105xx and STM32F107xx connectivity line BGA100 ballout top view

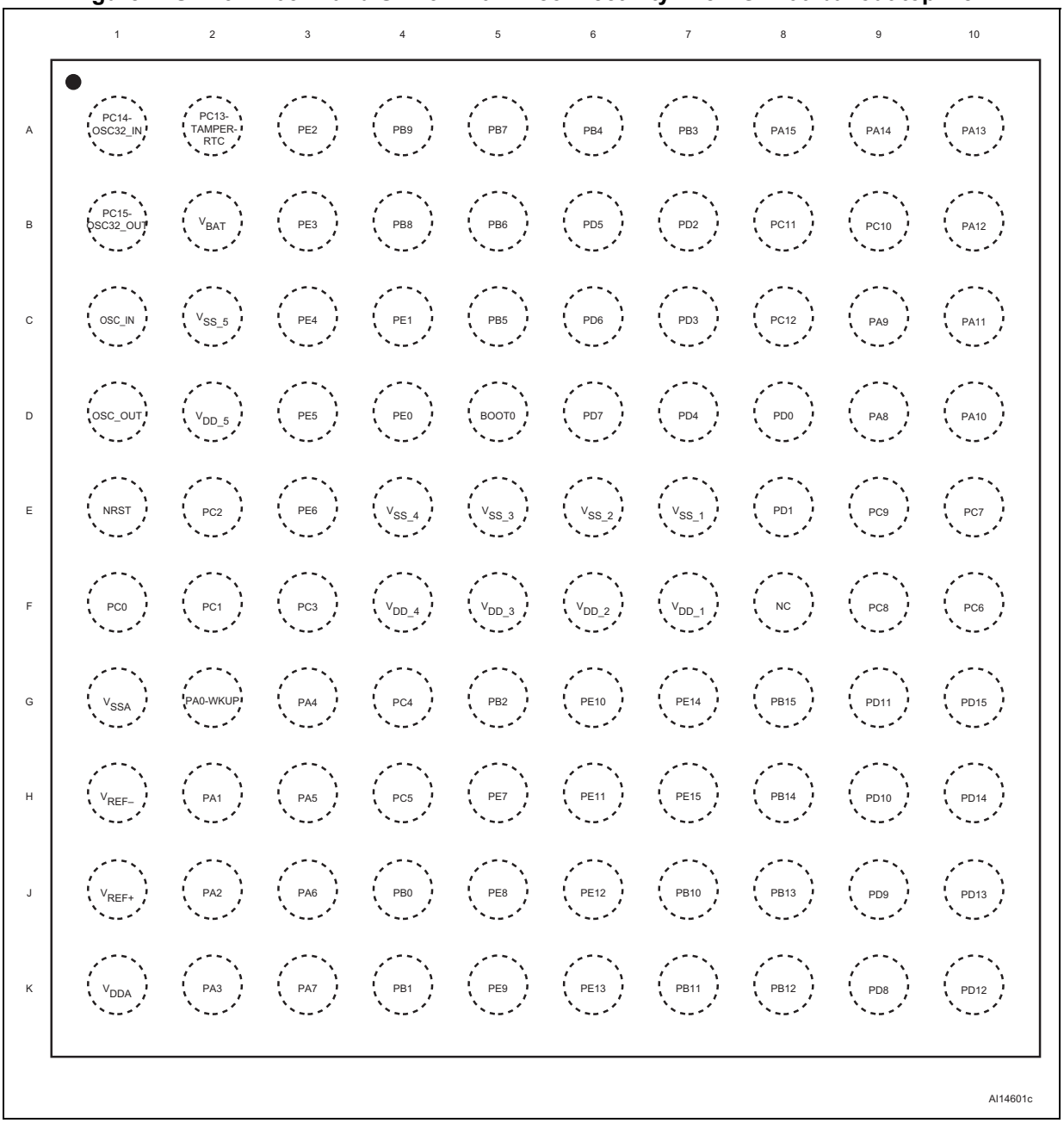


Table 5. Pin definitions (continued)

Pins			Pin name	Type[1]	I / O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
BGA100	LQFP64	LQFP100					Default	Remap
J9	-	56	PD9	I/O	FT	PD9	-	USART3_RX/ ETH_MII_RXD0/ ETH_RMII_RXD0
H9	-	57	PD10	I/O	FT	PD10	-	USART3_CK/ ETH_MII_RXD1/ ETH_RMII_RXD1
G9	-	58	PD11	I/O	FT	PD11	-	USART3_CTS/ ETH_MII_RXD2
K10	-	59	PD12	I/O	FT	PD12	-	TIM4_CH1 / USART3_RTS/ ETH_MII_RXD3
J10	-	60	PD13	I/O	FT	PD13	-	TIM4_CH2
H10	-	61	PD14	I/O	FT	PD14	-	TIM4_CH3
G10	-	62	PD15	I/O	FT	PD15	-	TIM4_CH4
F10	37	63	PC6	I/O	FT	PC6	I2S2_MCK/	TIM3_CH1
E10	38	64	PC7	I/O	FT	PC7	I2S3_MCK	TIM3_CH2
F9	39	65	PC8	I/O	FT	PC8	-	TIM3_CH3
E9	40	66	PC9	I/O	FT	PC9	-	TIM3_CH4
D9	41	67	PA8	I/O	FT	PA8	USART1_CK/OTG_FS_SOF / TIM1_CH1[8]/MCO	-
C9	42	68	PA9	I/O	FT	PA9	USART1_TX[7]/ TIM1_CH2[7]/ OTG_FS_VBUS	-
D10	43	69	PA10	I/O	FT	PA10	USART1_RX[7]/ TIM1_CH3[7]/OTG_FS_ID	-
C10	44	70	PA11	I/O	FT	PA11	USART1_CTS / CAN1_RX / TIM1_CH4[7]/OTG_FS_DM	-
B10	45	71	PA12	I/O	FT	PA12	USART1_RTS / OTG_FS_DP / CAN1_TX[7] / TIM1_ETR[7]	-
A10	46	72	PA13	I/O	FT	JTMS-SWDIO	-	PA13
F8	-	73	Not connected					-
E6	47	74	V_{SS_2}	S	-	V_{SS_2}	-	-
F6	48	75	V_{DD_2}	S	-	V_{DD_2}	-	-
A9	49	76	PA14	I/O	FT	JTCK-SWCLK	-	PA14

1. I = input, O = output, S = supply, HiZ = high impedance.
2. FT = 5 V tolerant. All I/Os are V_{DD} capable.
3. Function availability depends on the chosen device.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch, and so their use in output mode is limited: they can be used only in output 2 MHz mode with a maximum load of 30 pF and only one pin can be put in output mode at a time.
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
7. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
8. SPI2/I2S2 and I2C2 are not available when the Ethernet is being used.
9. For the LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 and BGA100 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.

Table 15. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled	72 MHz	48.4	49	mA
			48 MHz	33.9	34.4	
			36 MHz	26.7	27.2	
			24 MHz	19.3	19.8	
			16 MHz	14.2	14.8	
			8 MHz	8.7	9.1	
		External clock(2), all peripherals disabled	72 MHz	10.1	10.6	
			48 MHz	8.3	8.75	
			36 MHz	7.5	8	
			24 MHz	6.6	7.1	
			16 MHz	6	6.5	
			8 MHz	2.5	3	

1. Based on characterization, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 16. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)			Max		Unit
			V_{DD}/V_{BAT} = 2.0 V	V_{DD}/V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in Run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	32	33	600	1300	µA
		Regulator in Low Power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	25	26	590	1280	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON	-	3	3.8	-	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	-	2.8	3.6	-	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	-	1.9	2.1	5(2)	6.5(2)	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.1	1.2	1.4	2.1(2)	2.3(2)	

1. Typical values are measured at T_A = 25 °C.
2. Based on characterization, not tested in production.

5.3.7 Internal clock source characteristics

The parameters given in *Table 24* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

High-speed internal (HSI) RC oscillator

Table 24. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	8		MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register(2)		-	-	1(3)	%
		Factory-calibrated(4)	T_A = –40 to 105 °C	–2	-	2.5	%
			T_A = –10 to 85 °C	–1.5	-	2.2	%
			T_A = 0 to 70 °C	–1.3	-	2	%
			T_A = 25 °C	–1.1	-	1.8	%
$t_{su(HSI)}$(4)	HSI oscillator startup time	-		1	-	2	µs
$I_{DD(HSI)}$(4)	HSI oscillator power consumption	-		-	80	100	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Refer to application note AN2868 “STM32F10xxx internal RC oscillator (HSI) calibration” available from the ST website *www.st.com*.
3. Guaranteed by design, not tested in production.
4. Based on characterization, not tested in production.

Low-speed internal (LSI) RC oscillator

Table 25. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	30	40	60	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.65	1.2	µA

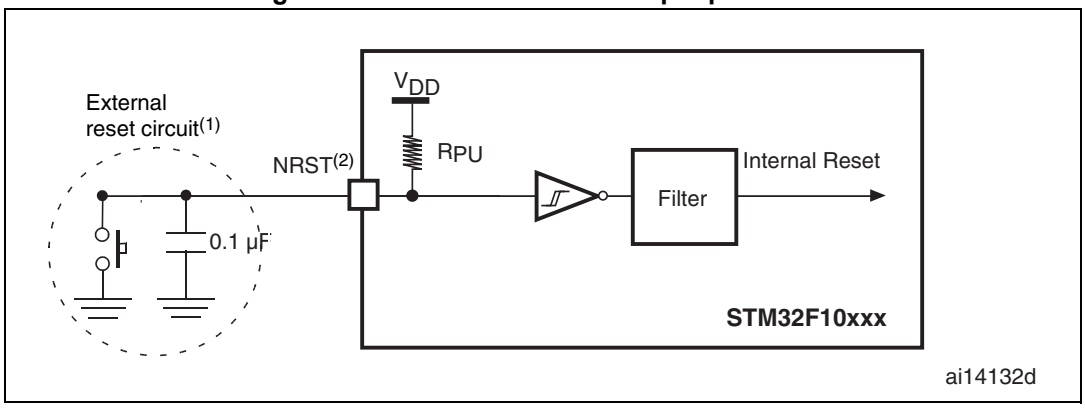
1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in *Table 26* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

Figure 23. Recommended NRST pin protection



2. The reset network protects the device against parasitic resets.
3. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 39*. Otherwise the reset will not be taken into account by the device.

5.3.15 TIM timer characteristics

The parameters given in *Table 40* are guaranteed by design.

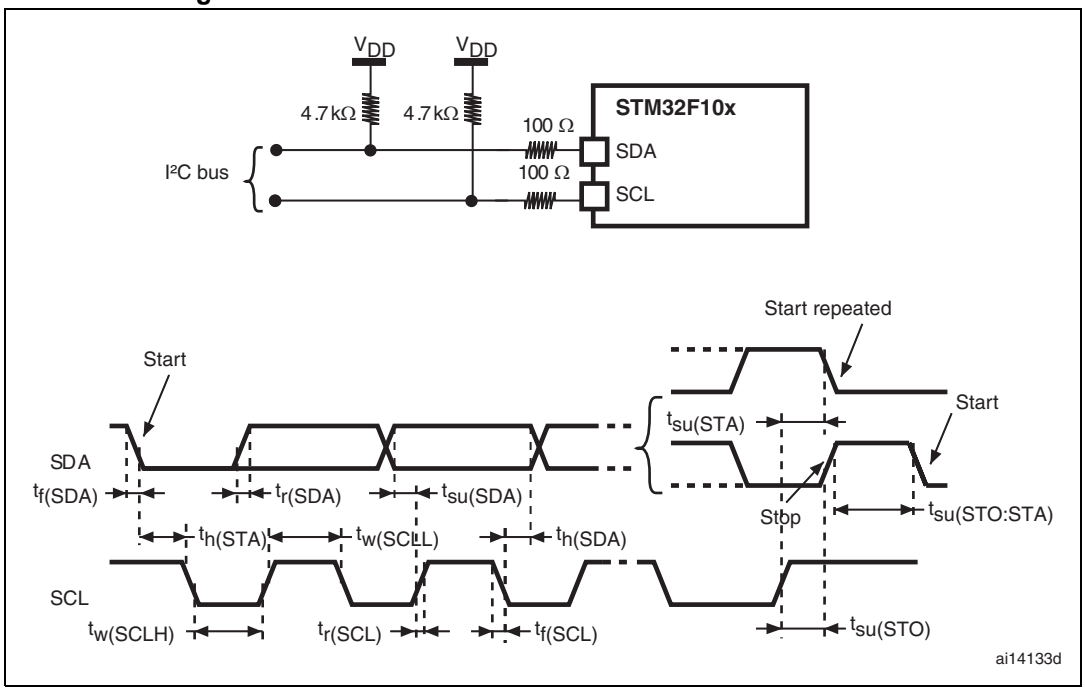
Refer to *Section 5.3.12: I/O current injection characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 40. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	36	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.0139	910	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.6	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM4 and TIM5 timers.

Figure 24. I²C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 42. SCL frequency (f_{PCLK1}= 36 MHz.,V_{DD} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

I^2S - SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 43* for SPI or in *Table 44* for I^2S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

Refer to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I^2S).

Table 43. SPI characteristics

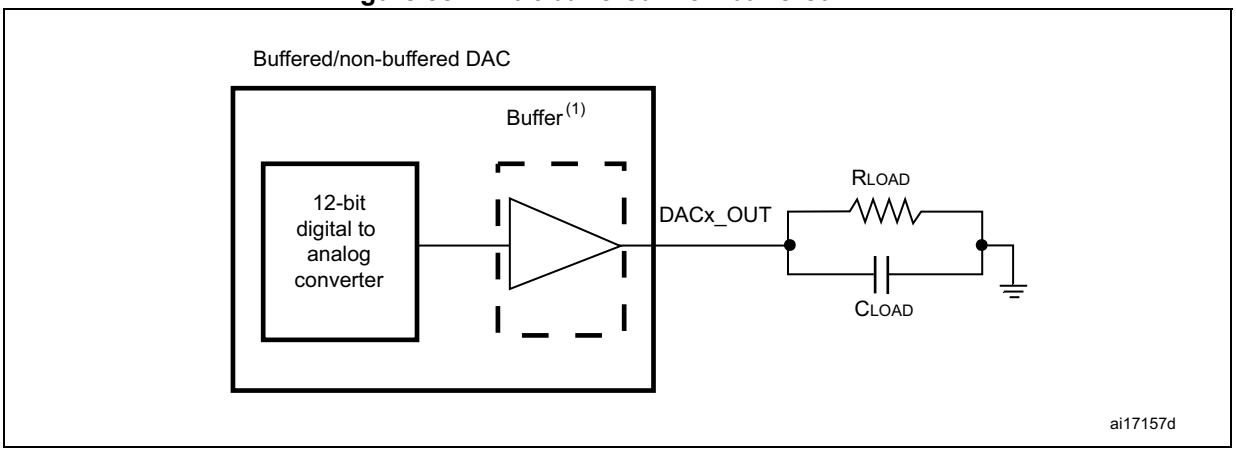
Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode	4 t_{PCLK}	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2 t_{PCLK}	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	50	60	
$t_{su(MI)}$	Data input setup time	Master mode	4	-	
$t_{su(SI)}$		Slave mode	5	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	
$t_{h(SI)}$		Slave mode	5	-	
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK} = 20 MHz	-	3*t_{PCLK}	
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	-	34	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	8	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	32	-	
$t_{h(MO)}$		Master mode (after enable edge)	10	-	

Table 56. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
Offset(2)	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$)	-	-	±10	mV	Given for the DAC in 12-bit configuration
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(2)	Gain error	-	-	±0.5	%	Given for the DAC in 12bit configuration
$t_{SETTLING}$(2)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	3	4	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
Update rate(2)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP}(2)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Guaranteed by design, not tested in production.
2. Guaranteed by characterization, not tested in production.

Figure 38. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

5.3.19 Temperature sensor characteristics

Table 57. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L (1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25} (1)	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START} (2)	Startup time	4	-	10	µs
T_{S_temp} (3)(2)	ADC sampling time when reading the temperature	-	-	17.1	µs

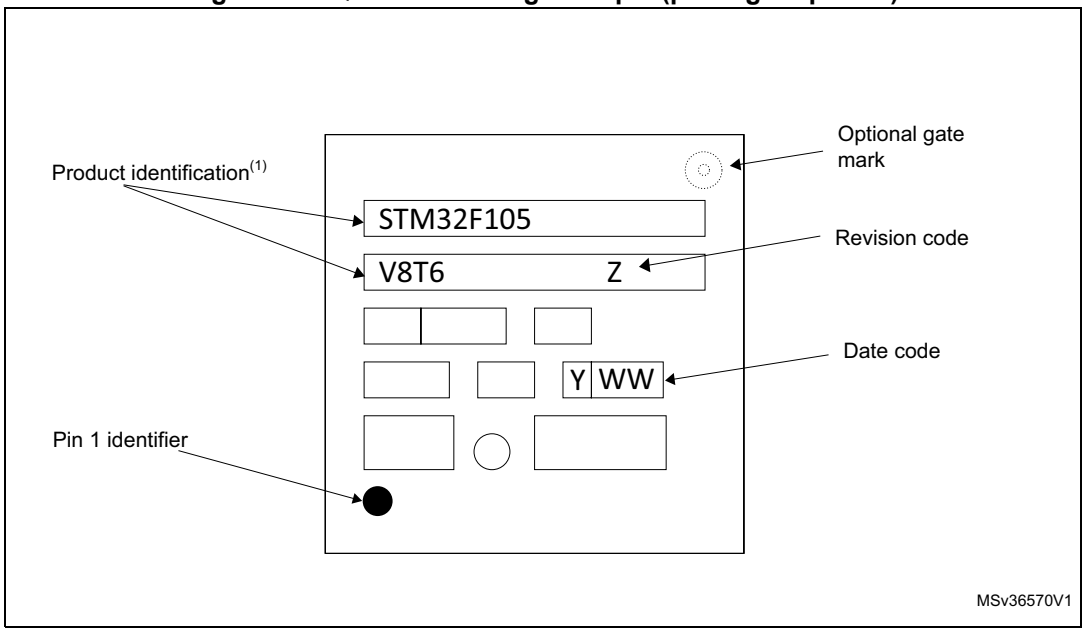
1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

Device marking for LQFP100

The following figure shows the device marking for the LQFP100 package.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

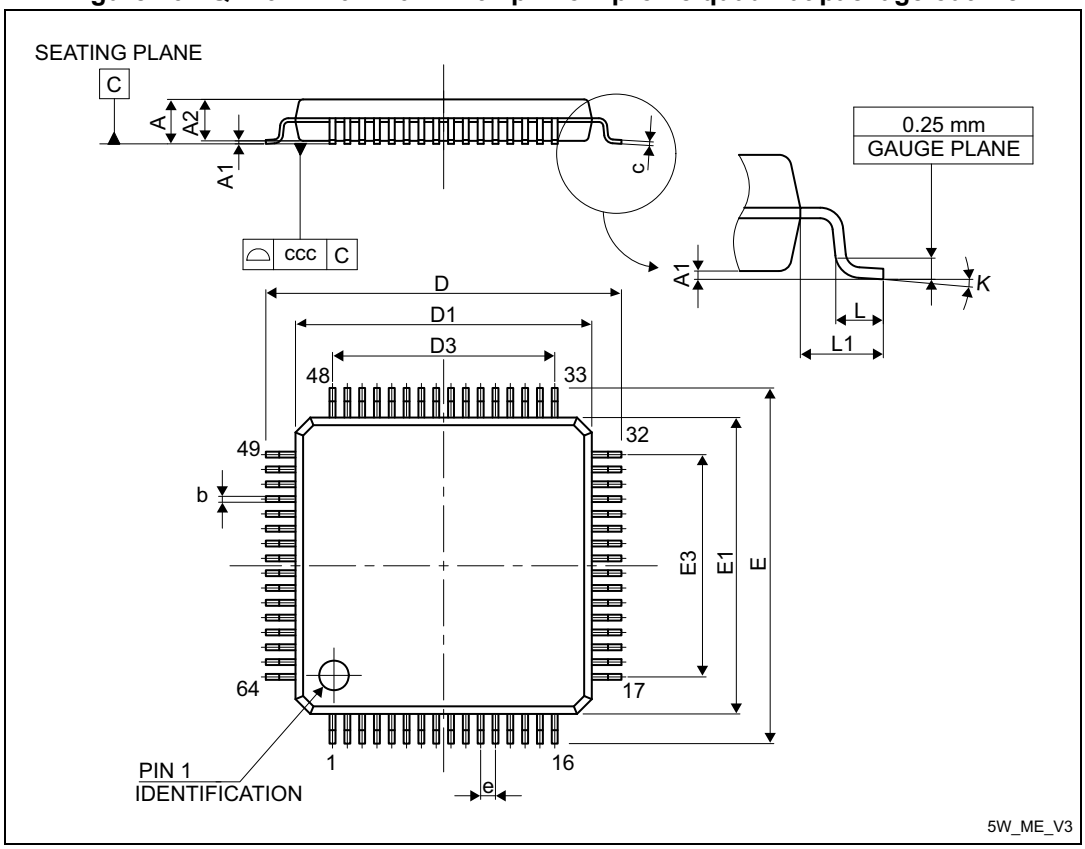
Figure 45.LQFP100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6.3 LQFP64 package information

Figure 46.LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline



1. Drawing is not in scale.

Table 60.LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

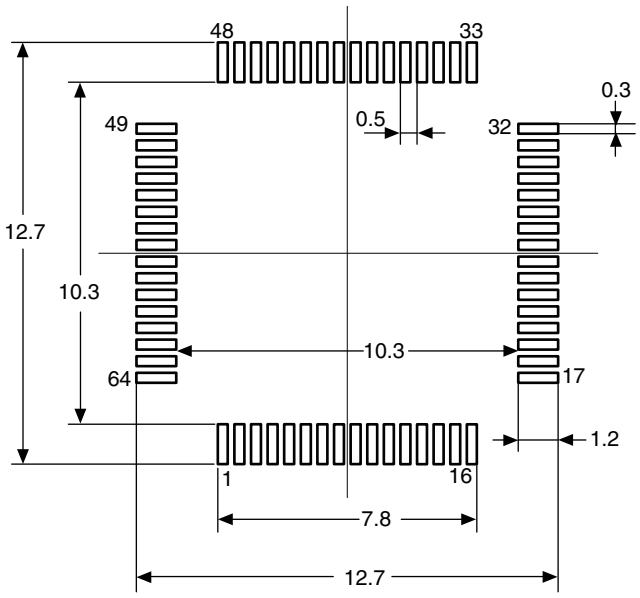
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-

Table 60.LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

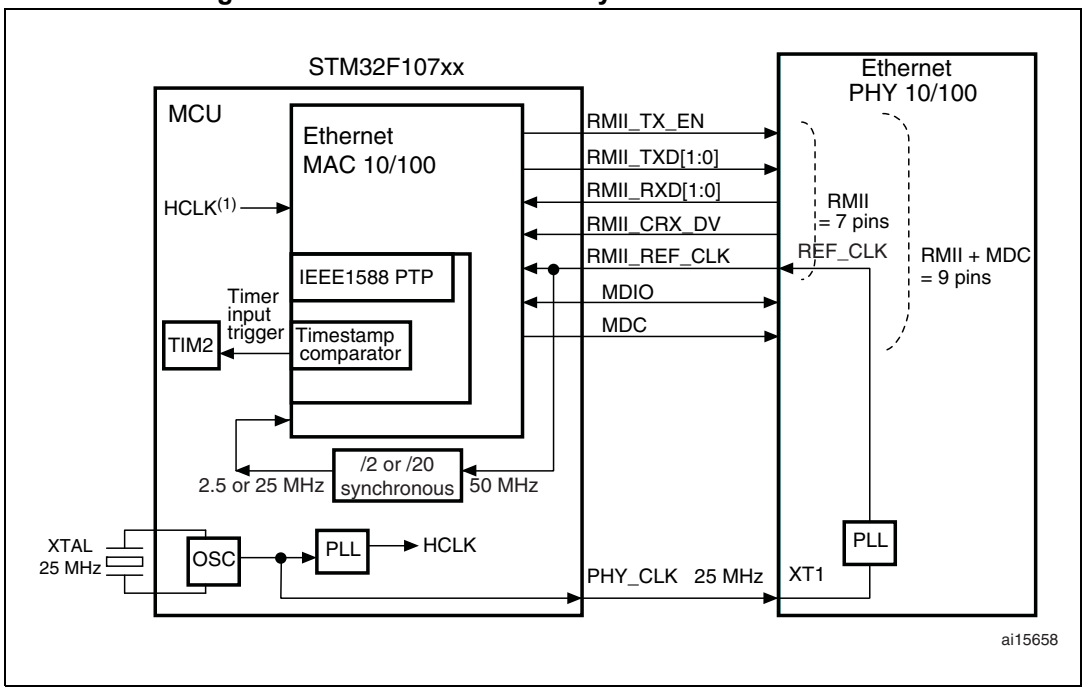
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 47.LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint



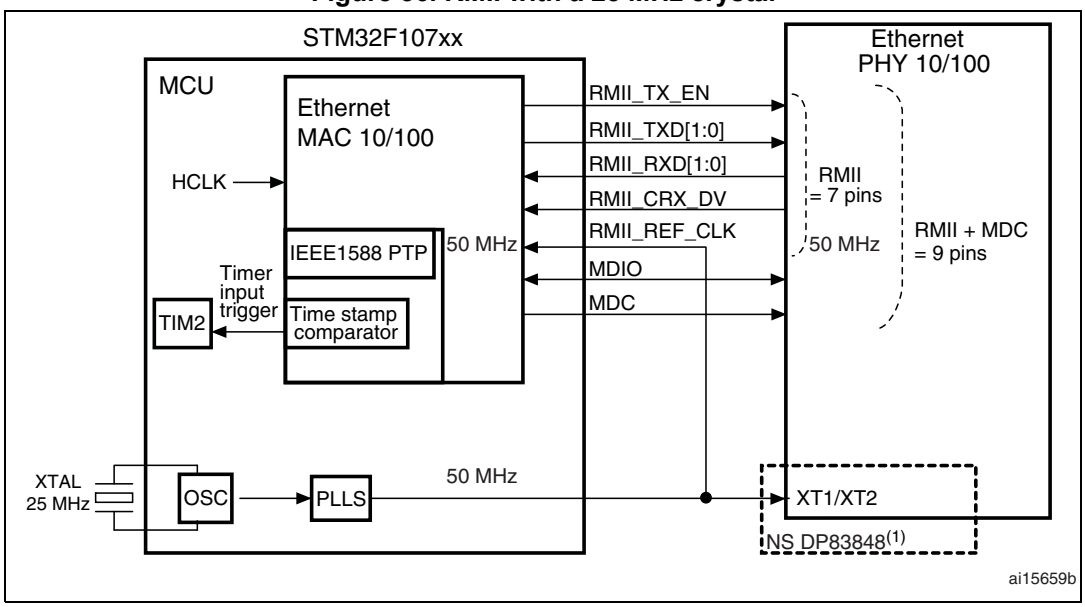
1. Dimensions are in millimeters.

Figure 55. RMII with a 25 MHz crystal and PHY with PLL



1. HCLK must be greater than 25 MHz.

Figure 56. RMII with a 25 MHz crystal



1. The NS DP83848 is recommended as the input jitter requirement of this PHY. It is compliant with the output jitter specification of the MCU.