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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	80
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f105v8t6

1 Introduction

This datasheet provides the description of the STM32F105xx and STM32F107xx connectivity line microcontrollers. For more details on the whole STMicroelectronics STM32F10xxx family, refer to *Section 2.2: Full compatibility throughout the family*.

The STM32F105xx and STM32F107xx datasheet should be read in conjunction with the STM32F10xxx reference manual.
For information on programming, erasing and protection of the internal Flash memory refer to the STM32F10xxx Flash programming manual.
The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core refer to the Cortex®-M3 Technical Reference Manual, available from the www.arm.com website.

2.3.1 ARM Cortex-M3 core with embedded Flash and SRAM

The ARM Cortex-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.
With its embedded ARM core, STM32F105xx and STM32F107xx connectivity line family is compatible with all ARM tools and software.
Figure 1 shows the general block diagram of the device family.

2.3.2 Embedded Flash memory

64 to 256 Kbytes of embedded Flash is available for storing programs and data.

2.3.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.3.4 Embedded SRAM

64 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.3.5 Nested vectored interrupt controller (NVIC)

The STM32F105xx and STM32F107xx connectivity line embeds a nested vectored interrupt controller able to handle up to 67 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.3.13 DMA

The flexible 12-channel general-purpose DMAs (7 channels for DMA1 and 5 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.
Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose, basic and advanced control timers TIMx, DAC, I^2S and ADC.

In the STM32F107xx, there is a DMA controller dedicated for use with the Ethernet (see *Section 2.3.20: Ethernet MAC interface with dedicated DMA and IEEE 1588 support* for more information).

2.3.14 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

For more information, refer to AN2604: "*STM32F101xx and STM32F103xx RTC calibration*", available from *www.st.com*.

USART1, USART2 and USART3 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

2.3.18 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC/SDHC[a] modes.

All SPIs can be served by the DMA controller.

2.3.19 Inter-integrated sound (I^2S)

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 96 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency with less than 0.5% accuracy error owing to the advanced clock controller (see *Section 2.3.7: Clocks and startup*).

Refer to the “Audio frequency precision” tables provided in the “Serial peripheral interface (SPI)” section of the STM32F10xxx reference manual.

2.3.20 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

Peripheral not available on STM32F105xx devices.

The STM32F107xx devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard media-independent interface (MII) or a reduced media-independent interface (RMII). The STM32F107xx requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). the PHY is connected to the STM32F107xx MII port using as many as 17 signals (MII) or 9 signals (RMII) and can be clocked using the 25 MHz (MII) or 50 MHz (RMII) output from the STM32F107xx.

The STM32F107xx includes the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors (see the STM32F105xx/STM32F107xx reference manual for details)
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support

a. SDHC = Secure digital high capacity.

3 Pinouts and pin description

Figure 2. STM32F105xx and STM32F107xx connectivity line BGA100 ballout top view

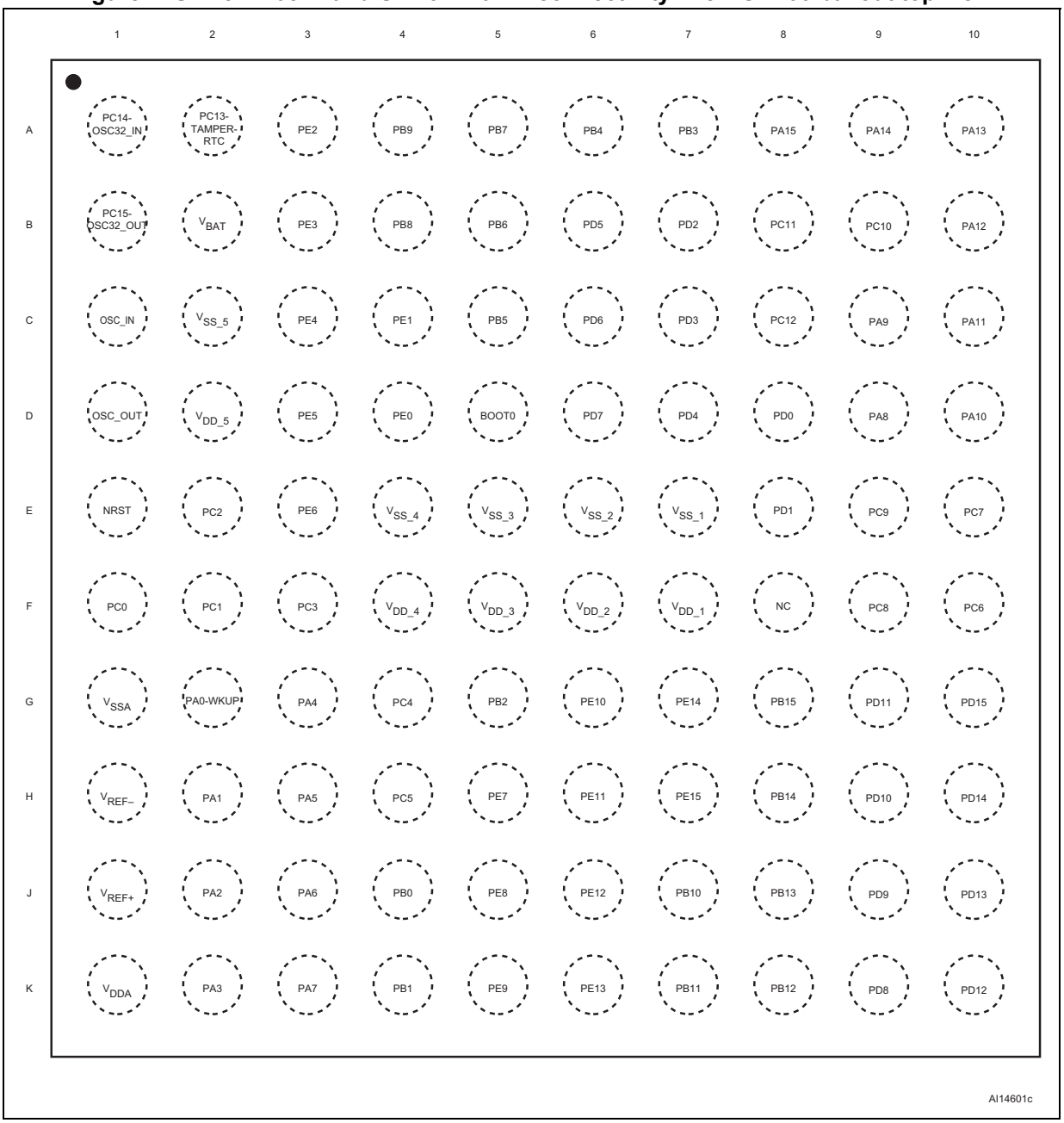


Table 5. Pin definitions

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
BGA100	LQFP64	LQFP100					Default	Remap
A3	-	1	PE2	I/O	FT	PE2	TRACECK	-
B3	-	2	PE3	I/O	FT	PE3	TRACED0	-
C3	-	3	PE4	I/O	FT	PE4	TRACED1	-
D3	-	4	PE5	I/O	FT	PE5	TRACED2	-
E3	-	5	PE6	I/O	FT	PE6	TRACED3	-
B2	1	6	V_{BAT}	S	-	V_{BAT}	-	-
A2	2	7	PC13-TAMPER-RTC(5)	I/O	-	PC13(6)	TAMPER-RTC	-
A1	3	8	PC14-OSC32_IN(5)	I/O	-	PC14(6)	OSC32_IN	-
B1	4	9	PC15-OSC32_OUT(5)	I/O	-	PC15(6)	OSC32_OUT	-
C2	-	10	V_{SS_5}	S	-	V_{SS_5}	-	-
D2	-	11	V_{DD_5}	S	-	V_{DD_5}	-	-
C1	5	12	OSC_IN	I	-	OSC_IN	-	-
D1	6	13	OSC_OUT	O	-	OSC_OUT	-	-
E1	7	14	NRST	I/O	-	NRST	-	-
F1	8	15	PC0	I/O	-	PC0	ADC12_IN10	-
F2	9	16	PC1	I/O	-	PC1	ADC12_IN11/ ETH_MII_MDC/ ETH_RMII_MDC	-
E2	10	17	PC2	I/O	-	PC2	ADC12_IN12/ ETH_MII_TXD2	-
F3	11	18	PC3	I/O	-	PC3	ADC12_IN13/ ETH_MII_TX_CLK	-
G1	12	19	V_{SSA}	S	-	V_{SSA}	-	-
H1	-	20	V_{REF-}	S	-	V_{REF-}	-	-
J1	-	21	V_{REF+}	S	-	V_{REF+}	-	-
K1	13	22	V_{DDA}	S	-	V_{DDA}	-	-
G2	14	23	PA0-WKUP	I/O	-	PA0	WKUP/USART2_CTS(7) ADC12_IN0/TIM2_CH1_ETR TIM5_CH1/ ETH_MII_CRS_WKUP	-

1. I = input, O = output, S = supply, HiZ = high impedance.
2. FT = 5 V tolerant. All I/Os are V_{DD} capable.
3. Function availability depends on the chosen device.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch, and so their use in output mode is limited: they can be used only in output 2 MHz mode with a maximum load of 30 pF and only one pin can be put in output mode at a time.
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
7. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
8. SPI2/I2S2 and I2C2 are not available when the Ethernet is being used.
9. For the LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 and BGA100 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.

Table 15. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled	72 MHz	48.4	49	mA
			48 MHz	33.9	34.4	
			36 MHz	26.7	27.2	
			24 MHz	19.3	19.8	
			16 MHz	14.2	14.8	
			8 MHz	8.7	9.1	
		External clock(2), all peripherals disabled	72 MHz	10.1	10.6	
			48 MHz	8.3	8.75	
			36 MHz	7.5	8	
			24 MHz	6.6	7.1	
			16 MHz	6	6.5	
			8 MHz	2.5	3	

1. Based on characterization, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 16. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)			Max		Unit
			V_{DD}/V_{BAT} = 2.0 V	V_{DD}/V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in Run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	32	33	600	1300	µA
		Regulator in Low Power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	25	26	590	1280	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON	-	3	3.8	-	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	-	2.8	3.6	-	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	-	1.9	2.1	5(2)	6.5(2)	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.1	1.2	1.4	2.1(2)	2.3(2)	

1. Typical values are measured at T_A = 25 °C.
2. Based on characterization, not tested in production.

Figure 10. Typical current consumption on V_{BAT} with RTC on vs. temperature at different V_{BAT} values

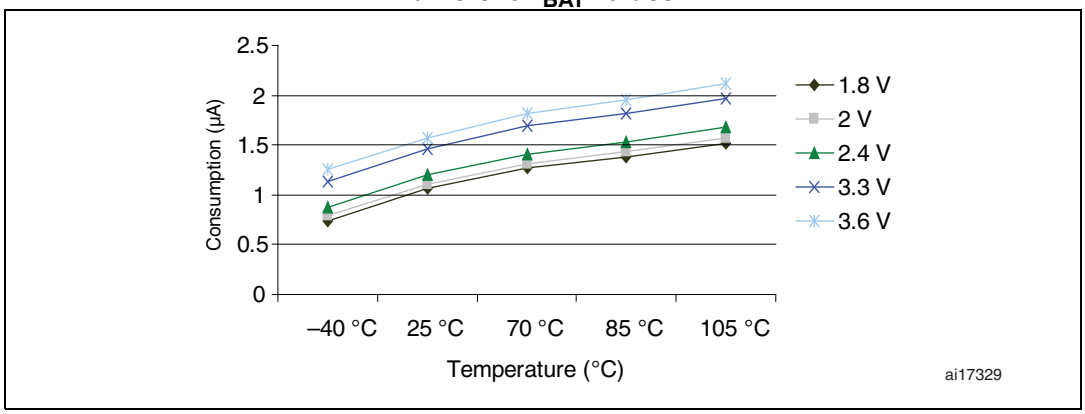


Figure 11. Typical current consumption in Stop mode with regulator in Run mode versus temperature at different V_{DD} values

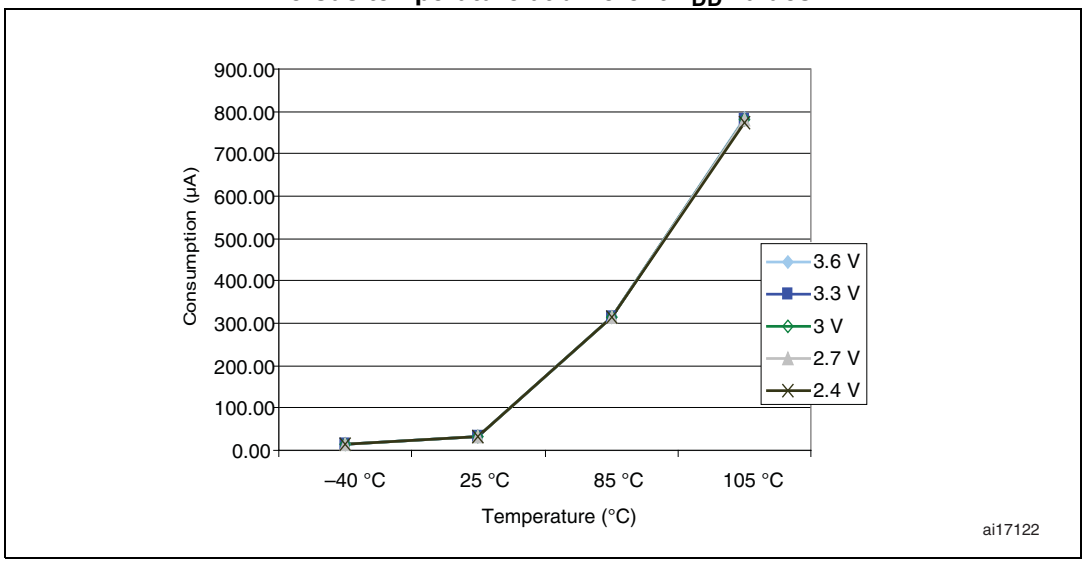
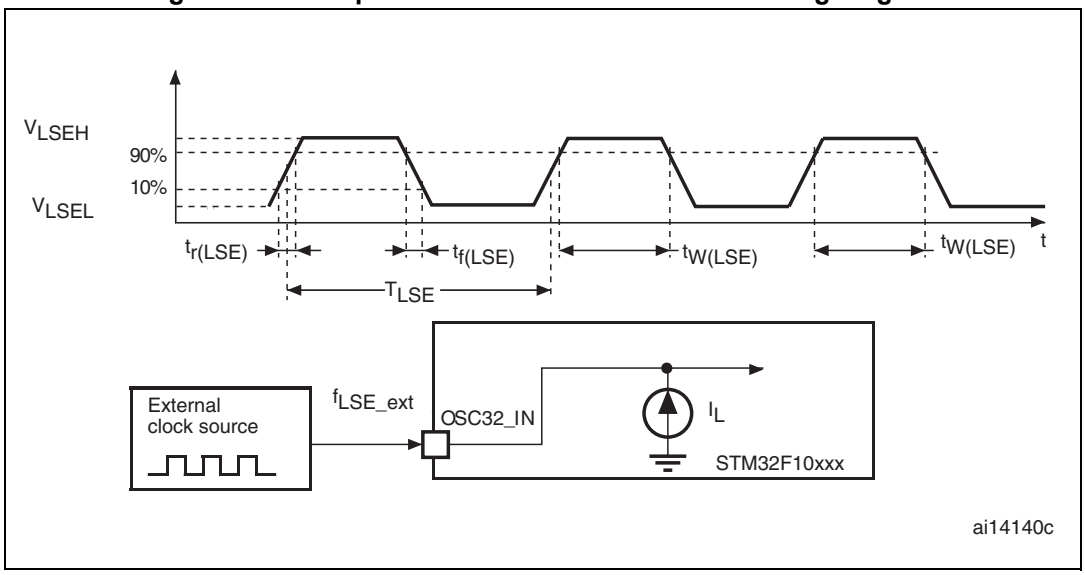


Figure 15. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 3 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 22*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 22. HSE 3-25 MHz oscillator characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	3		25	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	30	-	pF
i_2	HSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization, not tested in production.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

5.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 29. Flash memory characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	52.5	70	µs
t_{ERASE}	Page (1 KB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Read mode f_{HCLK} = 72 MHz with 2 wait states, V_{DD} = 3.3 V	-	-	20	mA
		Write / Erase modes f_{HCLK} = 72 MHz, V_{DD} = 3.3 V	-	-	5	mA
		Power-down mode / Halt, V_{DD} = 3.0 to 3.6 V	-	-	50	µA
V_{prog}	Programming voltage	-	2	-	3.6	V

1. Guaranteed by design, not tested in production.

Table 30. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	-	-	Kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	-	-	Years
		1 kcycle(2) at T_A = 105 °C	10	-	-	
		10 kcycles(2) at T_A = 55 °C	20	-	-	

1. Based on characterization, not tested in production.
2. Cycling performed over the whole temperature range.

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

Table 32. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]		Unit
				8/48 MHz	8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP100 package compliant with IEC61967-2	0.1 to 30 MHz	9	9	dBµV
			30 to 130 MHz	26	13	
			130 MHz to 1GHz	25	31	
			EMI Level	4	4	-

5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 33. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to JESD22-C101	II	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 34. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

5.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product

operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 35*

Table 35. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

5.3.13 I/O port characteristics

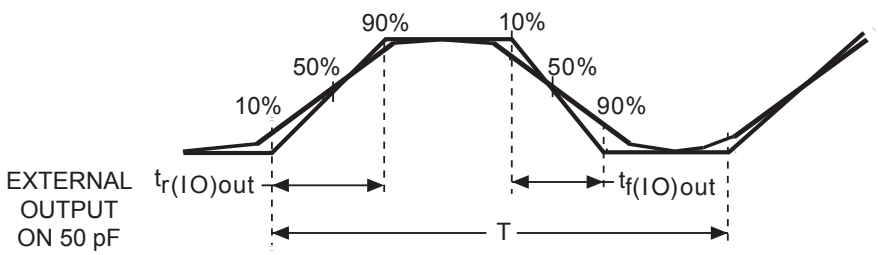
General input/output characteristics

Unless otherwise specified, the parameters given in *Table 36* are derived from tests performed under the conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 36. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO input low level voltage	-	–0.3	-	0.28*(V_{DD}-2 V)+0.8 V	V
	IO FT(1) input low level voltage	-	–0.3	-	0.32*(V_{DD}-2V)+0.75 V	V
V_{IH}	Standard IO input high level voltage	-	0.41*(V_{DD}-2 V)+1.3 V	-	V_{DD}+0.3	V
	IO FT(1) input high level voltage	V_{DD} > 2 V	0.42*(V_{DD}-2 V)+1 V	-	5.5	V
		$V_{DD} \leq$ 2 V			5.2	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis(2)	-	200	-	-	mV
	IO FT Schmitt trigger voltage hysteresis(2)	-	5% V_{DD}(3)	-	-	mV

Figure 22. I/O AC characteristics definition



Maximum frequency is achieved if (t_r + t_f) < (2/3)T and if the duty cycle is (45-55%) when loaded by 50 pF

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5.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 36*).

Unless otherwise specified, the parameters given in *Table 39* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 39. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	–0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	V_{DD} > 2.7 V	300	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Table 44. I^2S characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master data: 16 bits, audio freq = 48 K		1.52	1.54	MHz
		Slave		0	6.5	
$t_{r(CK)}$ $t_{f(CK)}$	I^2S clock rise and fall time	capacitive load C_L = 50 pF		-	8	ns
$t_{w(CKH)}$ (1)	I^2S clock high time	Master f_{PCLK} = 16 MHz, audio freq = 48 K		317	320	
$t_{w(CKL)}$ (1)	I^2S clock low time			333	336	
$t_{v(WS)}$ (1)	WS valid time	Master mode		3	-	
$t_{h(WS)}$ (1)	WS hold time	Master mode	I2S2	0	-	
			I2S3	0	-	
$t_{su(WS)}$ (1)	WS setup time	Slave mode	I2S2	4	-	
			I2S3	9	-	
$t_{h(WS)}$ (1)	WS hold time	Slave mode		0	-	
DuCy(SCK)	I2S slave input clock duty cycle	Slave mode		30	70	%
$t_{su(SD\_MR)}$ (1)	Data input setup time	Master receiver	I2S2	8	-	ns
			I2S3	10	-	
$t_{su(SD\_SR)}$ (1)		Slave receiver	I2S2	3	-	
			I2S3	8	-	
$t_{h(SD\_MR)}$ (1)	Data input hold time	Master receiver	I2S2	2	-	
			I2S3	4	-	
$t_{h(SD\_SR)}$ (1)		Slave receiver	I2S2	2	-	
			I2S3	4	-	
$t_{v(SD\_ST)}$ (1)(3)	Data output valid time	Slave transmitter (after enable edge)	I2S2	23	-	
			I2S3	33	-	
$t_{h(SD\_ST)}$ (1)	Data output hold time	Slave transmitter (after enable edge)	I2S2	29	-	
			I2S3	27	-	
$t_{v(SD\_MT)}$ (1)	Data output valid time	Master transmitter (after enable edge)	I2S2	-	5	
			I2S3	-	2	
$t_{h(SD\_MT)}$ (1)	Data output hold time	Master transmitter (after enable edge)	I2S2	11	-	
			I2S3	4	-	

1. Based on design simulation and/or characterization results, not tested in production.

Table 47. USB OTG FS electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, refer to USB Specification - Chapter 7 (version 2.0).

Ethernet characteristics

Table 48 showns the Ethernet operating voltage.

Table 48. Ethernet DC electrical characteristics

Symbol		Parameter	Min.(1)	Max.(1)	Unit
Input level	V_{DD}	Ethernet operating voltage	3.0	3.6	V

1. All the voltages are measured from the local ground potential.

Table 49 gives the list of Ethernet MAC signals for the SMI (station management interface) and *Figure 31* shows the corresponding timing diagram.

Figure 31. Ethernet SMI timing diagram

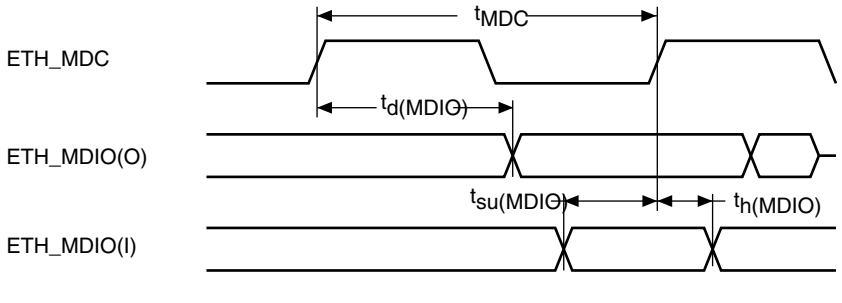


Table 49. Dynamic characteristics: Ethernet MAC signals for SMI

Symbol	Rating	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time (1.71 MHz, AHB = 72 MHz)	583	583.5	584	ns
$t_{d(MDIO)}$	MDIO write data valid time	13.5	14.5	15.5	ns
$t_{su(MDIO)}$	Read data setup time	35	-	-	ns
$t_{h(MDIO)}$	Read data hold time	0	-	-	ns

Table 52. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 52*.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 53. R_{AIN} max for f_{ADC} = 14 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

1. Based on characterization, not tested in production.

7 Part numbering

Table 62. Ordering information scheme

Example: STM32 F 105 R C T 6 V xxx TR

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

105 = connectivity, USB OTG FS

107 = connectivity, USB OTG FS & Ethernet

Pin count

R = 64 pins

V = 100 pins

Flash memory size

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

C = 256 Kbytes of Flash memory

Package

H = BGA

T = LQFP

Temperature range

6 = Industrial temperature range, –40 to 85 °C.

7 = Industrial temperature range, –40 to 105 °C.

Software option

Internal code or Blank

Options

xxx = programmed parts

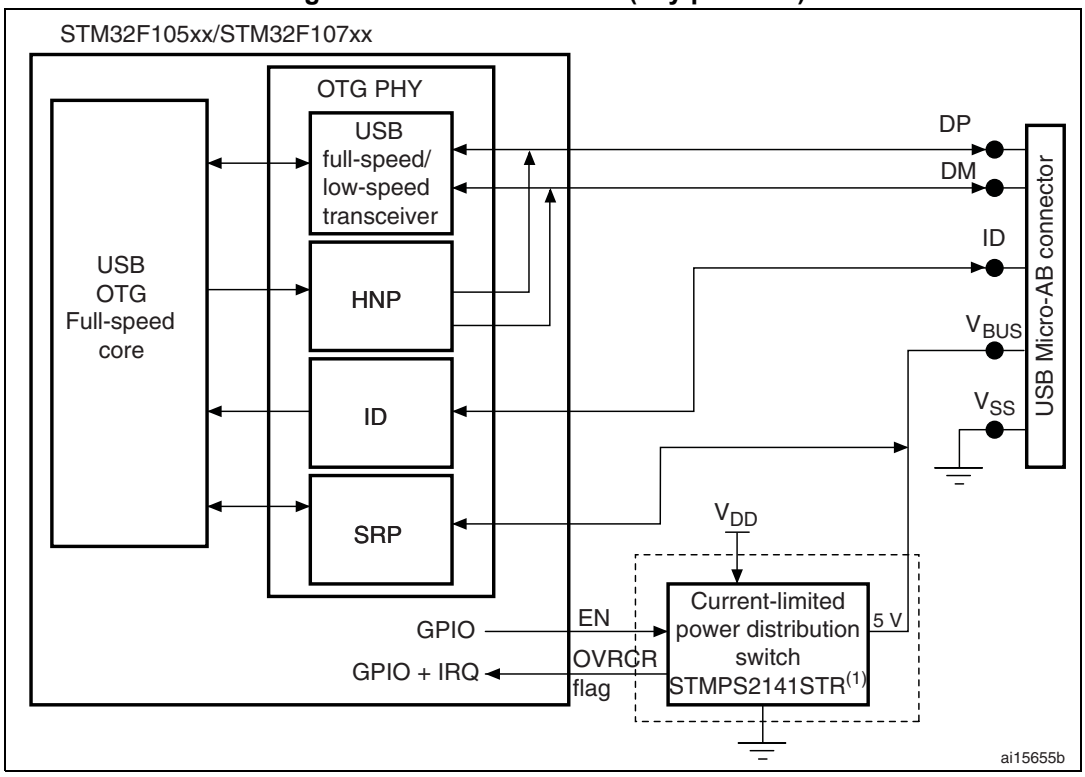
Packing

Blank = tray

TR = tape and reel

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, contact your nearest ST sales office.

Figure 52. OTG connection (any protocol)



1. STMPS2141STR needed only if the application has to support bus-powered devices.

Table 65. Document revision history (continued)

Date	Revision	Changes
06-Mar-2015	8	Updated *Table 40: LFBGA100 – 100-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data*, *Table 59: LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data* and *Table 60: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data* Updated *Figure 14: High-speed external clock source AC timing diagram*; *Figure 39: LFBGA100 - 10 x 10 mm low profile fine pitch ball grid array package outline*, *Figure 43: LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package outline*, *Figure 44: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint*, *Figure 46: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Figure 47: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint* Added *Figure 45: LQFP100 marking example (package top view)*, *Figure 48: LQFP64 marking example (package top view)*
3-Sept-2015	9	Updated: – *Table 19: Peripheral current consumption* – *Figure 44: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint* – *Table 58: LFBGA100 recommended PCB design rules (0.8 mm pitch BGA)*
22-Mar-2017	10	Updated: – *Table 5: Pin definitions* – *Section 6: Package information* Added: – *Figure 42: LFBGA100 marking example (package top view)*