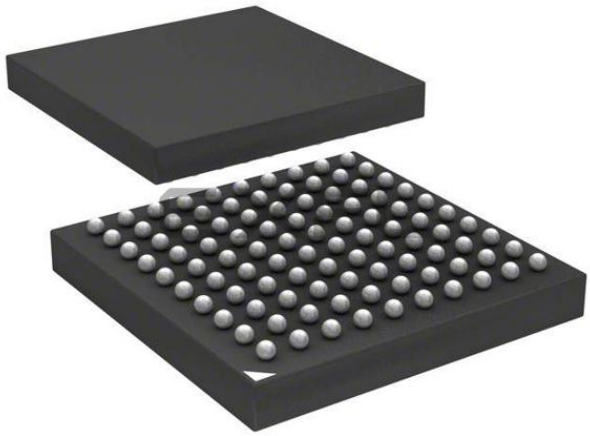

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	80
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f105vbh6

List of figures

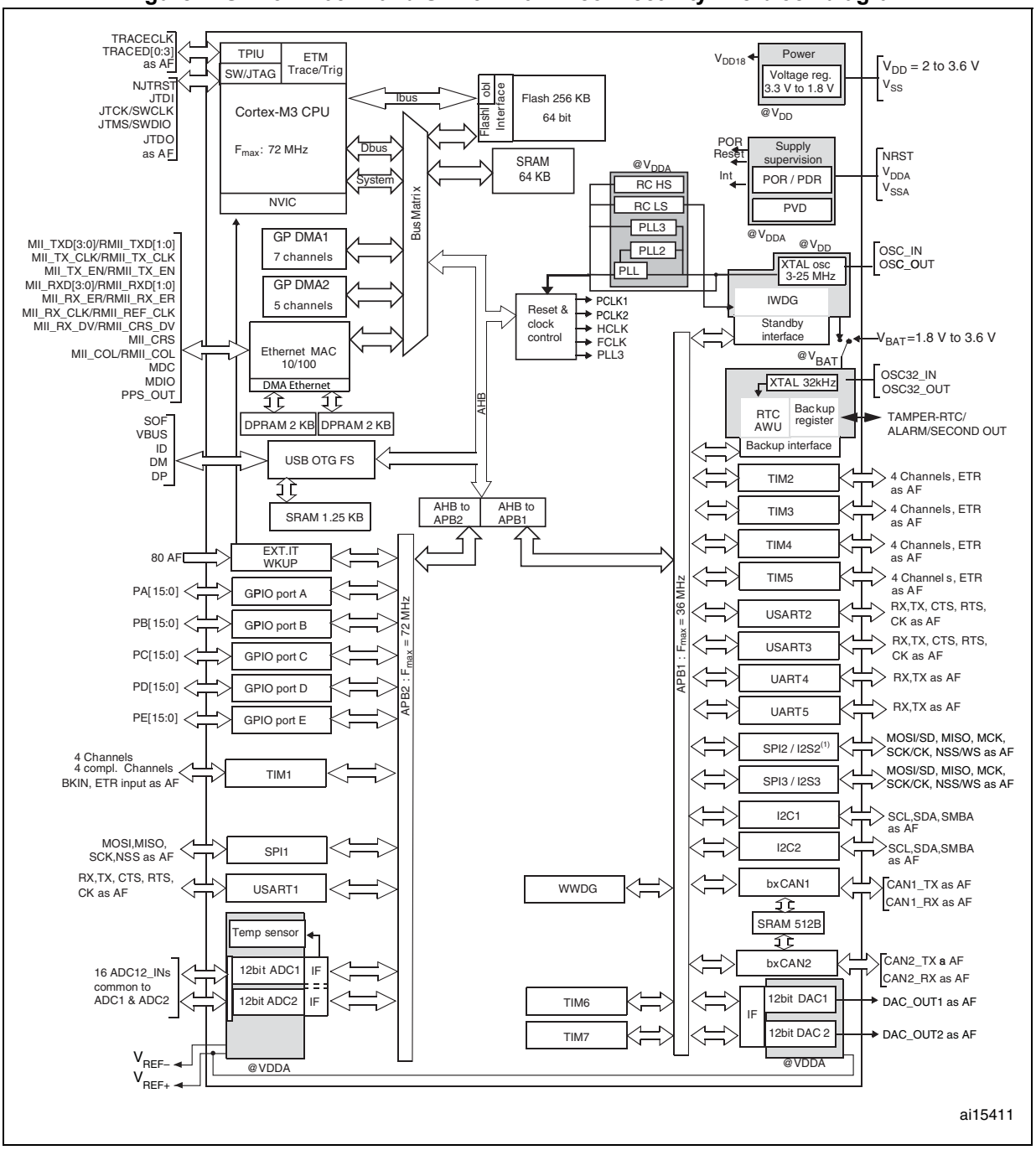
Table 2. STM32F105xx and STM32F107xx features and peripheral counts (continued)

Peripherals[1]		STM32F105Rx	STM32F107Rx	STM32F105Vx	STM32F107Vx
Communication interfaces	SPI(I^2S)[2]	3(2)	3(2)	3(2)	3(2)
	I^2C	2	1	2	1
	USART	5			
	USB OTG FS	Yes			
	CAN	2			
GPIOs		51		80	
12-bit ADC Number of channels		2 16			
12-bit DAC Number of channels		2 2			
CPU frequency		72 MHz			
Operating voltage		2.0 to 3.6 V			
Operating temperatures		Ambient temperatures: –40 to +85 °C /–40 to +105 °C Junction temperature: –40 to + 125 °C			

1. Refer to *Table 5: Pin definitions* for peripheral availability when the I/O pins are shared by the peripherals required by the application.
2. The SPI2 and SPI3 interfaces give the flexibility to work in either the SPI mode or the I^2S audio mode.

2.3 Overview

Figure 1. STM32F105xx and STM32F107xx connectivity line block diagram



1. T_A = –40 °C to +85 °C (suffix 6, see *Table 62*) or –40 °C to +105 °C (suffix 7, see *Table 62*), junction temperature up to 105 °C or 125 °C, respectively.
2. AF = alternate function on I/O port pin.

2.3.6 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 20 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

2.3.7 Clocks and startup

System clock selection is performed on startup, however, the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 3-25 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

A single 25 MHz crystal can clock the entire system including the ethernet and USB OTG FS peripherals. Several prescalers and PLLs allow the configuration of the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz. The maximum allowed frequency of the low speed APB domain is 36 MHz. Refer to *Figure 59: USB O44TG FS + Ethernet solution on page 100*.

The advanced clock controller clocks the core and all peripherals using a single crystal or oscillator. In order to achieve audio class performance, an audio crystal can be used. In this case, the I^2S master clock can generate all standard sampling frequencies from 8 kHz to 96 kHz with less than 0.5% accuracy error. Refer to *Figure 60: USB OTG FS + I2S (Audio) solution on page 100*.

To configure the PLLs, refer to *Table 63 on page 101*, which provides PLL configurations according to the application type.

2.3.8 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1, USART2 (remapped), CAN2 (remapped) or USB OTG FS in device mode (DFU: device firmware upgrade). For remapped signals refer to *Table 5: Pin definitions*.

The USART peripheral operates with the internal 8 MHz oscillator (HSI), however the CAN and USB OTG FS can only function if an external 8 MHz, 14.7456 MHz or 25 MHz clock (HSE) is present.

For full details about the boot loader, refer to AN2606.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.3.13 DMA

The flexible 12-channel general-purpose DMAs (7 channels for DMA1 and 5 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.
Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose, basic and advanced control timers TIMx, DAC, I^2S and ADC.

In the STM32F107xx, there is a DMA controller dedicated for use with the Ethernet (see *Section 2.3.20: Ethernet MAC interface with dedicated DMA and IEEE 1588 support* for more information).

2.3.14 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

For more information, refer to AN2604: "*STM32F101xx and STM32F103xx RTC calibration*", available from *www.st.com*.

USART1, USART2 and USART3 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

2.3.18 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC/SDHC[a] modes.

All SPIs can be served by the DMA controller.

2.3.19 Inter-integrated sound (I^2S)

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 96 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency with less than 0.5% accuracy error owing to the advanced clock controller (see *Section 2.3.7: Clocks and startup*).

Refer to the “Audio frequency precision” tables provided in the “Serial peripheral interface (SPI)” section of the STM32F10xxx reference manual.

2.3.20 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

Peripheral not available on STM32F105xx devices.

The STM32F107xx devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard media-independent interface (MII) or a reduced media-independent interface (RMII). The STM32F107xx requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). the PHY is connected to the STM32F107xx MII port using as many as 17 signals (MII) or 9 signals (RMII) and can be clocked using the 25 MHz (MII) or 50 MHz (RMII) output from the STM32F107xx.

The STM32F107xx includes the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors (see the STM32F105xx/STM32F107xx reference manual for details)
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support

a. SDHC = Secure digital high capacity.

- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes, that is 4 Kbytes in total
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 with the timestamp comparator connected to the TIM2 trigger input
- Triggers interrupt when system time becomes greater than target time

2.3.21 Controller area network (CAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). The 256 bytes of SRAM which are allocated for each CAN (512 bytes in total) are not shared with any other peripheral.

2.3.22 Universal serial bus on-the-go full-speed (USB OTG FS)

The STM32F105xx and STM32F107xx connectivity line devices embed a USB OTG full-speed (12 Mb/s) device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- 1.25 KB of SRAM used exclusively by the endpoints (not shared with any other peripheral)
- 4 bidirectional endpoints
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected
- the SOF output can be used to synchronize the external audio DAC clock in isochronous mode
- in accordance with the USB 2.0 Specification, the supported transfer speeds are:
  - in Host mode: full speed and low speed
  - in Device mode: full speed

2.3.23 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

I/Os on APB2 with up to 18 MHz toggling speed

4 Memory mapping

The memory map is shown in *Figure 5*.

Figure 5. Memory map

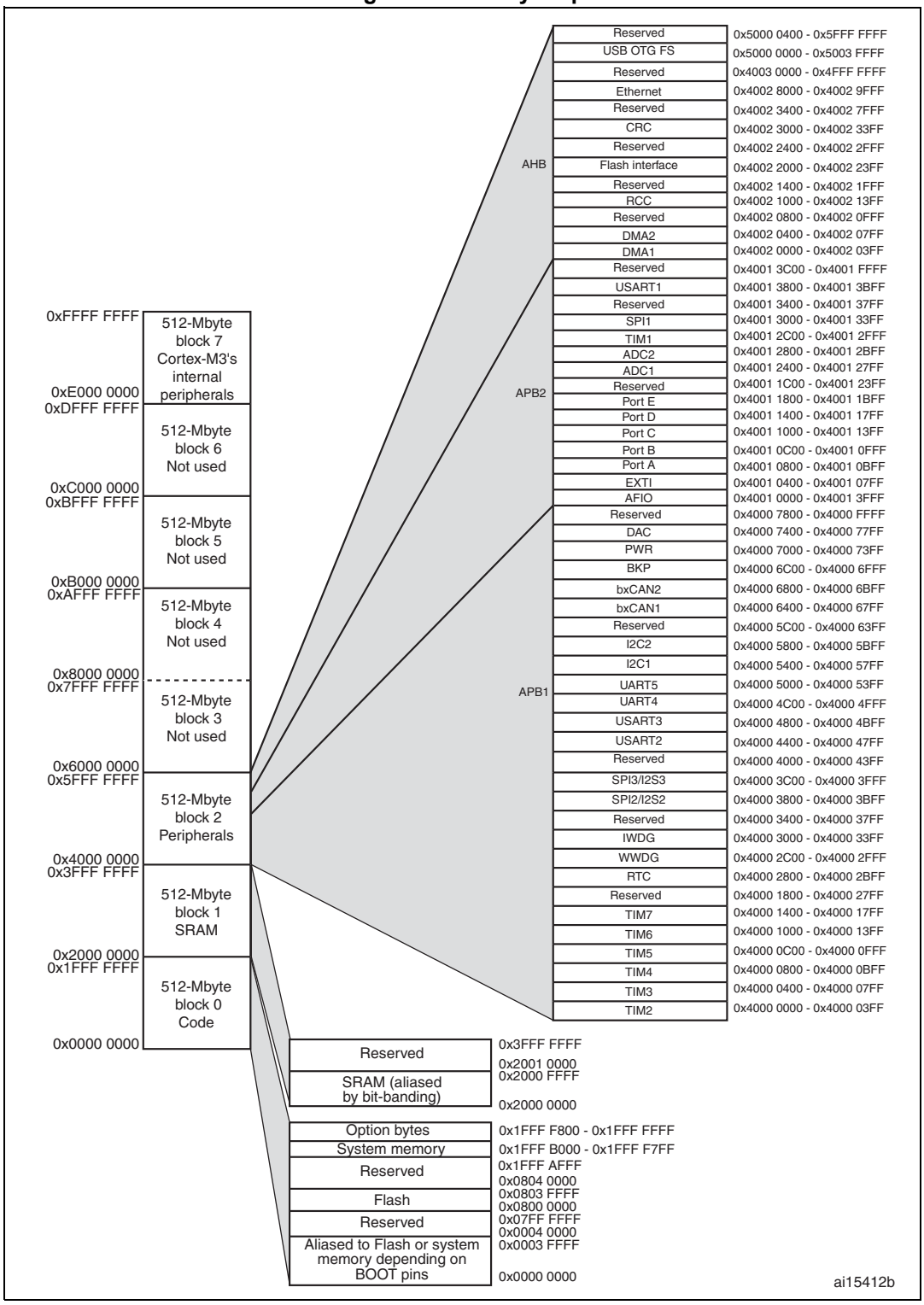
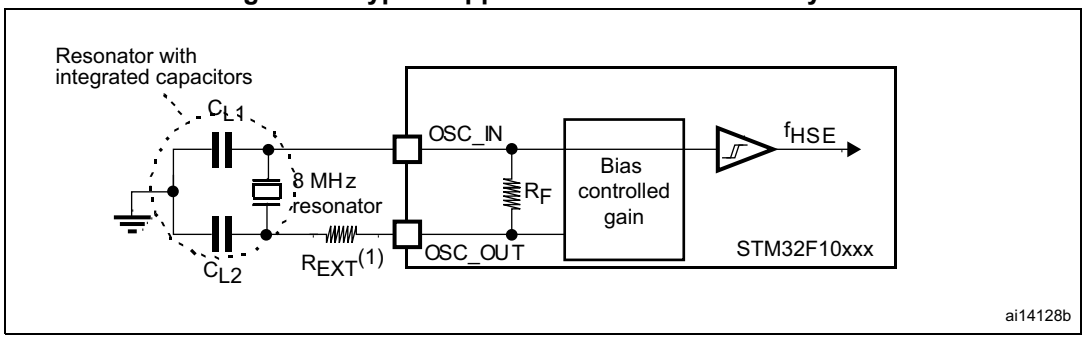


Table 19. Peripheral current consumption

Peripheral		Typical consumption at 25 °C	Unit
AHB (up to 72 MHz)	DMA1	14.03	µA/MHz
	DMA2	9.31	
	OTG_fs	111.11	
	ETH-MAC	56.25	
	CRC	1.11	
	BusMatrix(1)	15.97	
APB1(up to 36MHz)	APB1-Bridge	9.72	µA/MHz
	TIM2	33.61	
	TIM3	33.06	
	TIM4	32.50	
	TIM5	31.94	
	TIM6	6.11	
	TIM7	6.11	
	SPI2/I2S2(2)	7.50	
	SPI3/I2S3(2)	7.50	
	USART2	10.83	
	USART3	11.11	
	UART4	10.83	
	UART5	10.56	
	I2C1	11.39	
	I2C2	11.11	
	CAN1	19.44	
	CAN2	18.33	
	DAC(3)	8.61	
	WWDG	3.33	
	PWR	2.22	
	BKP	0.83	
	IWDG	3.89	

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 16*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Figure 16. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 23*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 23. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	5	-	MΩ
$C^{(2)}$	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 kΩ	-	-	15	pF
I_2	LSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS}	-	-	1.4	µA
g_m	Oscillator Transconductance	-	5	-	-	µA/V

Table 32. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]		Unit
				8/48 MHz	8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP100 package compliant with IEC61967-2	0.1 to 30 MHz	9	9	dBµV
			30 to 130 MHz	26	13	
			130 MHz to 1GHz	25	31	
			EMI Level	4	4	-

5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 33. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to JESD22-C101	II	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 34. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

5.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/-20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 7*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 7*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 37* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 37. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(2)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port I_{IO} =+ 8mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (2)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4	-	
V_{OL}(1)(3)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH}(2)(3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–1.3	-	
V_{OL}(1)(3)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(2)(3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
3. Based on characterization data, not tested in production.

5.3.18 DAC electrical specifications

Table 56. DAC characteristics

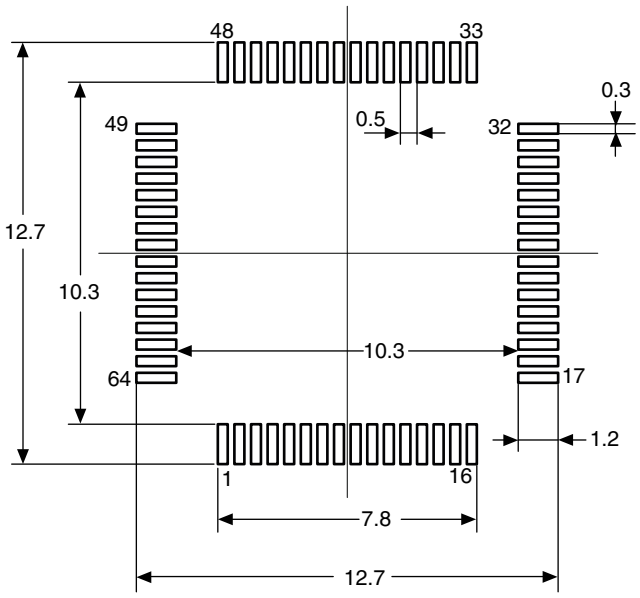
Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	2.4	-	3.6	V	-
V_{REF+}	Reference supply voltage	2.4	-	3.6	V	V_{REF+} must always be below V_{DDA}
V_{SSA}	Ground	0	-	0	V	-
R_{LOAD}(1)	Resistive load with buffer ON	5	-	-	kΩ	-
R_O(1)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(1)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x155) to (0xEAB) at V_{REF+} = 2.4 V
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer OFF	-	-	V_{REF+} – 1LSB	V	
$I_{DDVREF+}$	DAC DC current consumption in quiescent mode (Standby mode)	-	-	220	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
I_{DDA}	DAC DC current consumption in quiescent mode (Standby mode)	-	-	380	µA	With no load, middle code (0x800) on the inputs
		-	-	480	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
DNL(2)	Differential non linearity Difference between two consecutive code-1LSB)	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration.
		-	-	±2	LSB	Given for the DAC in 12-bit configuration.
INL(2)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±1	LSB	Given for the DAC in 10-bit configuration.
		-	-	±4	LSB	Given for the DAC in 12-bit configuration.

Table 60.LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

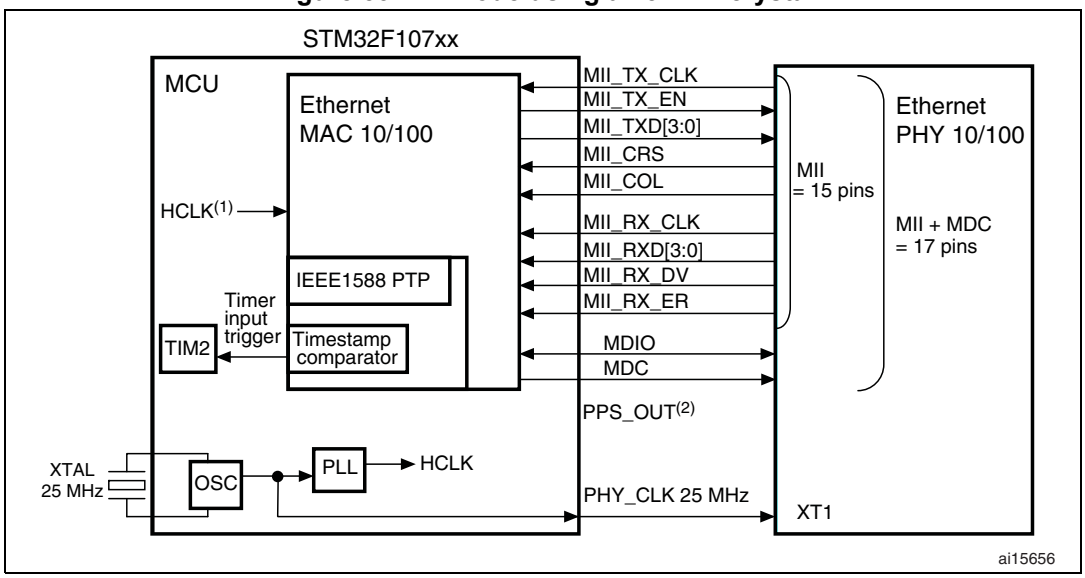
Figure 47.LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint



1. Dimensions are in millimeters.

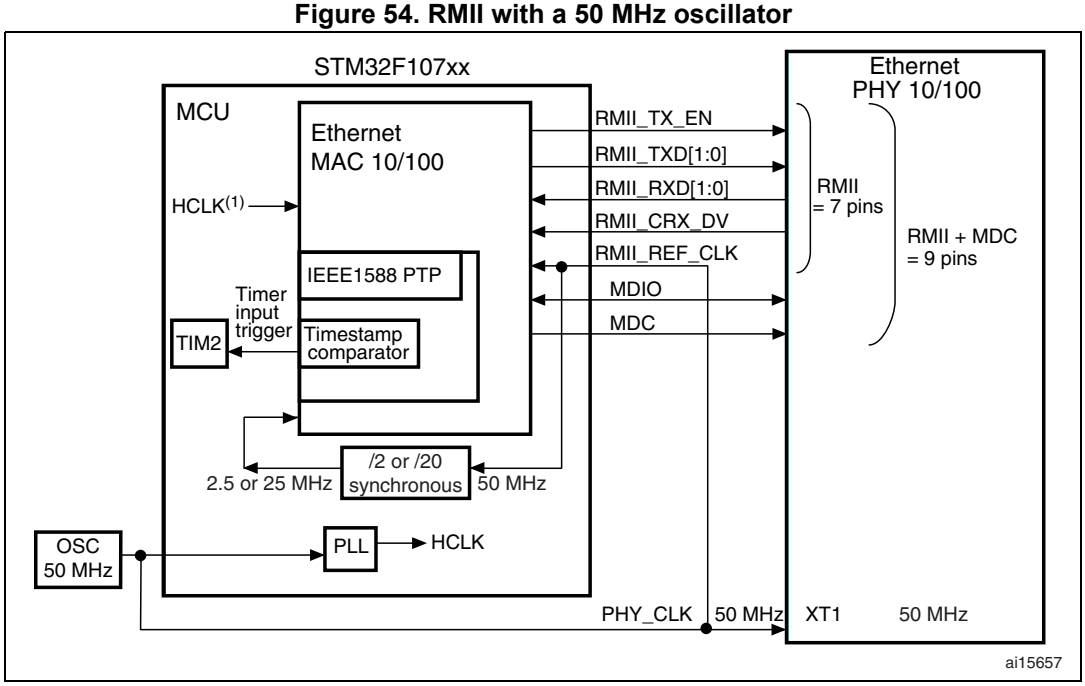
A.2 Ethernet interface solutions

Figure 53. MII mode using a 25 MHz crystal



1. HCLK must be greater than 25 MHz.
2. Pulse per second when using IEEE1588 PTP, optional signal.

Figure 54. RMII with a 50 MHz oscillator



1. HCLK must be greater than 25 MHz.

A.3 Complete audio player solutions

Two solutions are offered, illustrated in *Figure 57* and *Figure 58*.

Figure 57 shows storage media to audio DAC/amplifier streaming using a software Codec. This solution implements an audio crystal to provide audio class I^2S accuracy on the master clock (0.5% error maximum, see the Serial peripheral interface section in the reference manual for details).

Figure 57. Complete audio player solution 1

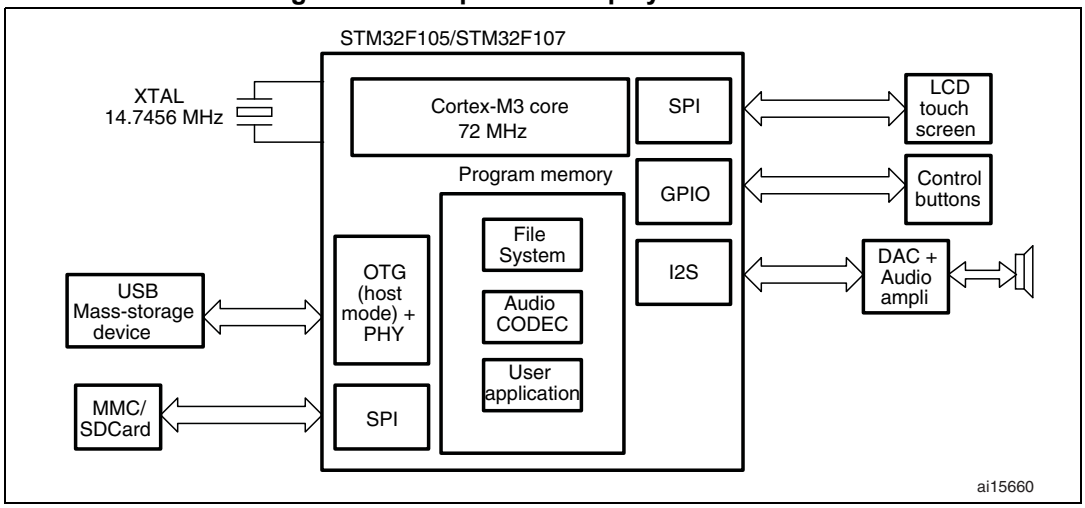


Figure 58 shows storage media to audio Codec/amplifier streaming with SOF synchronization of input/output audio streaming using a hardware Codec.

Figure 58. Complete audio player solution 2

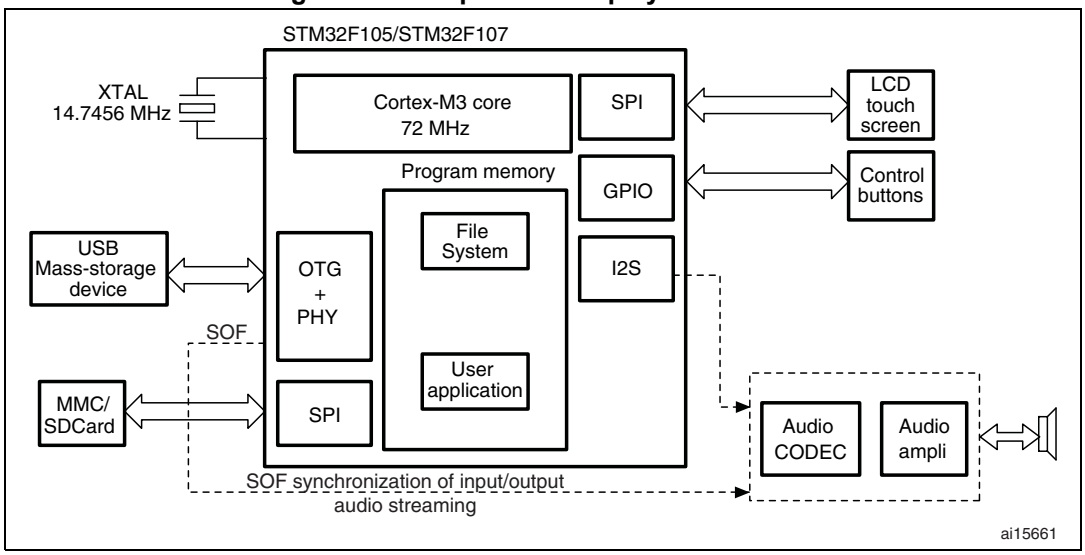


Table 64. Applicative current consumption in Run mode, code with data processing running from Flash

Symbol	parameter	Conditions[1]	Typ[2]	Max[2]		Unit
				85 °C	105 °C	
I_{DD}	Supply current in run mode	External clock, all peripherals enabled except ethernet, HSE = 8 MHz, f_{HCLK} = 72 MHz, no MCO	57	63	64	mA
		External clock, all peripherals enabled except ethernet, HSE = 14.74 MHz, f_{HCLK} = 72 MHz, no MCO	60.5	67	68	
		External clock, all peripherals enabled except OTG, HSE = 25 MHz, f_{HCLK} = 72 MHz, MCO = 25 MHz	53	60.7	61	
		External clock, all peripherals enabled, HSE = 25 MHz, f_{HCLK} = 72 MHz, MCO = 25 MHz	60.5	65.5	66	
		External clock, all peripherals enabled, HSE = 25 MHz, f_{HCLK} = 72 MHz, MCO = 50 MHz	64	69.7	70	
		External clock, all peripherals enabled, HSE = 50 MHz[3], f_{HCLK} = 72 MHz, no MCO	62.5	67.5	68	
		External clock, only OTG enabled, HSE = 8 MHz, f_{HCLK} = 48 MHz, no MCO	26.7	None	None	
		External clock, only ethernet enabled, HSE = 25 MHz, f_{HCLK} = 25 MHz, MCO = 25 MHz	14.3	None	None	

1. V_{DD} = 3.3 V.
2. Based on characterization, not tested in production.
3. External oscillator.

8 Revision history

Table 65. Document revision history

Date	Revision	Changes
18-Dec-2008	1	Initial release.
20-Feb-2009	2	I/O information clarified *on page 1. Figure 4: STM32F105xxx and STM32F107xxx connectivity line BGA100 ballout top view* corrected. *Section 2.3.8: Boot modes* updated. PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column, plus small additional changes in *Table 5: Pin definitions*. Consumption values modified in *Section 5.3.5: Supply current characteristics*. Note modified in *Table 13: Maximum current consumption in Run mode, code with data processing running from Flash* and *Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM*. *Table 20: High-speed external user clock characteristics* and *Table 21: Low-speed external user clock characteristics* modified. *Table 27: PLL characteristics* modified and *Table 28: PLL2 and PLL3 characteristics* added.

Table 65. Document revision history (continued)

Date	Revision	Changes
14-Sep-2009	4	Document status promoted from Preliminary data to full datasheet. Number of DACs corrected in *Table 3: STM32F105xx and STM32F107xx family versus STM32F103xx family*. *Note 5* added in *Table 5: Pin definitions*. V_{RERINT} and T_{Coeff} added to *Table 12: Embedded internal reference voltage*. Values added to *Table 13: Maximum current consumption in Run mode, code with data processing running from Flash*, *Table 14: Maximum current consumption in Run mode, code with data processing running from RAM* and *Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM*. Typical I_{DD_VBAT} value added in *Table 16: Typical and maximum current consumptions in Stop and Standby modes*. *Figure 10: Typical current consumption on VBAT with RTC on vs. temperature at different VBAT values* added. Values modified in *Table 17: Typical current consumption in Run mode, code with data processing running from Flash* and *Table 18: Typical current consumption in Sleep mode, code running from Flash or RAM*. f_{HSE_ext} min modified in *Table 20: High-speed external user clock characteristics*. C_{L1} and C_{L2} replaced by C in *Table 22: HSE 3-25 MHz oscillator characteristics* and *Table 23: LSE oscillator characteristics (fLSE = 32.768 kHz)*, notes modified and moved below the tables. *Note 1* modified below *Figure 16: Typical application with an 8 MHz crystal*. Conditions removed from *Table 26: Low-power mode wakeup timings*. Standards modified in *Section 5.3.10: EMC characteristics on page 54*, conditions modified in *Table 31: EMS characteristics*. Jitter maximum values added to *Table 27: PLL characteristics* and *Table 28: PLL2 and PLL3 characteristics*. R_{PU} and R_{PD} modified in *Table 36: I/O static characteristics*. Condition added for $V_{NF(NRST)}$ parameter in *Table 39: NRST pin characteristics*. Note removed and R_{PD}, R_{PU} values added in *Table 46: USB OTG FS DC electrical characteristics*. *Table 48: Ethernet DC electrical characteristics* added. Parameter values added to *Table 49: Dynamic characteristics: Ethernet MAC signals for SMI*, *Table 50: Dynamic characteristics: Ethernet MAC signals for RMII* and *Table 51: Dynamic characteristics: Ethernet MAC signals for MII*. C_{ADC} and R_{AIN} parameters modified in *Table 52: ADC characteristics*. R_{AIN} max values modified in *Table 53: RAIN max for fADC = 14 MHz*. *Table 56: DAC characteristics* modified. *Figure 38: 12-bit buffered /non-buffered DAC* added. *Table 64: Applicative current consumption in Run mode, code with data processing running from Flash* added. Small text changes.

Table 65. Document revision history (continued)

Date	Revision	Changes
06-Mar-2015	8	Updated *Table 40: LFBGA100 – 100-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data*, *Table 59: LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data* and *Table 60: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data* Updated *Figure 14: High-speed external clock source AC timing diagram*; *Figure 39: LFBGA100 - 10 x 10 mm low profile fine pitch ball grid array package outline*, *Figure 43: LQFP100 – 14 x 14 mm 100 pin low-profile quad flat package outline*, *Figure 44: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint*, *Figure 46: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Figure 47: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint* Added *Figure 45: LQFP100 marking example (package top view)*, *Figure 48: LQFP64 marking example (package top view)*
3-Sept-2015	9	Updated: – *Table 19: Peripheral current consumption* – *Figure 44: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint* – *Table 58: LFBGA100 recommended PCB design rules (0.8 mm pitch BGA)*
22-Mar-2017	10	Updated: – *Table 5: Pin definitions* – *Section 6: Package information* Added: – *Figure 42: LFBGA100 marking example (package top view)*