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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f105vct6w

List of figures

2.2 Full compatibility throughout the family

The STM32F105xx and STM32F107xx constitute the connectivity line family whose members are fully pin-to-pin, software and feature compatible.

The STM32F105xx and STM32F107xx are a drop-in replacement for the low-density (STM32F103x4/6), medium-density (STM32F103x8/B) and high-density (STM32F103xC/D/E) performance line devices, allowing the user to try different memory densities and peripherals providing a greater degree of freedom during the development cycle.

Table 3. STM32F105xx and STM32F107xx family versus STM32F103xx family(1)

<table>
<tr><th>STM32 device</th><th colspan="2">Low-density STM32F103xx devices</th><th colspan="3">Medium-density STM32F103xx devices</th><th colspan="3">High-density STM32F103xx devices</th><th colspan="3">STM32F105xx</th><th colspan="2">STM32F107xx</th></tr>
<tr><td>Flash size (KB)</td><td>16</td><td>32</td><td>32</td><td>64</td><td>128</td><td>256</td><td>384</td><td>512</td><td>64</td><td>128</td><td>256</td><td>128</td><td>256</td></tr>
<tr><td>RAM size (KB)</td><td>6</td><td>10</td><td>10</td><td>20</td><td>20</td><td>48</td><td>64</td><td>64</td><td>64</td><td>64</td><td>64</td><td>64</td><td>64</td></tr>
<tr><td>144 pins</td><td colspan="5" rowspan="2"></td><td colspan="3" rowspan="3">5 × USARTs
4 × 16-bit timers,
2 × basic timers, 3 × SPIs,
2 × I²Ss, 2 × I2Cs, USB,
CAN, 2 × PWM timers
3 × ADCs, 2 × DACs,
1 × SDIO, FSMC (100- and 144-pin packages(2))</td><td colspan="5"></td></tr>
<tr><td>100 pins</td><td colspan="3" rowspan="2">3 × USARTs
3 × 16-bit timers
2 × SPIs,
2 × I²Cs, USB, CAN,
1 × PWM timer
2 × ADCs</td><td colspan="3" rowspan="2">5 × USARTs,
4 × 16-bit timers,
2 × basic timers,
3 × SPIs,
2 × I²Ss,
2 × I2Cs,
USB OTG FS,
2 × CANs,
1 × PWM timer,
2 × ADCs,
2 × DACs</td><td colspan="2" rowspan="2">5 × USARTs,
4 × 16-bit timers,
2 × basic timers,
3 × SPIs,
2 × I²S,
1 × I2C,
USB OTG FS,
2 × CANs,
1 × PWM timer,
2 × ADCs,
2 × DACs,
Ethernet</td></tr>
<tr><td>64 pins</td><td colspan="2" rowspan="3">2 × USARTs
2 × 16-bit timers
1 × SPI, 1 × I²C, USB, CAN,
1 × PWM timer
2 × ADCs</td><td colspan="2" rowspan="3">2 × USARTs
2 × 16-bit timers
1 × SPI,
1 × I²C,
USB, CAN,
1 × PWM timer
2 × ADCs</td></tr>
<tr><td>48 pins</td><td colspan="3"></td></tr>
<tr><td>36 pins</td><td colspan="3"></td></tr>
</table>

1. Refer to *Table 5: Pin definitions* for peripheral availability when the I/O pins are shared by the peripherals required by the application.
2. Ports F and G are not available in devices delivered in 100-pin packages.

2.3.9 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supplies for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

2.3.10 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.3.11 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop modes.
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode.

2.3.12 Low-power modes

The STM32F105xx and STM32F107xx connectivity line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.
  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm or the USB OTG FS wakeup.

USART1, USART2 and USART3 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

2.3.18 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC/SDHC[a] modes.

All SPIs can be served by the DMA controller.

2.3.19 Inter-integrated sound (I^2S)

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 96 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency with less than 0.5% accuracy error owing to the advanced clock controller (see *Section 2.3.7: Clocks and startup*).

Refer to the “Audio frequency precision” tables provided in the “Serial peripheral interface (SPI)” section of the STM32F10xxx reference manual.

2.3.20 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

Peripheral not available on STM32F105xx devices.

The STM32F107xx devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard media-independent interface (MII) or a reduced media-independent interface (RMII). The STM32F107xx requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). the PHY is connected to the STM32F107xx MII port using as many as 17 signals (MII) or 9 signals (RMII) and can be clocked using the 25 MHz (MII) or 50 MHz (RMII) output from the STM32F107xx.

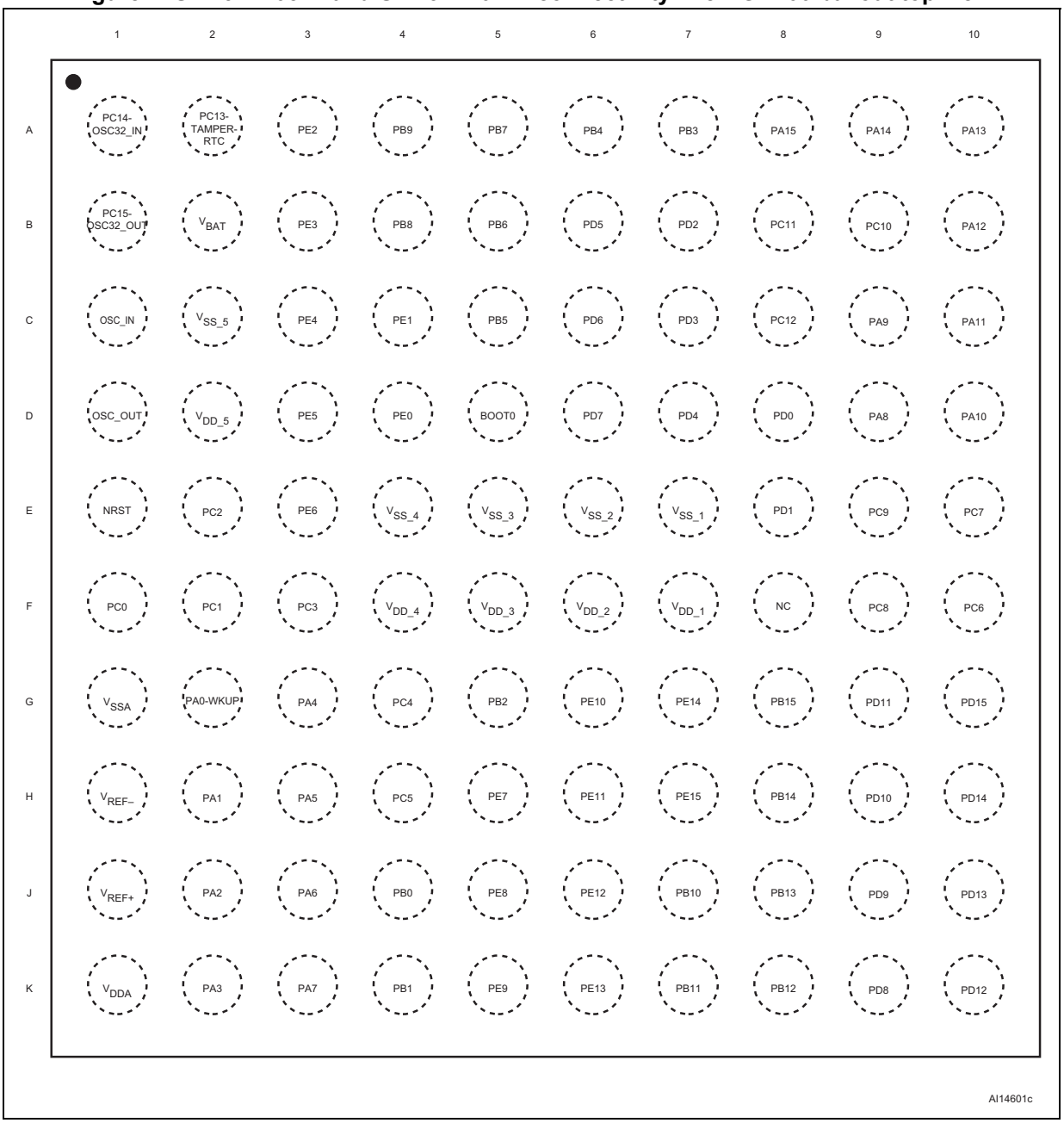
The STM32F107xx includes the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors (see the STM32F105xx/STM32F107xx reference manual for details)
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support

a. SDHC = Secure digital high capacity.

3 Pinouts and pin description

Figure 2. STM32F105xx and STM32F107xx connectivity line BGA100 ballout top view



4 Memory mapping

The memory map is shown in *Figure 5*.

Figure 5. Memory map

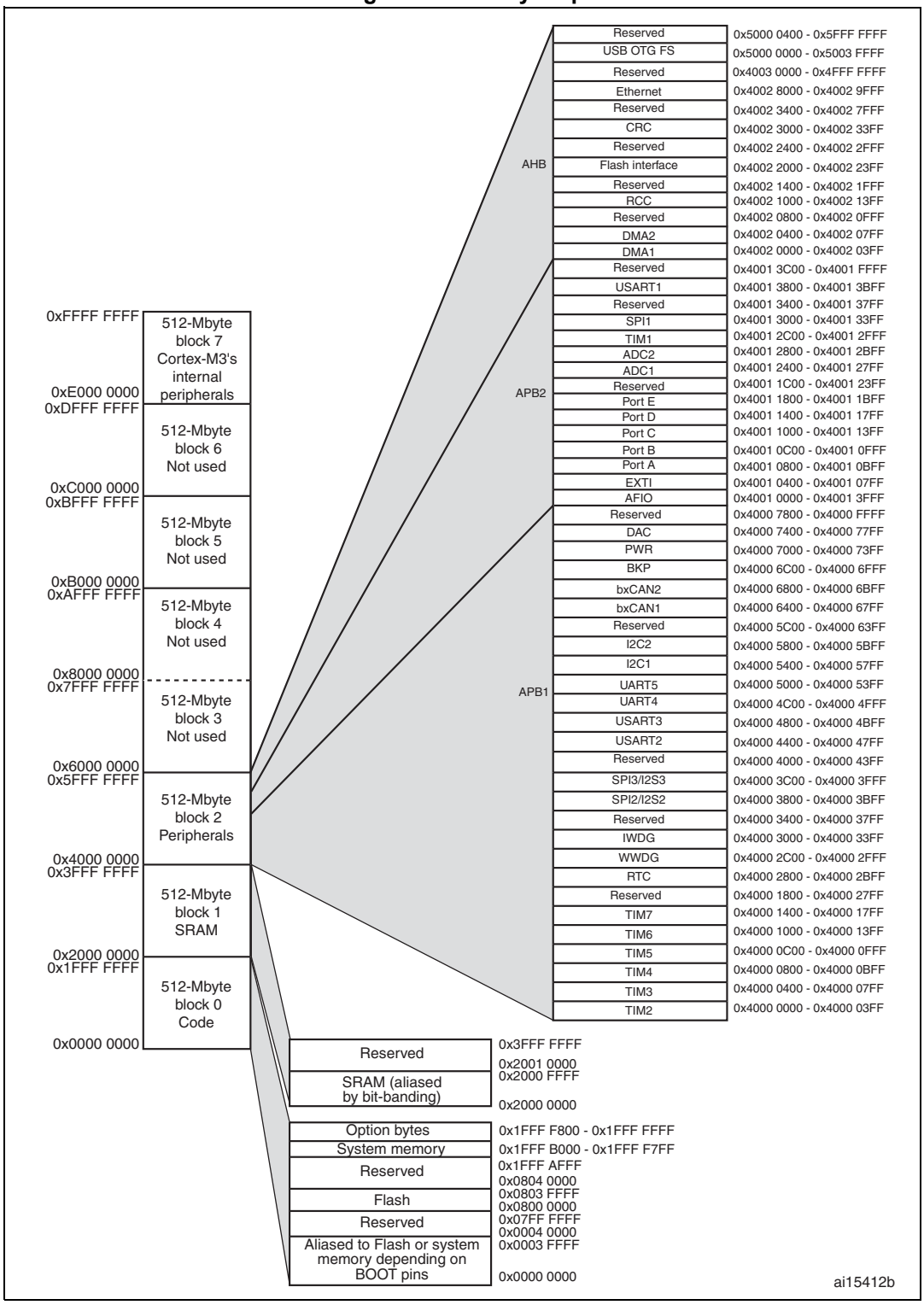


Figure 10. Typical current consumption on V_{BAT} with RTC on vs. temperature at different V_{BAT} values

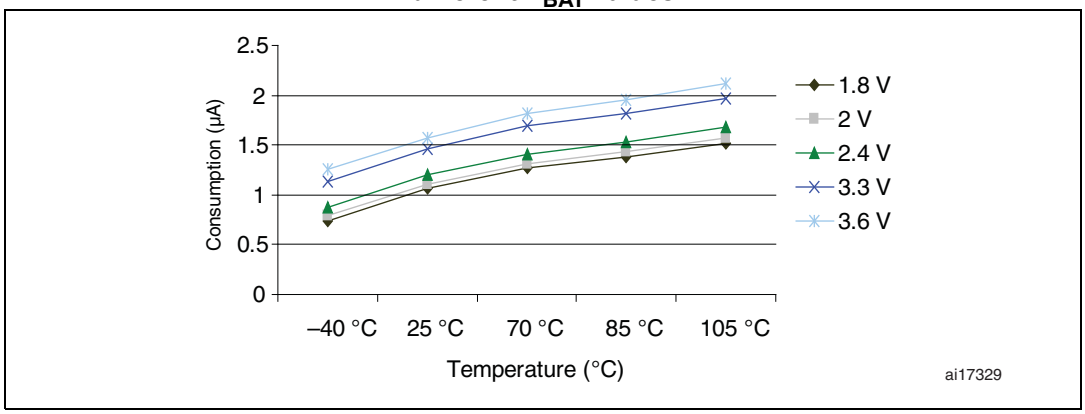


Figure 11. Typical current consumption in Stop mode with regulator in Run mode versus temperature at different V_{DD} values

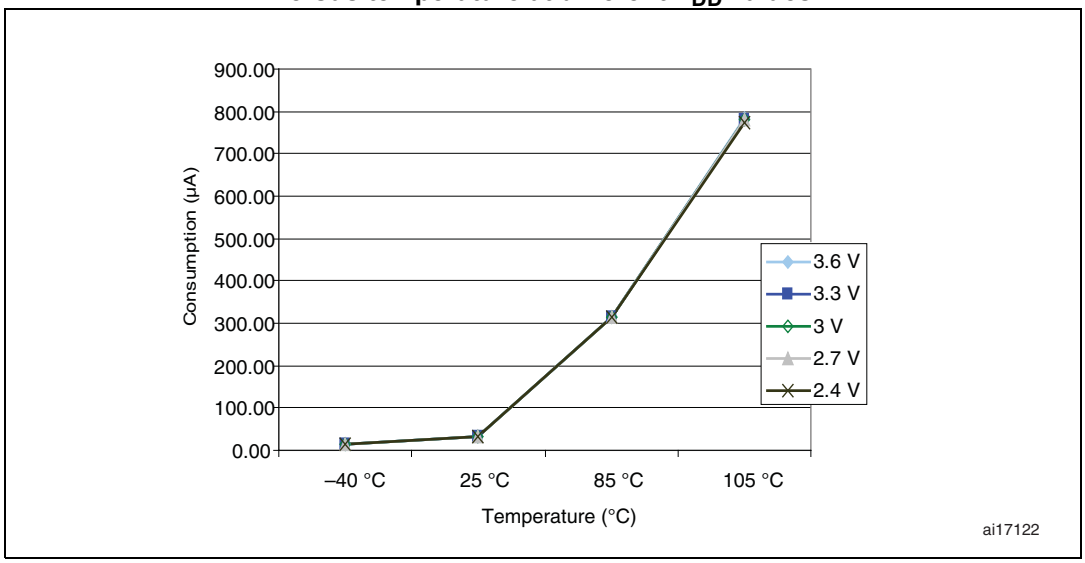


Table 19. Peripheral current consumption

Peripheral		Typical consumption at 25 °C	Unit
AHB (up to 72 MHz)	DMA1	14.03	µA/MHz
	DMA2	9.31	
	OTG_fs	111.11	
	ETH-MAC	56.25	
	CRC	1.11	
	BusMatrix(1)	15.97	
APB1(up to 36MHz)	APB1-Bridge	9.72	µA/MHz
	TIM2	33.61	
	TIM3	33.06	
	TIM4	32.50	
	TIM5	31.94	
	TIM6	6.11	
	TIM7	6.11	
	SPI2/I2S2(2)	7.50	
	SPI3/I2S3(2)	7.50	
	USART2	10.83	
	USART3	11.11	
	UART4	10.83	
	UART5	10.56	
	I2C1	11.39	
	I2C2	11.11	
	CAN1	19.44	
	CAN2	18.33	
	DAC(3)	8.61	
	WWDG	3.33	
	PWR	2.22	
	BKP	0.83	
	IWDG	3.89	

operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 35*

Table 35. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

5.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 36* are derived from tests performed under the conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 36. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO input low level voltage	-	–0.3	-	0.28*(V_{DD}-2 V)+0.8 V	V
	IO FT(1) input low level voltage	-	–0.3	-	0.32*(V_{DD}-2V)+0.75 V	V
V_{IH}	Standard IO input high level voltage	-	0.41*(V_{DD}-2 V)+1.3 V	-	V_{DD}+0.3	V
	IO FT(1) input high level voltage	V_{DD} > 2 V	0.42*(V_{DD}-2 V)+1 V	-	5.5	V
		$V_{DD} \leq$ 2 V			5.2	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis(2)	-	200	-	-	mV
	IO FT Schmitt trigger voltage hysteresis(2)	-	5% V_{DD}(3)	-	-	mV

Table 36. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
I_{lkg}	Input leakage current (4)		$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os	-	-	±1	µA
			V_{IN}= 5 V, I/O FT	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(5)	All pins except for PA10	$V_{IN} = V_{SS}$	30	40	50	kΩ
		PA10		8	11	15	
R_{PD}	Weak pull-down equivalent resistor(5)	All pins except for PA10	$V_{IN} = V_{DD}$	30	40	50	kΩ
		PA10		8	11	15	
C_{IO}	I/O pin capacitance		-	-	5	-	pF

1. FT = Five-volt tolerant. In order to sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
3. With a minimum of 100 mV.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 18* and *Figure 19* for standard I/Os, and in *Figure 20* and *Figure 21* for 5 V tolerant I/Os.

Figure 18. Standard I/O input characteristics - CMOS port

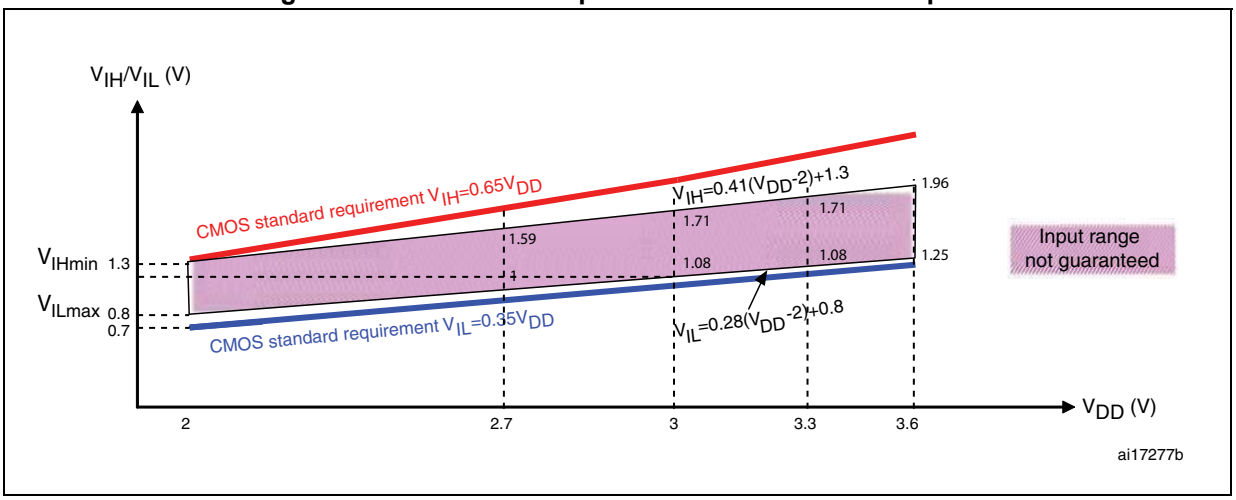


Figure 19. Standard I/O input characteristics - TTL port

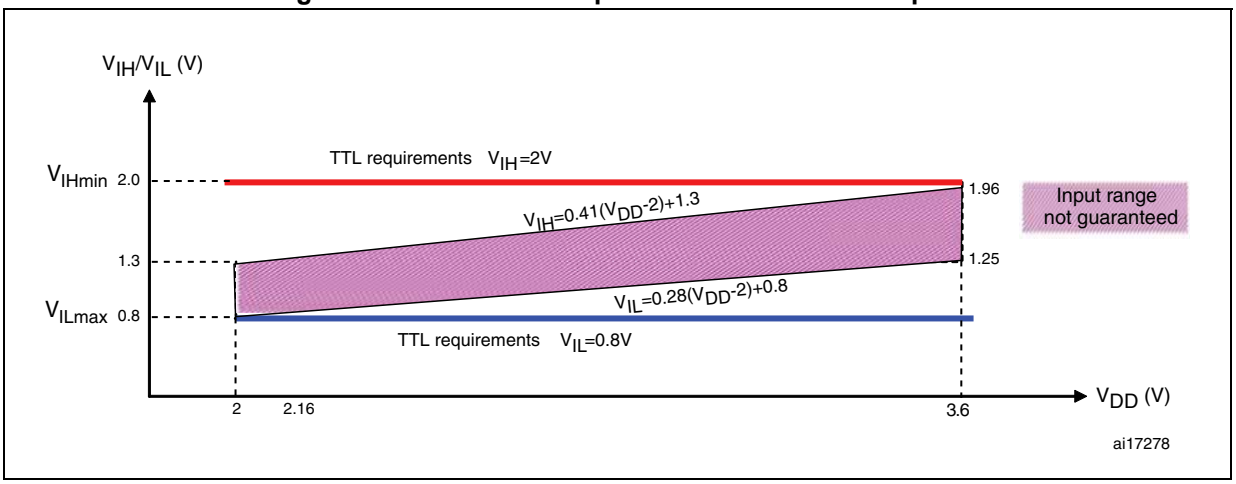


Figure 20. 5 V tolerant I/O input characteristics - CMOS port

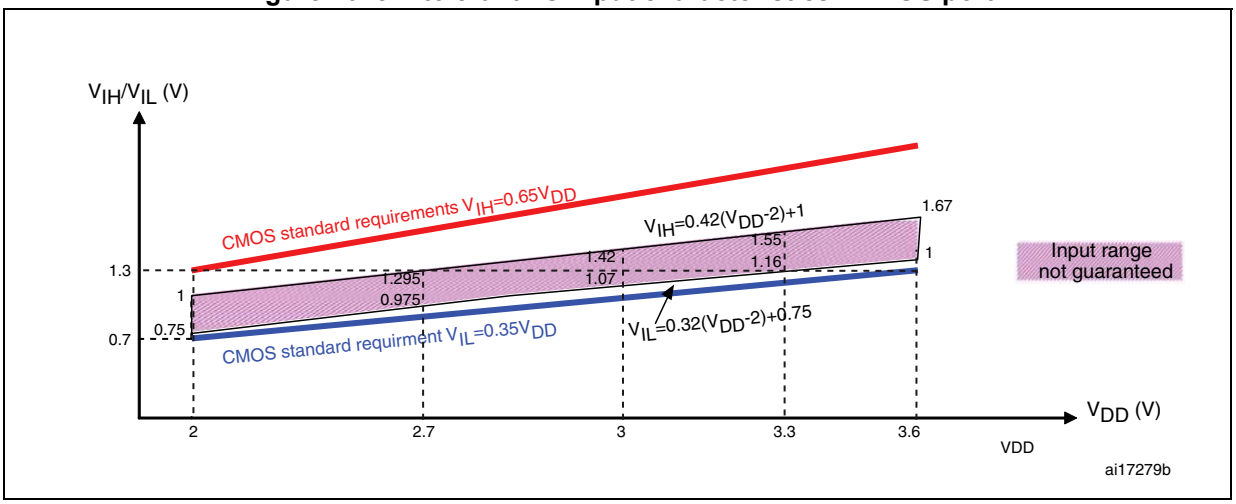
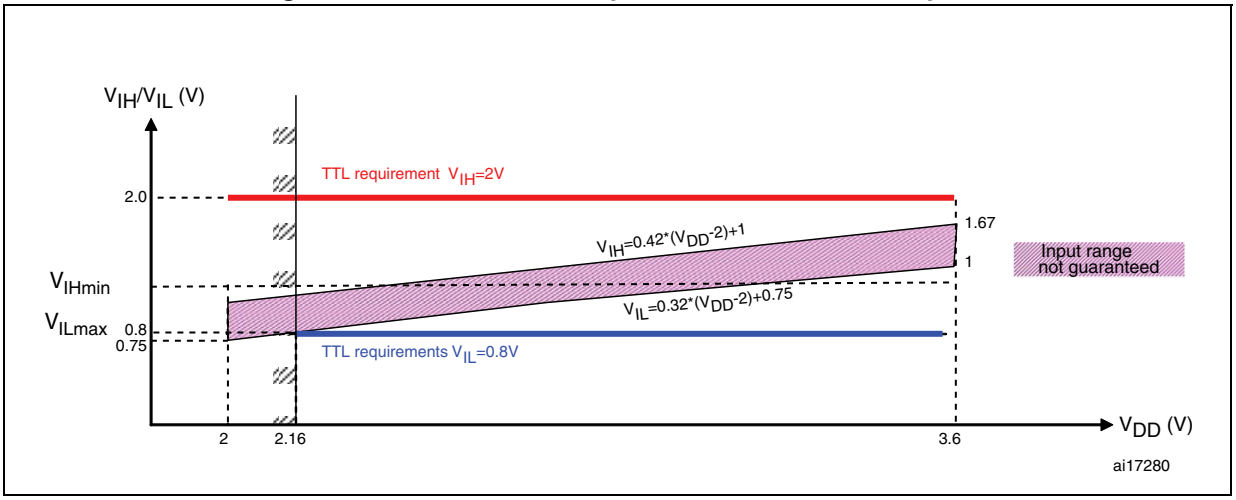


Figure 21. 5 V tolerant I/O input characteristics - TTL port



5.3.16 Communications interfaces

I^2C interface characteristics

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

The STM32F105xx and STM32F107xx I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I^2C characteristics are described in *Table 41*. Refer also to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 41. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(3)	-	0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20 + 0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I^2C frequencies. It must be at least 4 MHz to achieve the fast mode I^2C frequencies and it must be a mulitple of 10 MHz in order to reach I^2C fast mode maximum clock 400 kHz.
3. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

I^2S - SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 43* for SPI or in *Table 44* for I^2S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

Refer to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I^2S).

Table 43. SPI characteristics

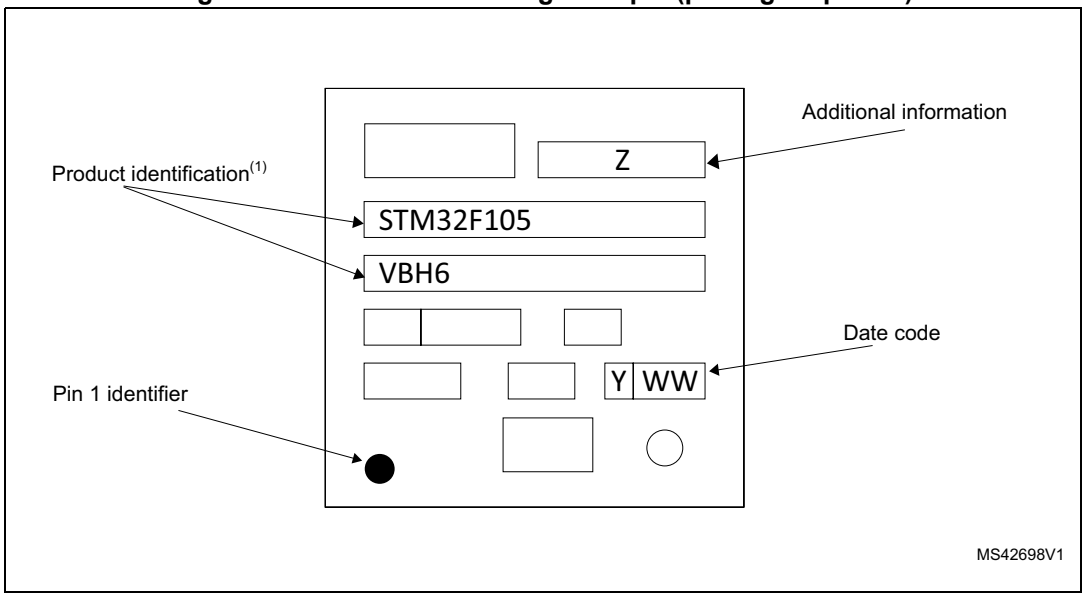
Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode	4 t_{PCLK}	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2 t_{PCLK}	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	50	60	
$t_{su(MI)}$	Data input setup time	Master mode	4	-	
$t_{su(SI)}$		Slave mode	5	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	
$t_{h(SI)}$		Slave mode	5	-	
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK} = 20 MHz	-	3*t_{PCLK}	
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	-	34	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	8	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	32	-	
$t_{h(MO)}$		Master mode (after enable edge)	10	-	

Device marking for LFBGA100

The following figure shows the device marking for the LQFP100 package.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 42. LFBGA100 marking example (package top view)



Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

6.4.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 62: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F103xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Thus: P_{Dmax} = 447 mW

Using the values obtained in *Table 61* T_{Jmax} is calculated as follows:

– For LQFP100, 46 °C/W

T_{Jmax} = 82 °C + (46 °C/W × 447 mW) = 82 °C + 20.6 °C = 102.6 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Table 62: Ordering information scheme*).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 115 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

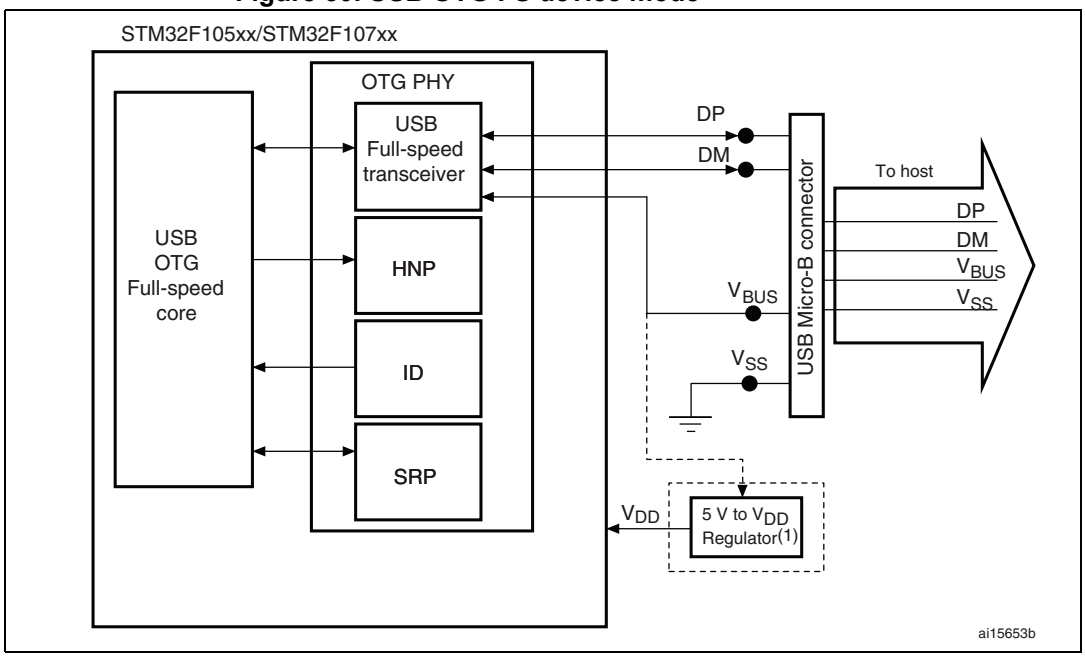
P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Appendix A Application block diagrams

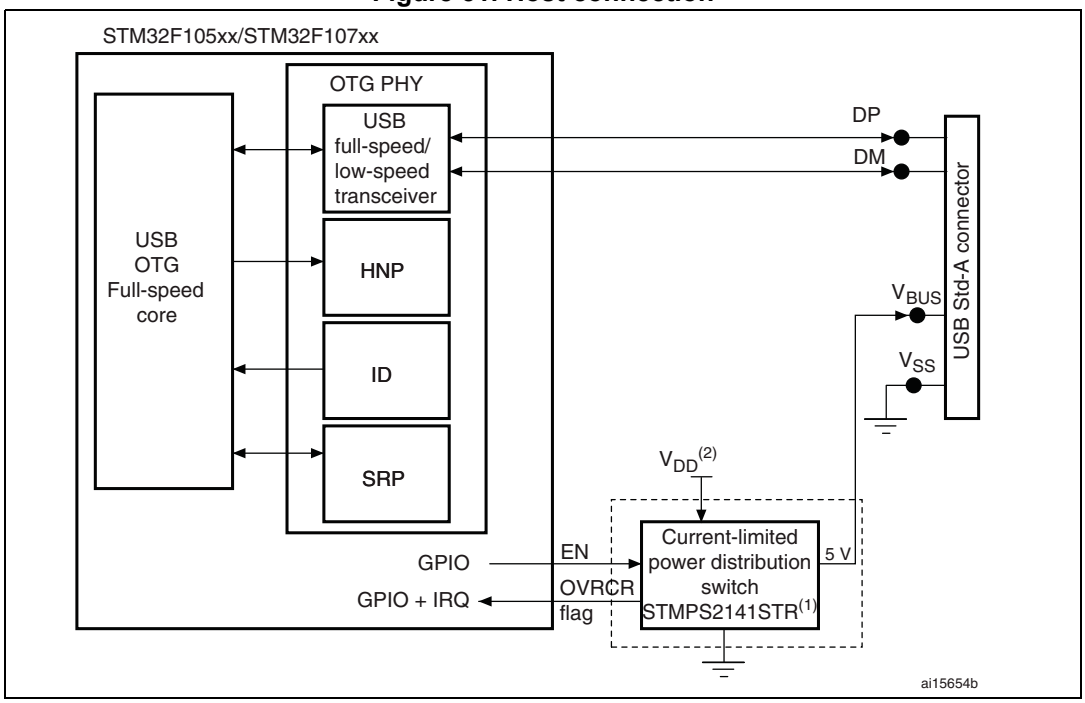
A.1 USB OTG FS interface solutions

Figure 50. USB OTG FS device mode



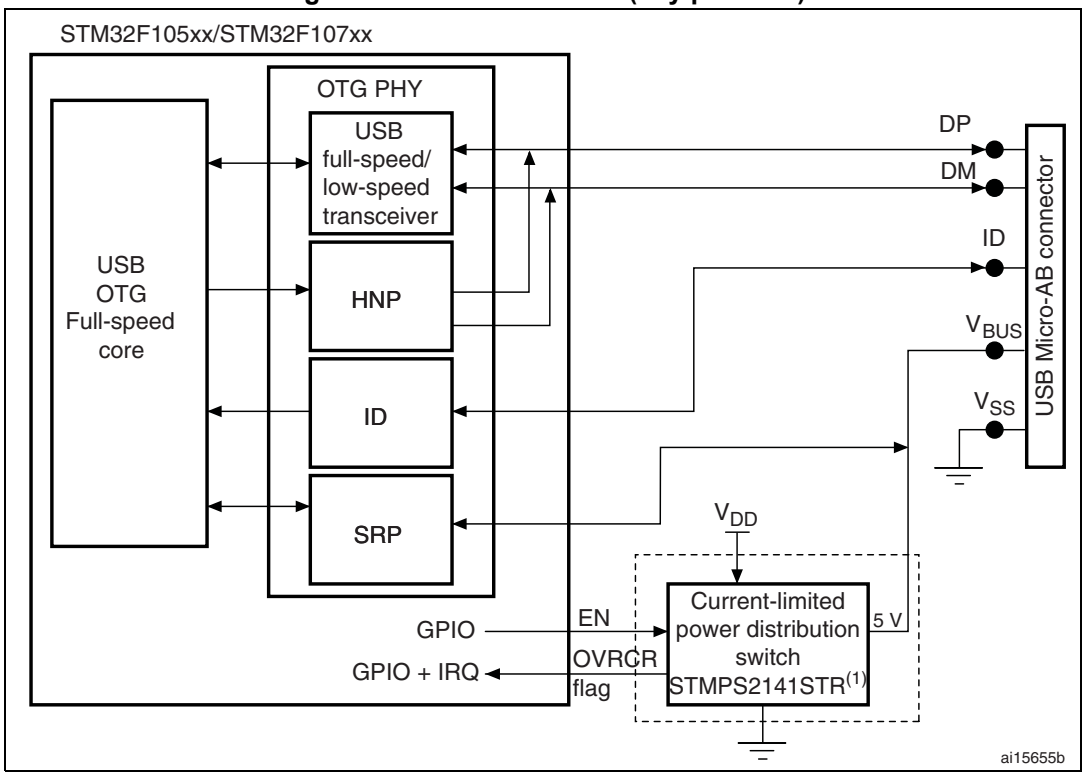
1. Use a regulator if you want to build a bus-powered device.

Figure 51. Host connection



1. STMPS2141STR needed only if the application has to support bus-powered devices.

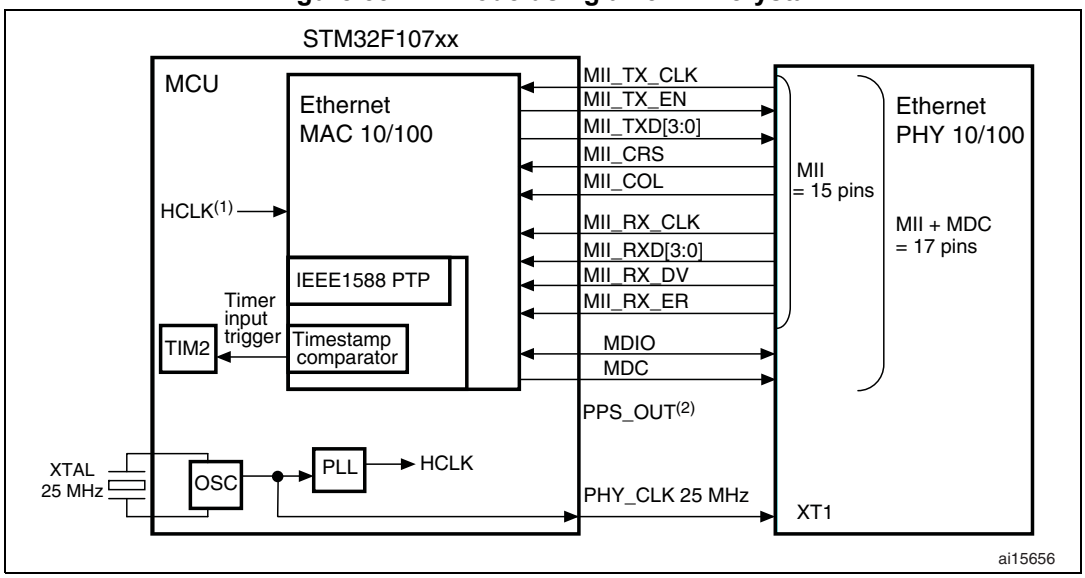
Figure 52. OTG connection (any protocol)



1. STMPS2141STR needed only if the application has to support bus-powered devices.

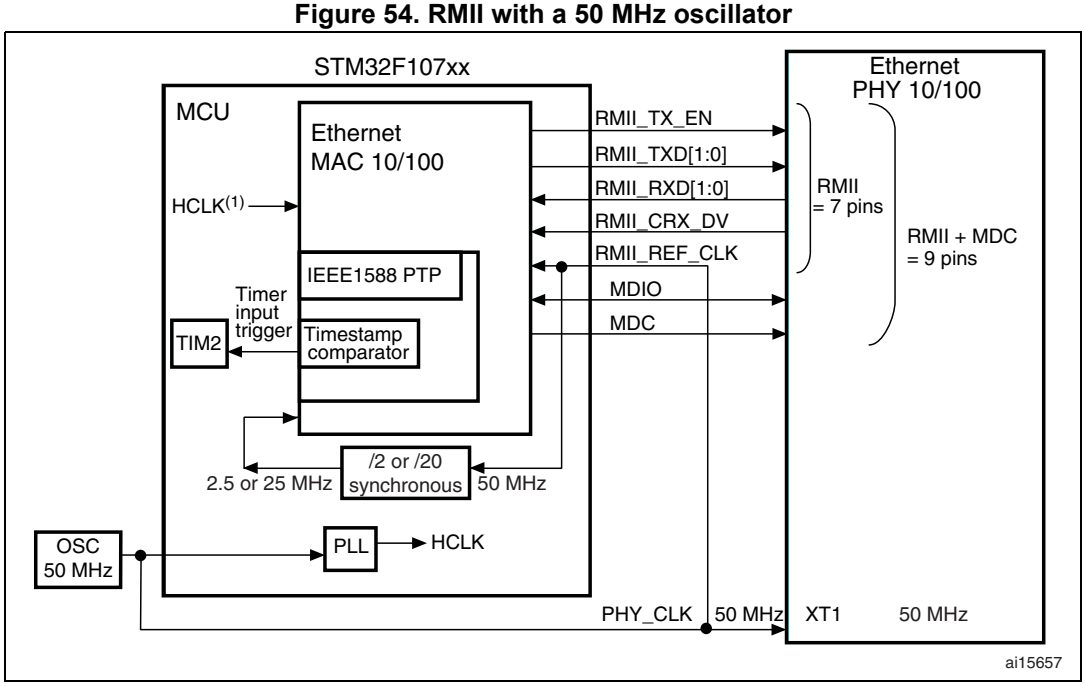
A.2 Ethernet interface solutions

Figure 53. MII mode using a 25 MHz crystal



1. HCLK must be greater than 25 MHz.
2. Pulse per second when using IEEE1588 PTP, optional signal.

Figure 54. RMII with a 50 MHz oscillator



1. HCLK must be greater than 25 MHz.

A.3 Complete audio player solutions

Two solutions are offered, illustrated in *Figure 57* and *Figure 58*.

Figure 57 shows storage media to audio DAC/amplifier streaming using a software Codec. This solution implements an audio crystal to provide audio class I^2S accuracy on the master clock (0.5% error maximum, see the Serial peripheral interface section in the reference manual for details).

Figure 57. Complete audio player solution 1

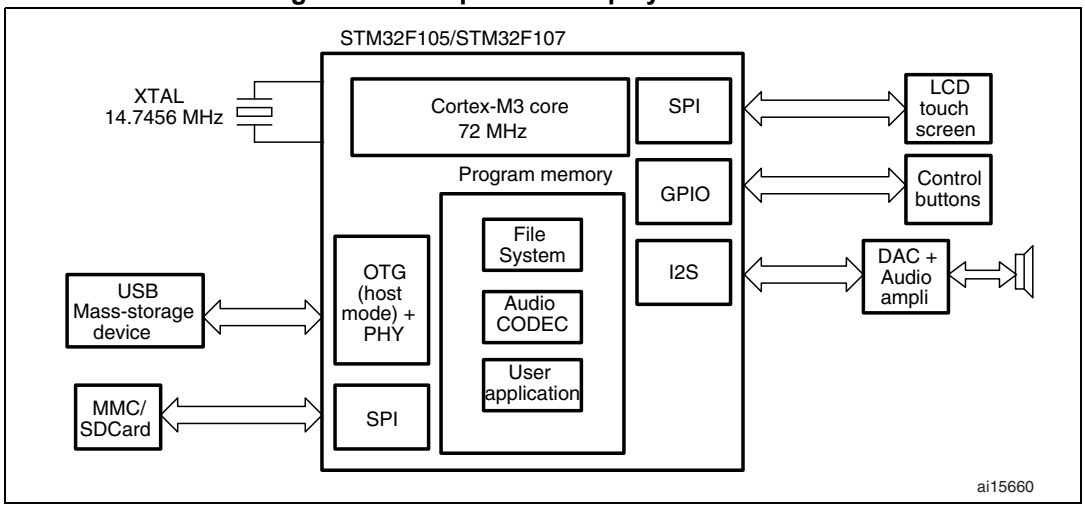


Figure 58 shows storage media to audio Codec/amplifier streaming with SOF synchronization of input/output audio streaming using a hardware Codec.

Figure 58. Complete audio player solution 2