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### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG |
| Peripherals | DMA, POR, PWM, Voltage Detect, WDT |
| Number of I/O | 51 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f107rbt6tr |

# List of figures

### 2.3.1 ARM Cortex-M3 core with embedded Flash and SRAM

The ARM Cortex-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.
With its embedded ARM core, STM32F105xx and STM32F107xx connectivity line family is compatible with all ARM tools and software.
*Figure 1* shows the general block diagram of the device family.

### 2.3.2 Embedded Flash memory

64 to 256 Kbytes of embedded Flash is available for storing programs and data.

### 2.3.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

### 2.3.4 Embedded SRAM

64 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

### 2.3.5 Nested vectored interrupt controller (NVIC)

The STM32F105xx and STM32F107xx connectivity line embeds a nested vectored interrupt controller able to handle up to 67 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

Any of the standard timers can be used to generate PWM outputs. Each of the timers has independent DMA request generations.

#### Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

#### Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

#### Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

#### SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

### 2.3.16 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

### 2.3.17 Universal synchronous/asynchronous receiver transmitters (USARTs)

The STM32F105xx and STM32F107xx connectivity line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability.

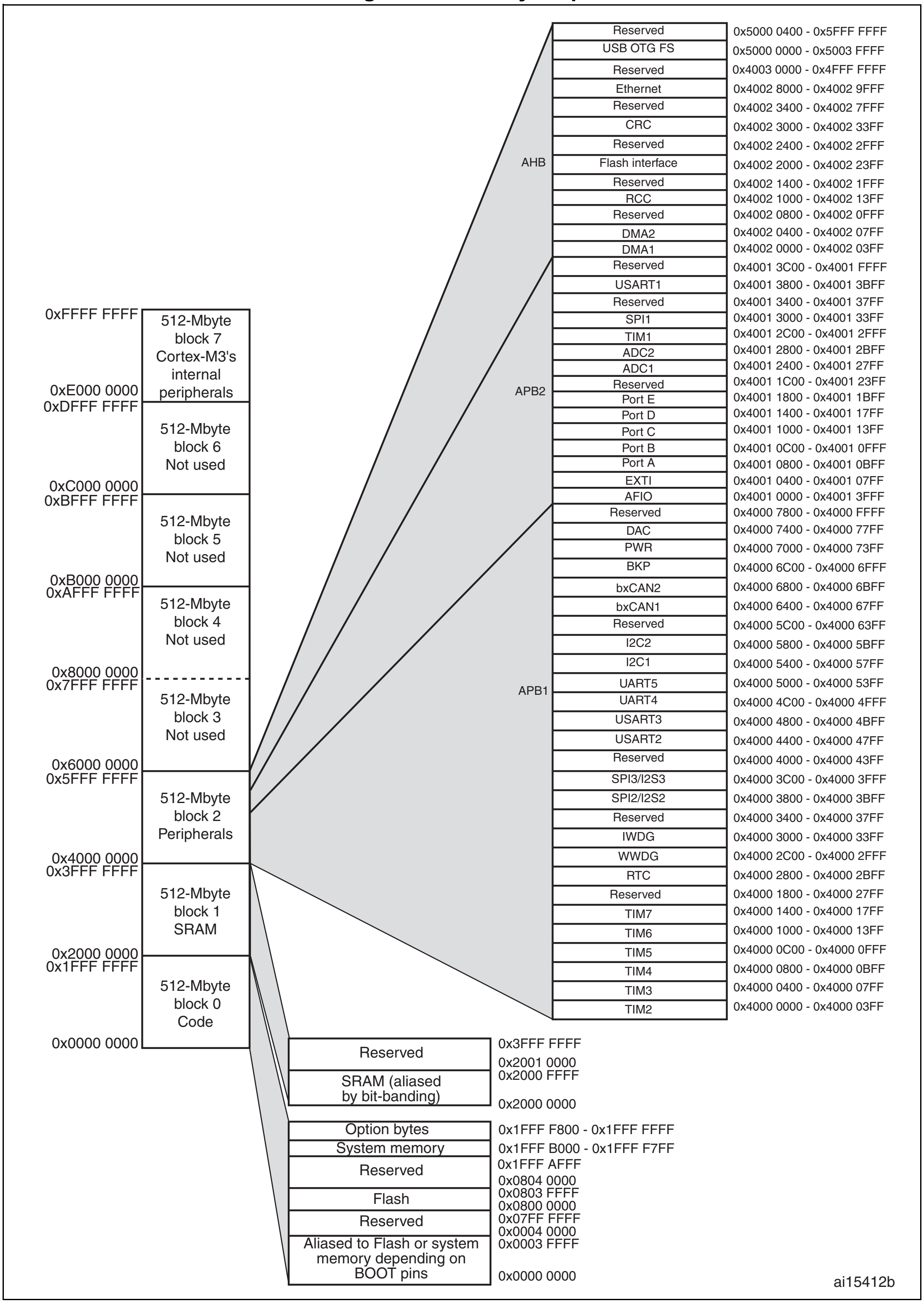
The USART1 interface is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s.

1. I = input, O = output, S = supply, HiZ = high impedance.
2. FT = 5 V tolerant. All I/Os are $V_{DD}$ capable.
3. Function availability depends on the chosen device.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch, and so their use in output mode is limited: they can be used only in output 2 MHz mode with a maximum load of 30 pF and only one pin can be put in output mode at a time.
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
7. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
8. SPI2/I2S2 and I2C2 are not available when the Ethernet is being used.
9. For the LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 and BGA100 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.

# 4 Memory mapping

The memory map is shown in *Figure 5*.

**Figure 5. Memory map**



## 5.3.4 Embedded reference voltage

The parameters given in *Table 12* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

**Table 12. Embedded internal reference voltage**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltage | –40 °C < $T_A$ < +105 °C | 1.16 | 1.20 | 1.26 | V |
| | | –40 °C < $T_A$ < +85 °C | 1.16 | 1.20 | 1.24 | V |
| $T_{S\_vrefint}$(1) | ADC sampling time when reading the internal reference voltage | - | - | 5.1 | 17.1(2) | µs |
| $V_{RERINT}$(2) | Internal reference voltage spread over the temperature range | $V_{DD}$ = 3 V ±10 mV | - | - | 10 | mV |
| $T_{Coeff}$(2) | Temperature coefficient | - | - | - | 100 | ppm/°C |

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

## 5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 9: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

### Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the $f_{HCLK}$ frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 13*, *Table 14* and *Table 15* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

**Table 18. Typical current consumption in Sleep mode, code running from Flash or RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ(1) All peripherals enabled(2) | Typ(1) All peripherals disabled | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current in Sleep mode | External clock(3) | 72 MHz | 28.2 | 6 | mA |
| | | | 48 MHz | 19 | 4.2 | |
| | | | 36 MHz | 14.7 | 3.4 | |
| | | | 24 MHz | 10.1 | 2.5 | |
| | | | 16 MHz | 6.7 | 2 | |
| | | | 8 MHz | 3.2 | 1.3 | |
| | | | 4 MHz | 2.3 | 1.2 | |
| | | | 2 MHz | 1.7 | 1.16 | |
| | | | 1 MHz | 1.5 | 1.1 | |
| | | | 500 kHz | 1.3 | 1.05 | |
| | | | 125 kHz | 1.2 | 1.05 | |
| | | Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency | 36 MHz | 13.7 | 2.6 | |
| | | | 24 MHz | 9.3 | 1.8 | |
| | | | 16 MHz | 6.3 | 1.3 | |
| | | | 8 MHz | 2.7 | 0.6 | |
| | | | 4 MHz | 1.6 | 0.5 | |
| | | | 2 MHz | 1 | 0.46 | |
| | | | 1 MHz | 0.8 | 0.44 | |
| | | | 500 kHz | 0.6 | 0.43 | |
| | | | 125 kHz | 0.5 | 0.42 | |

1. Typical values are measures at $T_A$ = 25 °C, $V_{DD}$ = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when $f_{HCLK}$ > 8 MHz.

### On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 19*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with one peripheral clocked on (with only the clock applied)
- ambient operating temperature and $V_{DD}$ supply voltage conditions summarized in *Table 6*

### 5.3.7 Internal clock source characteristics

The parameters given in Table 24 are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in Table 9.

#### High-speed internal (HSI) RC oscillator

**Table 24. HSI oscillator characteristics [(1)]**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | - | | - | 8 | | MHz |
| $DuCy_{(HSI)}$ | Duty cycle | - | | 45 | - | 55 | % |
| $ACC_{HSI}$ | Accuracy of the HSI oscillator | User-trimmed with the RCC_CR register[(2)] | | - | - | 1[(3)] | % |
| | | Factory-calibrated[(4)] | $T_A$ = –40 to 105 °C | –2 | - | 2.5 | % |
| | | | $T_A$ = –10 to 85 °C | –1.5 | - | 2.2 | % |
| | | | $T_A$ = 0 to 70 °C | –1.3 | - | 2 | % |
| | | | $T_A$ = 25 °C | –1.1 | - | 1.8 | % |
| $t_{su(HSI)}$[(4)] | HSI oscillator startup time | - | | 1 | - | 2 | µs |
| $I_{DD(HSI)}$[(4)] | HSI oscillator power consumption | - | | - | 80 | 100 | µA |

1. $V_{DD}$ = 3.3 V, $T_A$ = –40 to 105 °C unless otherwise specified.
2. Refer to application note AN2868 “STM32F10xxx internal RC oscillator (HSI) calibration” available from the ST website www.st.com.
3. Guaranteed by design, not tested in production.
4. Based on characterization, not tested in production.

#### Low-speed internal (LSI) RC oscillator

**Table 25. LSI oscillator characteristics [(1)]**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{LSI}$[(2)] | Frequency | 30 | 40 | 60 | kHz |
| $t_{su(LSI)}$[(3)] | LSI oscillator startup time | - | - | 85 | µs |
| $I_{DD(LSI)}$[(3)] | LSI oscillator power consumption | - | 0.65 | 1.2 | µA |

1. $V_{DD}$ = 3 V, $T_A$ = –40 to 105 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

#### Wakeup time from low-power mode

The wakeup times given in Table 26 is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

A device reset allows normal operations to be resumed.

The test results are given in *Table 31*. They are based on the EMS levels and classes defined in application note AN1709.

**Table 31. EMS characteristics**

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP100, $T_A$ = +25 °C, $f_{HCLK}$ = 72 MHz, conforms to IEC 61000-4-2 | 2B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, LQFP100, $T_A$ = +25 °C, $f_{HCLK}$ = 72 MHz, conforms to IEC 61000-4-4 | 4A |

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

#### Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

#### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC61967-2 standard which specifies the test board and the pin loading.

**Table 36. I/O static characteristics (continued)**

| Symbol | Parameter | | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{lkg}$ | Input leakage current [4] | | $V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os | - | - | ±1 | µA |
| | | | $V_{IN}$= 5 V, I/O FT | - | - | 3 | |
| $R_{PU}$ | Weak pull-up equivalent resistor[5] | All pins except for PA10 | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | kΩ |
| | | PA10 | | 8 | 11 | 15 | |
| $R_{PD}$ | Weak pull-down equivalent resistor[5] | All pins except for PA10 | $V_{IN} = V_{DD}$ | 30 | 40 | 50 | kΩ |
| | | PA10 | | 8 | 11 | 15 | |
| $C_{IO}$ | I/O pin capacitance | | - | - | 5 | - | pF |

1. FT = Five-volt tolerant. In order to sustain a voltage higher than $V_{DD}$+0.3 the internal pull-up/pull-down resistors must be disabled.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
3. With a minimum of 100 mV.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 18* and *Figure 19* for standard I/Os, and in *Figure 20* and *Figure 21* for 5 V tolerant I/Os.

**Figure 18. Standard I/O input characteristics - CMOS port**

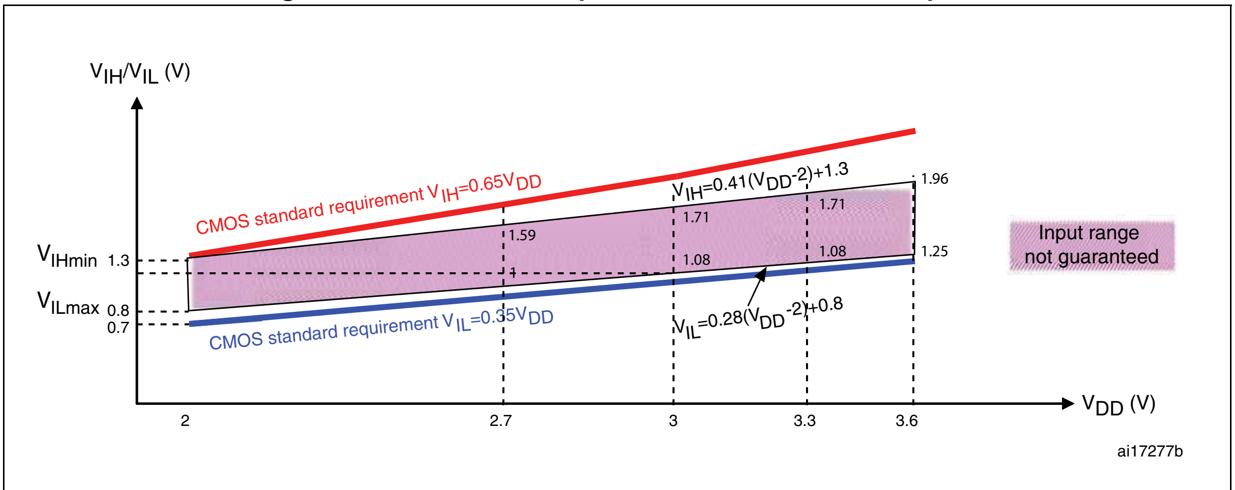


**Figure 19. Standard I/O input characteristics - TTL port**

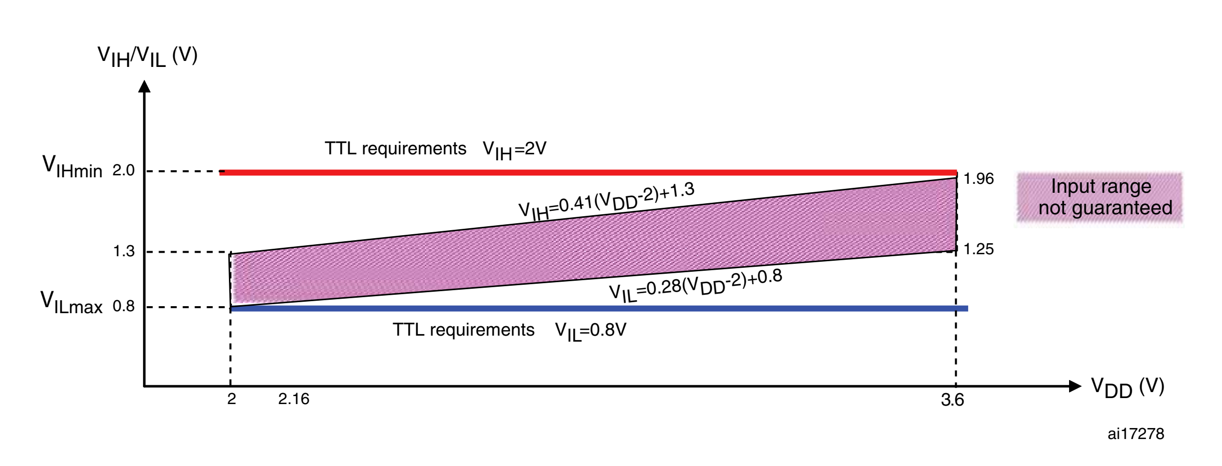



**Figure 20. 5 V tolerant I/O input characteristics - CMOS port**

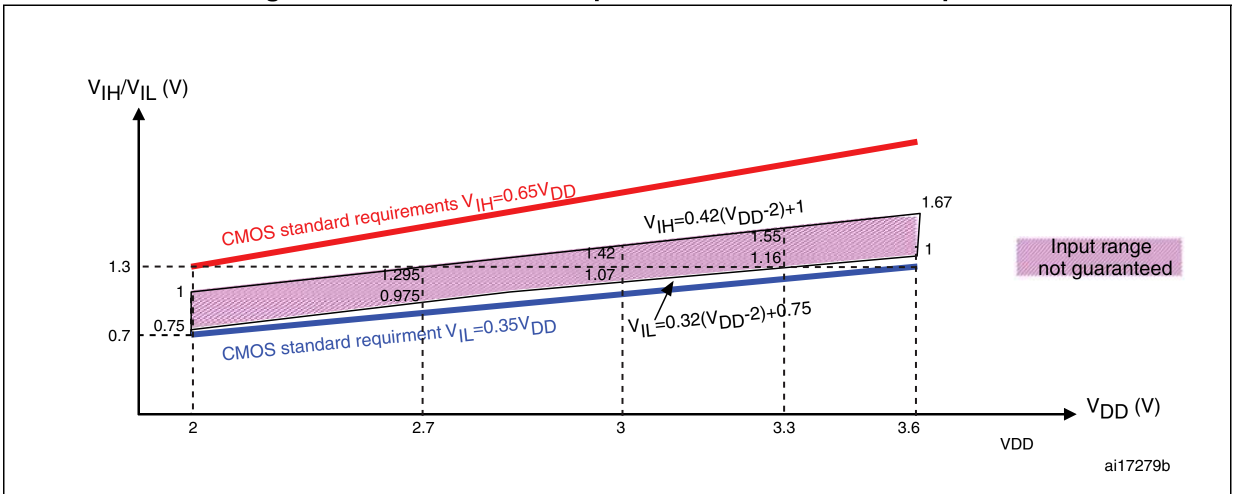
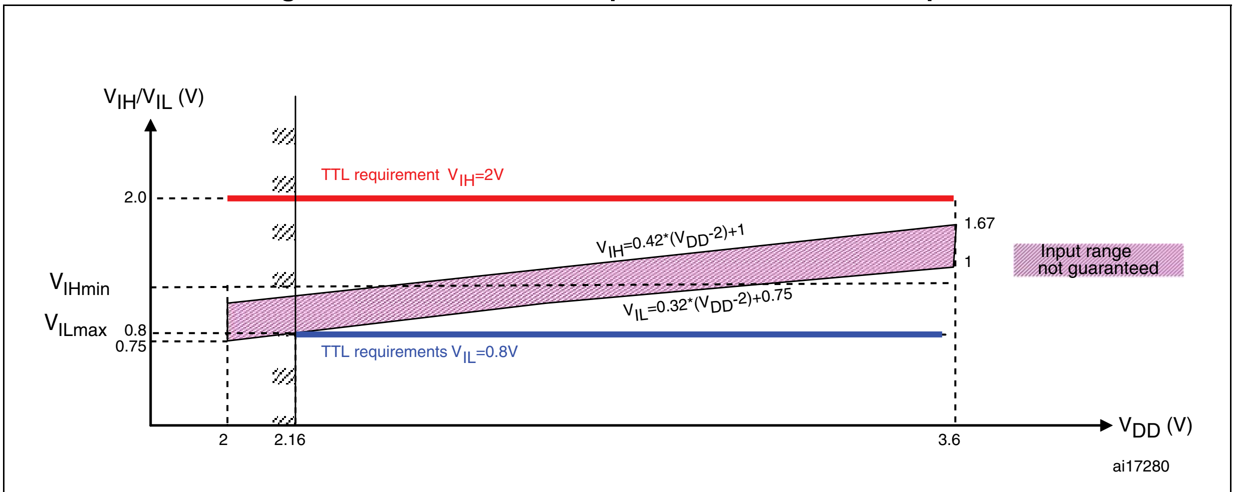



**Figure 21. 5 V tolerant I/O input characteristics - TTL port**



### $I^2S$ - SPI interface characteristics

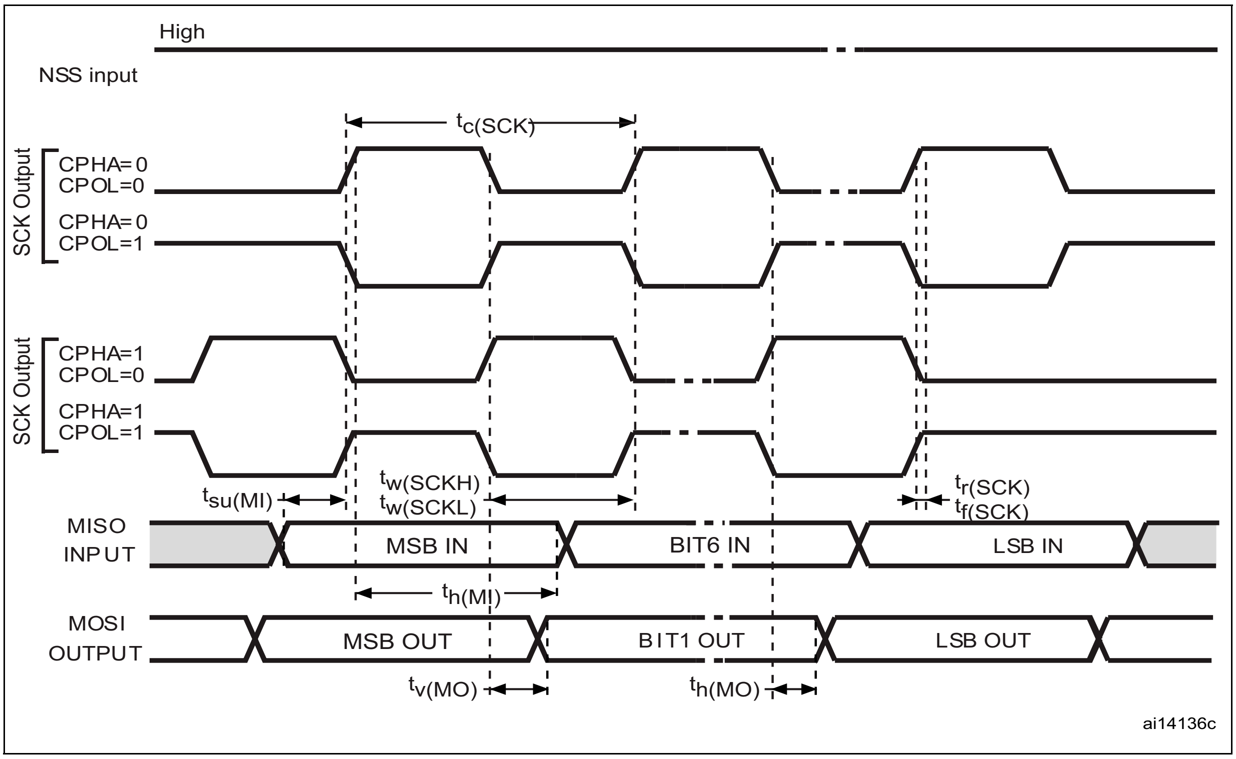
Unless otherwise specified, the parameters given in *Table 43* for SPI or in *Table 44* for $I^2S$ are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

Refer to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for $I^2S$).

**Table 43. SPI characteristics**

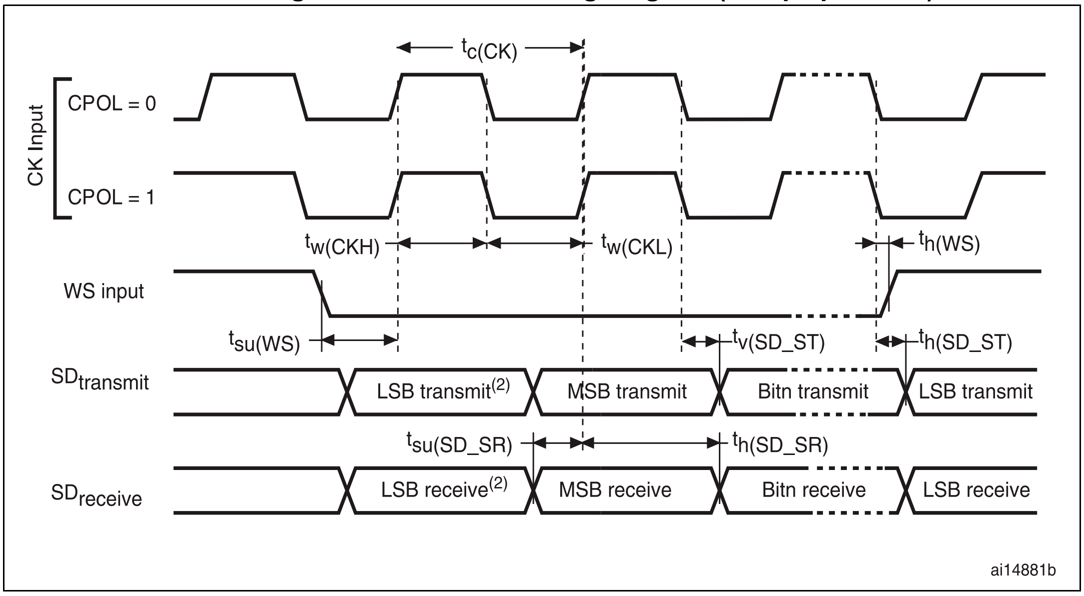
| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$ $1/t_{c(SCK)}$ | SPI clock frequency | Master mode | - | 18 | MHz |
| | | Slave mode | - | 18 | |
| $t_{r(SCK)}$ $t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load: C = 30 pF | - | 8 | ns |
| DuCy(SCK) | SPI slave input clock duty cycle | Slave mode | 30 | 70 | % |
| $t_{su(NSS)}$ | NSS setup time | Slave mode | 4 $t_{PCLK}$ | - | ns |
| $t_{h(NSS)}$ | NSS hold time | Slave mode | 2 $t_{PCLK}$ | - | |
| $t_{w(SCKH)}$ $t_{w(SCKL)}$ | SCK high and low time | Master mode, $f_{PCLK}$ = 36 MHz, presc = 4 | 50 | 60 | |
| $t_{su(MI)}$ | Data input setup time | Master mode | 4 | - | |
| $t_{su(SI)}$ | | Slave mode | 5 | - | |
| $t_{h(MI)}$ | Data input hold time | Master mode | 5 | - | |
| $t_{h(SI)}$ | | Slave mode | 5 | - | |
| $t_{a(SO)}$ | Data output access time | Slave mode, $f_{PCLK}$ = 20 MHz | - | 3*$t_{PCLK}$ | |
| $t_{v(SO)}$ | Data output valid time | Slave mode (after enable edge) | - | 34 | |
| $t_{v(MO)}$ | Data output valid time | Master mode (after enable edge) | - | 8 | |
| $t_{h(SO)}$ | Data output hold time | Slave mode (after enable edge) | 32 | - | |
| $t_{h(MO)}$ | | Master mode (after enable edge) | 10 | - | |

**Figure 27. SPI timing diagram - master mode(1)**



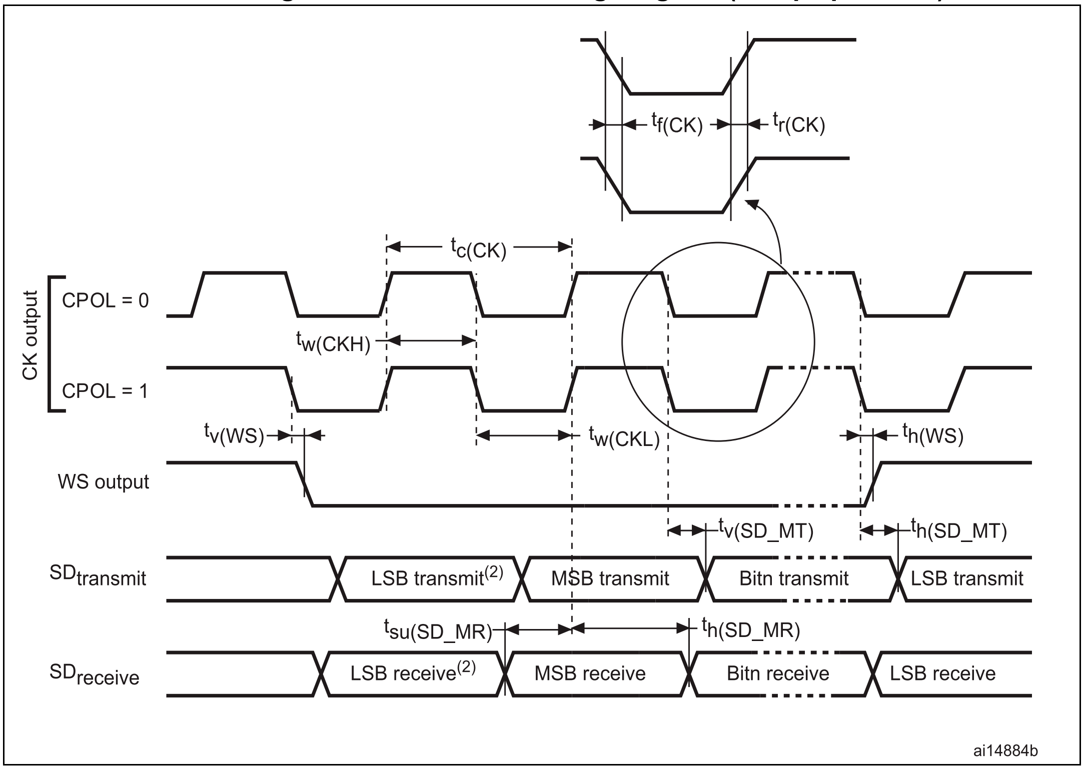

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Figure 28. I²S slave timing diagram (Philips protocol)(1)**




1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

**Figure 29. I²S master timing diagram (Philips protocol)(1)**




1. Based on characterization, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

**Table 52. ADC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{lat}$(2) | Injection trigger conversion latency | $f_{ADC}$ = 14 MHz | - | - | 0.214 | µs |
| | | - | - | - | 3(4) | $1/f_{ADC}$ |
| $t_{latr}$(2) | Regular trigger conversion latency | $f_{ADC}$ = 14 MHz | - | - | 0.143 | µs |
| | | - | - | - | 2(4) | $1/f_{ADC}$ |
| $t_S$(2) | Sampling time | $f_{ADC}$ = 14 MHz | 0.107 | - | 17.1 | µs |
| | | - | 1.5 | - | 239.5 | $1/f_{ADC}$ |
| $t_{STAB}$(2) | Power-up time | - | 0 | 0 | 1 | µs |
| $t_{CONV}$(2) | Total conversion time (including sampling time) | $f_{ADC}$ = 14 MHz | 1 | - | 18 | µs |
| | | - | 14 to 252 ($t_S$ for sampling +12.5 for successive approximation) | | | $1/f_{ADC}$ |

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. $V_{REF+}$ is internally connected to $V_{DDA}$ and $V_{REF-}$ is internally connected to $V_{SSA}$.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 52*.

**Equation 1: $R_{AIN}$ max formula**

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

**Table 53. $R_{AIN}$ max for $f_{ADC}$ = 14 MHz(1)**

| $T_s$ (cycles) | $t_S$ (µs) | $R_{AIN}$ max (kΩ) |
|---|---|---|
| 1.5 | 0.11 | 0.4 |
| 7.5 | 0.54 | 5.9 |
| 13.5 | 0.96 | 11.4 |
| 28.5 | 2.04 | 25.2 |
| 41.5 | 2.96 | 37.2 |
| 55.5 | 3.96 | 50 |
| 71.5 | 5.11 | NA |
| 239.5 | 17.1 | NA |

1. Based on characterization, not tested in production.

**Table 59. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| E3 | - | 12.000 | - | - | 0.4724 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0.0° | 3.5° | 7.0° | 0.0° | 3.5° | 7.0° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 44. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint**

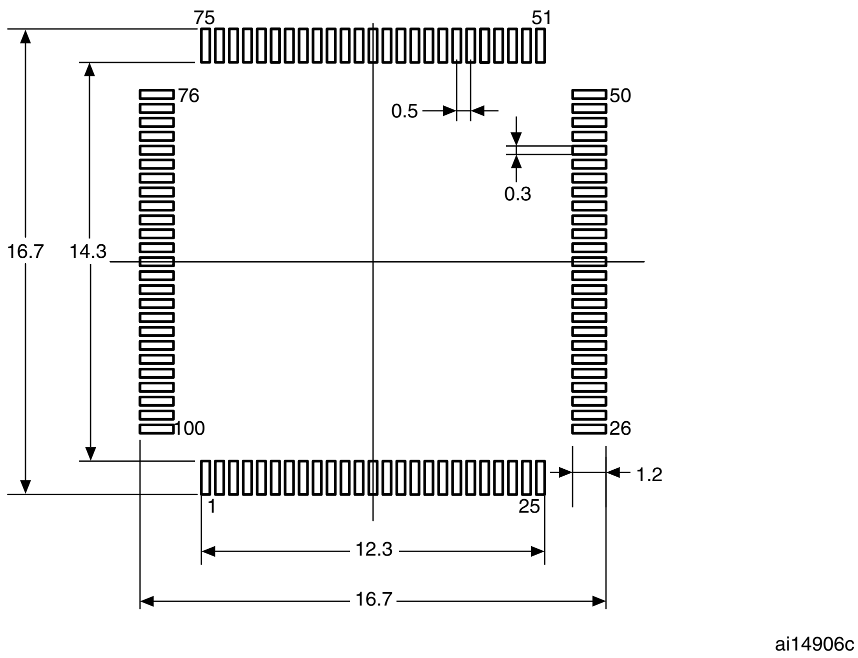
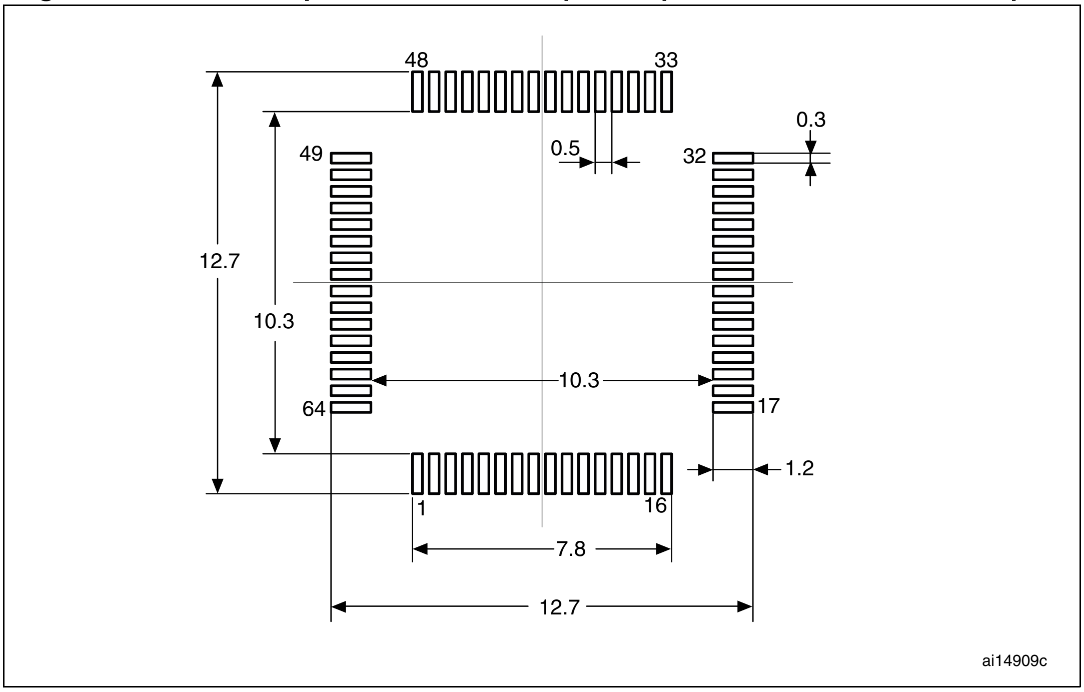


**Table 60.LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| e | - | 0.500 | - | - | 0.0197 | - |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 47.LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint**




1. Dimensions are in millimeters.

## 6.4 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 9: General operating conditions on page 37*.

The maximum chip-junction temperature, $T_J$ max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A$ max is the maximum ambient temperature in $^\circ$C,
- $\Theta_{JA}$ is the package junction-to-ambient thermal resistance, in $^\circ$C/W,
- $P_D$ max is the sum of $P_{INT}$ max and $P_{I/O}$ max ($P_D$ max = $P_{INT}$ max + $P_{I/O}$max),
- $P_{INT}$ max is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = $\Sigma$ ($V_{OL}$ × $I_{OL}$) + $\Sigma$(($V_{DD}$ – $V_{OH}$) × $I_{OH}$),

taking into account the actual $V_{OL}$ / $I_{OL}$ and $V_{OH}$ / $I_{OH}$ of the I/Os at low and high level in the application.

**Table 61. Package thermal characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | **Thermal resistance junction-ambient** LQFP100 - 14 × 14 mm / 0.5 mm pitch | 46 | °C/W |
| | **Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch | 45 | |
| $\Theta_{JA}$ | **Thermal resistance junction-ambient** LFBGA100 - 10 × 10 mm / 0.8 mm pitch | 40 | °C/W |
| | **Thermal resistance junction-ambient** LQFP100 - 14 × 14 mm / 0.5 mm pitch | 46 | |
| | **Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch | 45 | |

### 6.4.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

Table 65. Document revision history (continued)

| Date | Revision | Changes |
|---|---|---|
| 19-Jun-2009 | 3 | Section 2.3.8: Boot modes and Section 2.3.20: Ethernet MAC interface with dedicated DMA and IEEE 1588 support updated.<br>Section 2.3.24: Remap capability added.<br>Figure 1: STM32F105xx and STM32F107xx connectivity line block diagram and Figure 5: Memory map updated.<br>In Table 5: Pin definitions:<br>– I2S3_WS, I2S3_CK and I2S3_SD default alternate functions added<br>– small changes in signal names<br>– Note 6 modified<br>– ETH_MII_PPS_OUT and ETH_RMII_PPS_OUT replaced by ETH_PPS_OUT<br>– ETH_MII_MDIO and ETH_RMII_MDIO replaced by ETH_MDIO<br>– ETH_MII_MDC and ETH_RMII_MDC replaced by ETH_MDC<br>Figures: Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled and Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled removed.<br>Table 13: Maximum current consumption in Run mode, code with data processing running from Flash, Table 14: Maximum current consumption in Run mode, code with data processing running from RAM and Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM are to be determined.<br>Figure 12 and Figure 13 show typical curves. PLL1 renamed to PLL.<br>$I_{DD}$ supply current in Stop mode modified in Table 16: Typical and maximum current consumptions in Stop and Standby modes.<br>Figure 11: Typical current consumption in Stop mode with regulator in Run mode versus temperature at different VDD values, Figure 13: Typical current consumption in Standby mode versus temperature at different VDD values and Figure 13: Typical current consumption in Standby mode versus temperature at different VDD values updated.<br>Table 17: Typical current consumption in Run mode, code with data processing running from Flash, Table 18: Typical current consumption in Sleep mode, code running from Flash or RAM and Table 19: Peripheral current consumption updated.<br>$f_{HSE\_ext}$ modified in Table 20: High-speed external user clock characteristics.<br>Min PLL input clock ($f_{PLL\_IN}$), $f_{PLL\_OUT}$ min and $f_{PLL\_VCO}$ min modified in Table 27: PLL characteristics.<br>$ACC_{HSI}$ max values modified in Table 24: HSI oscillator characteristics. Table 31: EMS characteristics and Table 32: EMI characteristics updated. Table 43: SPI characteristics updated.<br>Modified: Figure 28: I2S slave timing diagram (Philips protocol)(1), Figure 29: I2S master timing diagram (Philips protocol)(1) and Figure 31: Ethernet SMI timing diagram.<br>BGA100 package removed.<br>Section 6.4: Thermal characteristics added. Small text changes. |