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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	51
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f107rct6tr

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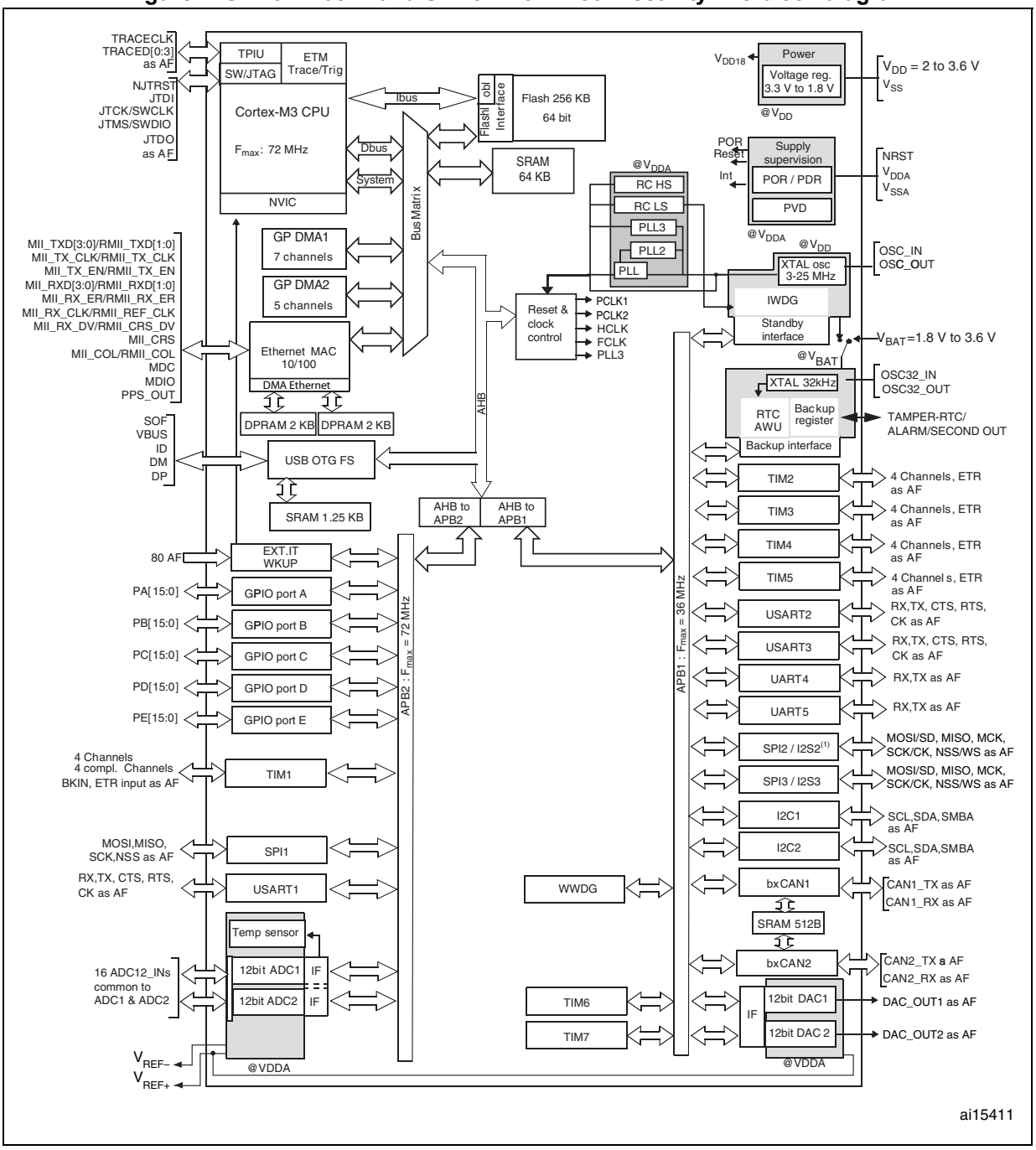
2.3 Overview

Figure 1. STM32F105xx and STM32F107xx connectivity line block diagram



1. T_A = –40 °C to +85 °C (suffix 6, see *Table 62*) or –40 °C to +105 °C (suffix 7, see *Table 62*), junction temperature up to 105 °C or 125 °C, respectively.
2. AF = alternate function on I/O port pin.

2.3.9 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supplies for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

2.3.10 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.3.11 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop modes.
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode.

2.3.12 Low-power modes

The STM32F105xx and STM32F107xx connectivity line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

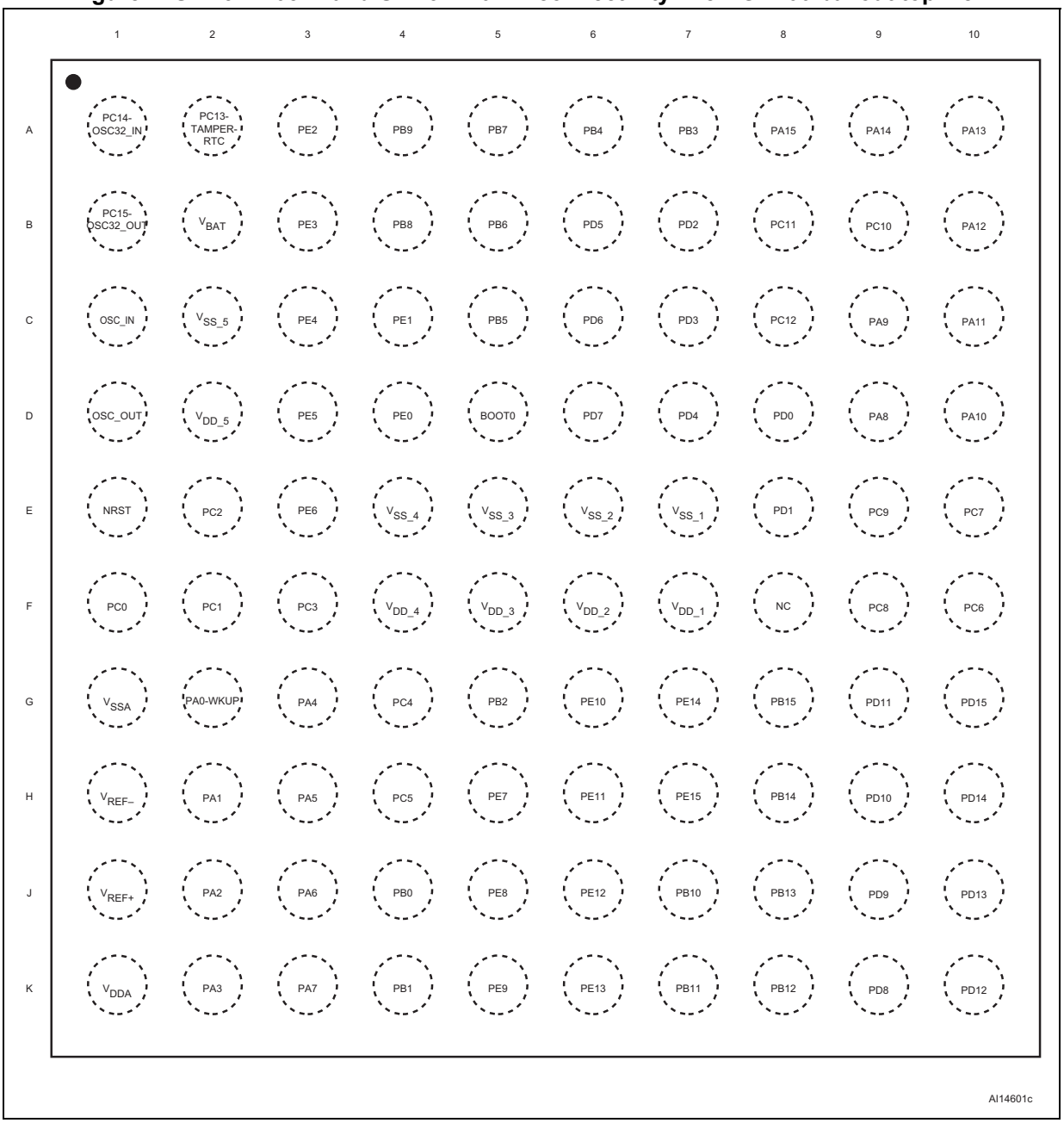
  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.
  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm or the USB OTG FS wakeup.

3 Pinouts and pin description

Figure 2. STM32F105xx and STM32F107xx connectivity line BGA100 ballout top view



1. I = input, O = output, S = supply, HiZ = high impedance.
2. FT = 5 V tolerant. All I/Os are V_{DD} capable.
3. Function availability depends on the chosen device.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch, and so their use in output mode is limited: they can be used only in output 2 MHz mode with a maximum load of 30 pF and only one pin can be put in output mode at a time.
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
7. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: *www.st.com*.
8. SPI2/I2S2 and I2C2 are not available when the Ethernet is being used.
9. For the LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 and BGA100 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.

Table 13. Maximum current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled	72 MHz	68	68.4	mA
			48 MHz	49	49.2	
			36 MHz	38.7	38.9	
			24 MHz	27.3	27.9	
			16 MHz	20.2	20.5	
			8 MHz	10.2	10.8	
		External clock(2), all peripherals disabled	72 MHz	32.7	32.9	
			48 MHz	25	25.2	
			36 MHz	20.3	20.6	
			24 MHz	14.8	15.1	
			16 MHz	11.2	11.7	
			8 MHz	6.6	7.2	

1. Based on characterization, not tested in production.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 14. Maximum current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled	72 MHz	65.5	66	mA
			48 MHz	45.4	46	
			36 MHz	35.5	36.1	
			24 MHz	25.2	25.6	
			16 MHz	18	18.5	
			8 MHz	10.5	11	
		External clock(2), all peripherals disabled	72 MHz	31.4	31.9	
			48 MHz	27.8	28.2	
			36 MHz	17.6	18.3	
			24 MHz	13.1	13.8	
			16 MHz	10.2	10.9	
			8 MHz	6.1	7.8	

1. Based on characterization, tested in production at V_{DD} max, f_{HCLK} max..
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 19. Peripheral current consumption (continued)

Peripheral		Typical consumption at 25 °C	Unit
APB2 (up to 72 MHz)	APB2-Bridge	3.47	µA/MHz
	GPIOA	6.39	
	GPIOB	6.39	
	GPIOC	6.11	
	GPIOD	6.39	
	GPIOE	6.11	
	SPI1	3.61	
	USART1	12.08	
	TIM1	23.47	
	ADC1(4)	18.21	

1. The BusMatrix is automatically active when at least one master is ON.(CPU, ETH-MAC, DMA1 or DMA2).
2. When I2S is enabled we have a consumption add equal to 0, 02 mA.
3. When DAC_OUT1 or DAC_OUT2 is enabled we have a consumption add equal to 0, 3 mA.
4. Specific conditions for measuring ADC current consumption: f_{HCLK} = 56 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/4$. When ADON bit in the ADC_CR2 register is set to 1, a current consumption of analog part equal to 0.6 mA must be added.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 20* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 9*.

Table 20. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External user clock source frequency(1)	-	1	8	50	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

5.3.7 Internal clock source characteristics

The parameters given in *Table 24* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

High-speed internal (HSI) RC oscillator

Table 24. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	8		MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register(2)		-	-	1(3)	%
		Factory-calibrated(4)	T_A = –40 to 105 °C	–2	-	2.5	%
			T_A = –10 to 85 °C	–1.5	-	2.2	%
			T_A = 0 to 70 °C	–1.3	-	2	%
			T_A = 25 °C	–1.1	-	1.8	%
$t_{su(HSI)}$(4)	HSI oscillator startup time	-		1	-	2	µs
$I_{DD(HSI)}$(4)	HSI oscillator power consumption	-		-	80	100	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Refer to application note AN2868 “STM32F10xxx internal RC oscillator (HSI) calibration” available from the ST website *www.st.com*.
3. Guaranteed by design, not tested in production.
4. Based on characterization, not tested in production.

Low-speed internal (LSI) RC oscillator

Table 25. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	30	40	60	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.65	1.2	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in *Table 26* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

A device reset allows normal operations to be resumed.

The test results are given in *Table 31*. They are based on the EMS levels and classes defined in application note AN1709.

Table 31. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 72 MHz, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 72 MHz, conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC61967-2 standard which specifies the test board and the pin loading.

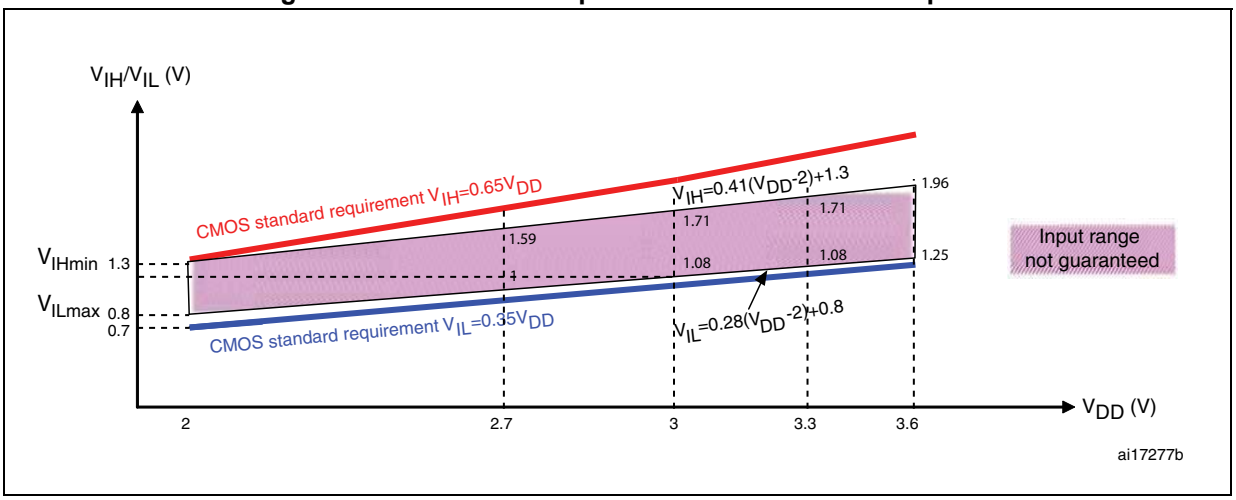
Table 36. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
I_{lkg}	Input leakage current (4)		$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os	-	-	±1	µA
			V_{IN}= 5 V, I/O FT	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(5)	All pins except for PA10	$V_{IN} = V_{SS}$	30	40	50	kΩ
		PA10		8	11	15	
R_{PD}	Weak pull-down equivalent resistor(5)	All pins except for PA10	$V_{IN} = V_{DD}$	30	40	50	kΩ
		PA10		8	11	15	
C_{IO}	I/O pin capacitance		-	-	5	-	pF

1. FT = Five-volt tolerant. In order to sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
3. With a minimum of 100 mV.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 18* and *Figure 19* for standard I/Os, and in *Figure 20* and *Figure 21* for 5 V tolerant I/Os.

Figure 18. Standard I/O input characteristics - CMOS port



5.3.16 Communications interfaces

I^2C interface characteristics

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

The STM32F105xx and STM32F107xx I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I^2C characteristics are described in *Table 41*. Refer also to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 41. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(3)	-	0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20 + 0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I^2C frequencies. It must be at least 4 MHz to achieve the fast mode I^2C frequencies and it must be a mulitple of 10 MHz in order to reach I^2C fast mode maximum clock 400 kHz.
3. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Table 47. USB OTG FS electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, refer to USB Specification - Chapter 7 (version 2.0).

Ethernet characteristics

Table 48 showns the Ethernet operating voltage.

Table 48. Ethernet DC electrical characteristics

Symbol		Parameter	Min.(1)	Max.(1)	Unit
Input level	V_{DD}	Ethernet operating voltage	3.0	3.6	V

1. All the voltages are measured from the local ground potential.

Table 49 gives the list of Ethernet MAC signals for the SMI (station management interface) and *Figure 31* shows the corresponding timing diagram.

Figure 31. Ethernet SMI timing diagram

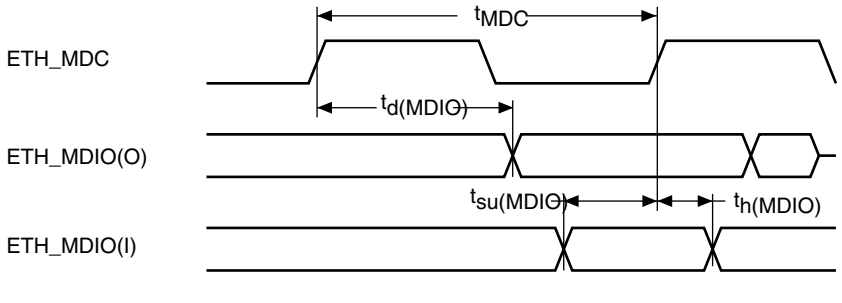


Table 49. Dynamic characteristics: Ethernet MAC signals for SMI

Symbol	Rating	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time (1.71 MHz, AHB = 72 MHz)	583	583.5	584	ns
$t_{d(MDIO)}$	MDIO write data valid time	13.5	14.5	15.5	ns
$t_{su(MDIO)}$	Read data setup time	35	-	-	ns
$t_{h(MDIO)}$	Read data hold time	0	-	-	ns

5.3.18 DAC electrical specifications

Table 56. DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage	2.4	-	3.6	V	-
V_{REF+}	Reference supply voltage	2.4	-	3.6	V	V_{REF+} must always be below V_{DDA}
V_{SSA}	Ground	0	-	0	V	-
R_{LOAD}(1)	Resistive load with buffer ON	5	-	-	kΩ	-
R_O(1)	Impedance output with buffer OFF	-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(1)	Capacitive load	-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer ON	0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{REF+} = 3.6 V and (0x155) to (0xEAB) at V_{REF+} = 2.4 V
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer ON	-	-	V_{DDA} – 0.2	V	
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer OFF	-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer OFF	-	-	V_{REF+} – 1LSB	V	
$I_{DDVREF+}$	DAC DC current consumption in quiescent mode (Standby mode)	-	-	220	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
I_{DDA}	DAC DC current consumption in quiescent mode (Standby mode)	-	-	380	µA	With no load, middle code (0x800) on the inputs
		-	-	480	µA	With no load, worst code (0xF1C) at V_{REF+} = 3.6 V in terms of DC consumption on the inputs
DNL(2)	Differential non linearity Difference between two consecutive code-1LSB)	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration.
		-	-	±2	LSB	Given for the DAC in 12-bit configuration.
INL(2)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±1	LSB	Given for the DAC in 10-bit configuration.
		-	-	±4	LSB	Given for the DAC in 12-bit configuration.

5.3.19 Temperature sensor characteristics

Table 57. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L (1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25} (1)	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START} (2)	Startup time	4	-	10	µs
T_{S_temp} (3)(2)	ADC sampling time when reading the temperature	-	-	17.1	µs

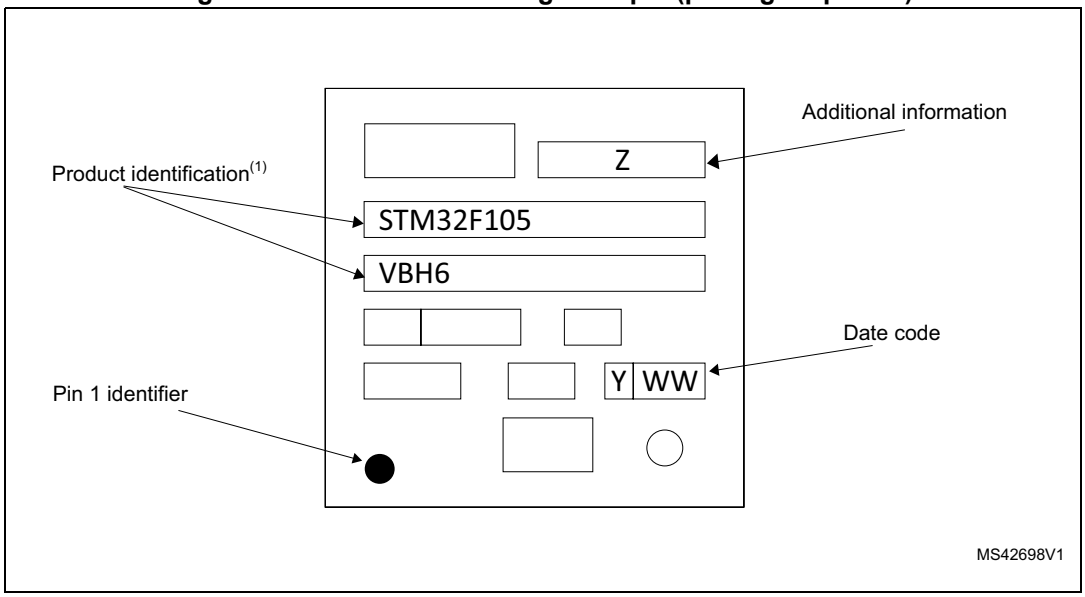
1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

Device marking for LFBGA100

The following figure shows the device marking for the LQFP100 package.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 42. LFBGA100 marking example (package top view)



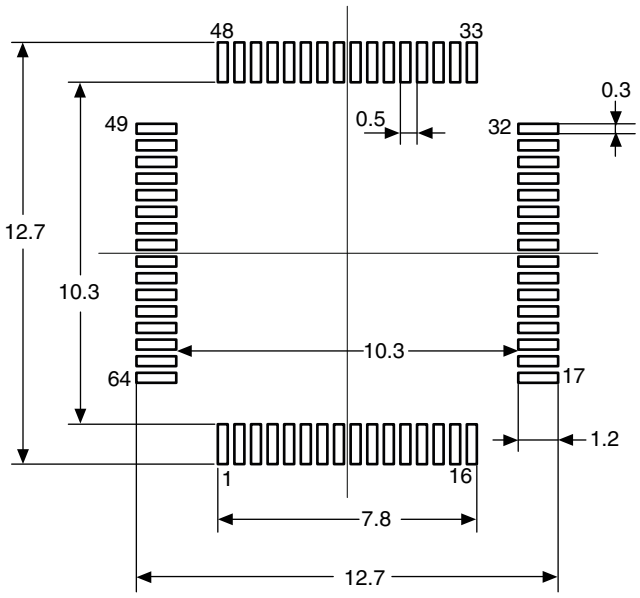
Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 60.LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 47.LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint

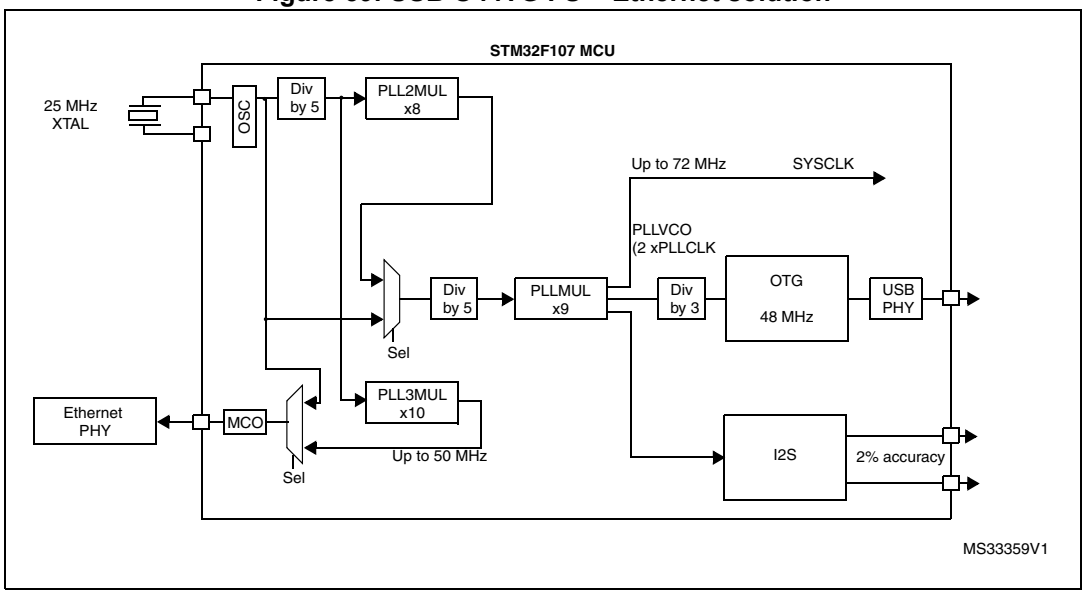


1. Dimensions are in millimeters.

A.4 USB OTG FS interface + Ethernet/I²S interface solutions

With the clock tree implemented on the STM32F107xx, only one crystal is required to work with both the USB (host/device/OTG) and the Ethernet (MII/RMII) interfaces. *Figure 59* illustrate the solution.

Figure 59. USB O44TG FS + Ethernet solution



With the clock tree implem1ented on the STM32F107xx, only one crystal is required to work with both the USB (host/device/OTG) and the I²S (Audio) interfaces. *Figure 60* illustrate the solution.

Figure 60. USB OTG FS + I²S (Audio) solution

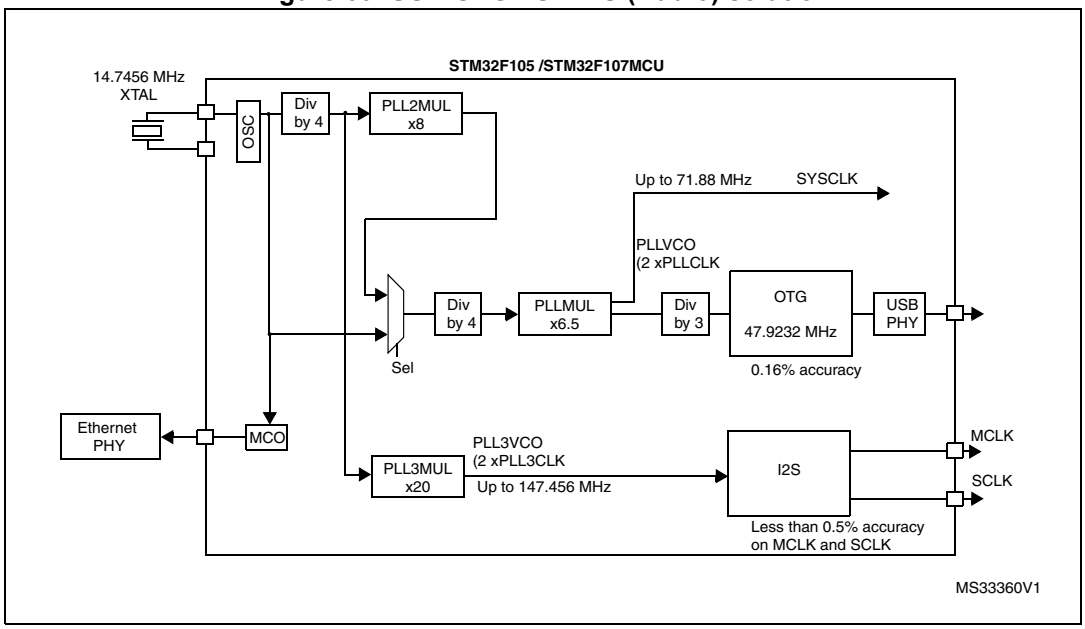


Table 63. PLL configurations

Application	Crystal value in MHz (XT1)	PREDIV2	PLL2MUL	PLLSRC	PREDIV1	PLLMUL	USB prescaler (PLLVCO output)	PLL3MUL	I2Sn clock input	MCO (main clock output)
Ethernet only	25	/5	PLL2ON x8	PLL2	/5	PLLON x9	NA	PLL3ON x10	NA	XT1 (MII) PLL3 (RMII)
Ethernet + OTG	25	/5	PLL2ON x8	PLL2	/5	PLLON x9	/3	PLL3ON x10	NA	XT1 (MII) PLL3 (RMII)
Ethernet + OTG + basic audio	25	/5	PLL2ON x8	PLL2	/5	PLLON x9	/3	PLL3ON x10	PLL	XT1 (MII) PLL3 (RMII)
Ethernet + OTG + Audio class I^2S(1)	14.7456	/4	PLL2ON x12	PLL2	/4	PLLON x6.5	/3	PLL3ON x20	PLL3 VCO Out	NA ETH PHY must use its own crystal
OTG only	8	NA	PLL2OFF	XT1	/1	PLLON x9	/3	PLL3OFF	NA	NA
OTG + basic audio	8	NA	PLL2OFF	XT1	/1	PLLON x9	/3	PLL3OFF	PLL	NA
OTG + Audio class I^2S(1)	14.7456	/4	PLL2ON x12	PLL2	/4	PLLON x6.5	/3	PLL3ON x20	PLL3 VCO Out	NA
Audio class I^2S only(1)	14.7456	/4	PLL2ON x12	PLL2	/4	PLLON x6.5	NA	PLL3ON x20	PLL3 VCO out	NA

1. SYSCLK is set to be at 72 MHz except in this case where SYSCLK is at 71.88 MHz.

Table 64 give the I_{DD} run mode values that correspond to the conditions specified in *Table 63*.