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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	80
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f107vbt6

1 Introduction

This datasheet provides the description of the STM32F105xx and STM32F107xx connectivity line microcontrollers. For more details on the whole STMicroelectronics STM32F10xxx family, refer to *Section 2.2: Full compatibility throughout the family*.

The STM32F105xx and STM32F107xx datasheet should be read in conjunction with the STM32F10xxx reference manual.
For information on programming, erasing and protection of the internal Flash memory refer to the STM32F10xxx Flash programming manual.
The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core refer to the Cortex®-M3 Technical Reference Manual, available from the www.arm.com website.

2 Description

The STM32F105xx and STM32F107xx connectivity line family incorporates the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 256 Kbytes and SRAM 64 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, four general-purpose 16-bit timers plus a PWM timer, as well as standard and advanced communication interfaces: up to two I^2Cs, three SPIs, two I2Ss, five USARTs, an USB OTG FS and two CANs. Ethernet is available on the STM32F107xx only.

The STM32F105xx and STM32F107xx connectivity line family operates in the –40 to +105 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F105xx and STM32F107xx connectivity line family offers devices in three different package types: from 64 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F105xx and STM32F107xx connectivity line microcontroller family suitable for a wide range of applications such as motor drives and application control, medical and handheld equipment, industrial applications, PLCs, inverters, printers, and scanners, alarm systems, video intercom, HVAC and home audio equipment.

2.1 Device overview

Figure 1 shows the general block diagram of the device family.

Table 2. STM32F105xx and STM32F107xx features and peripheral counts

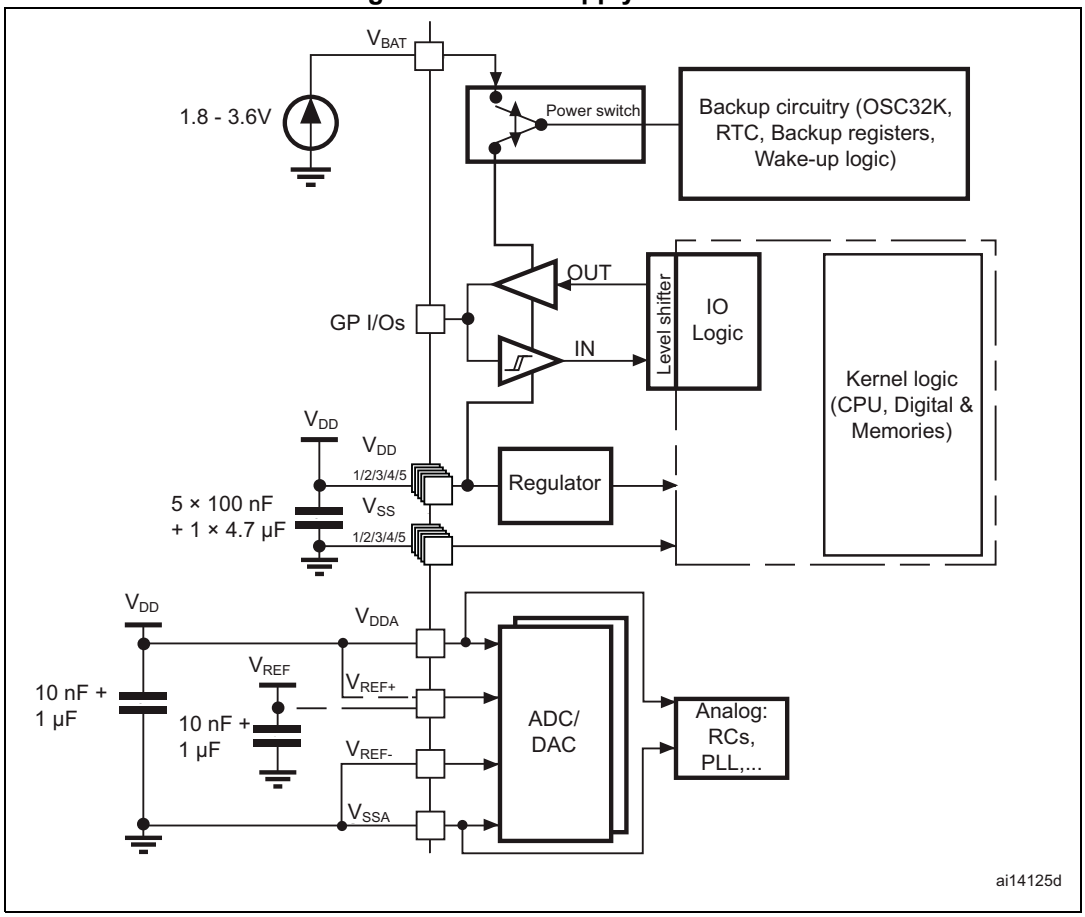
Peripherals(1)		STM32F105Rx			STM32F107Rx		STM32F105Vx			STM32F107Vx	
Flash memory in Kbytes		64	128	256	128	256	64	128	256	128	256
SRAM in Kbytes		64									
Package		LQFP64					LQFP 100	LQFP 100, BGA 100	LQFP 100	LQFP 100	LQFP 100, BGA 100
Ethernet		No			Yes		No			Yes	
Timers	General-purpose	4									
	Advanced-control	1									
	Basic	2									

Table 5. Pin definitions (continued)

Pins			Pin name	Type[1]	I / O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
BGA100	LQFP64	LQFP100					Default	Remap
K5	-	40	PE9	I/O	FT	PE9	-	TIM1_CH1
-	-	-	V_{SS_7}	S	-	-	-	-
-	-	-	V_{DD_7}	S	-	-	-	-
G6	-	41	PE10	I/O	FT	PE10	-	TIM1_CH2N
H6	-	42	PE11	I/O	FT	PE11	-	TIM1_CH2
J6	-	43	PE12	I/O	FT	PE12	-	TIM1_CH3N
K6	-	44	PE13	I/O	FT	PE13	-	TIM1_CH3
G7	-	45	PE14	I/O	FT	PE14	-	TIM1_CH4
H7	-	46	PE15	I/O	FT	PE15	-	TIM1_BKIN
J7	29	47	PB10	I/O	FT	PB10	I2C2_SCL[8]/USART3_TX[7]/ ETH_MII_RX_ER	TIM2_CH3
K7	30	48	PB11	I/O	FT	PB11	I2C2_SDA[8]/USART3_RX[7]/ ETH_MII_TX_EN/ ETH_RMII_TX_EN	TIM2_CH4
E7	31	49	V_{SS_1}	S	-	V_{SS_1}	-	-
F7	32	50	V_{DD_1}	S	-	V_{DD_1}	-	-
K8	33	51	PB12	I/O	FT	PB12	SPI2_NSS[8]/I2S2_WS[8]/ I2C2_SMBA[8] / USART3_CK[7]/ TIM1_BKIN[7] / CAN2_RX/ ETH_MII_TXD0/ ETH_RMII_TXD0	-
J8	34	52	PB13	I/O	FT	PB13	SPI2_SCK[8] / I2S2_CK[8] / USART3_CTS[7]/ TIM1_CH1N/CAN2_TX/ ETH_MII_TXD1/ ETH_RMII_TXD1	-
H8	35	53	PB14	I/O	FT	PB14	SPI2_MISO[8] / TIM1_CH2N / USART3_RTS[7]	-
G8	36	54	PB15	I/O	FT	PB15	SPI2_MOSI[8] / I2S2_SD[8] / TIM1_CH3N[7]	-
K9	-	55	PD8	I/O	FT	PD8	-	USART3_TX/ ETH_MII_RX_DV/ ETH_RMII_CRS_DV

5.1.6 Power supply scheme

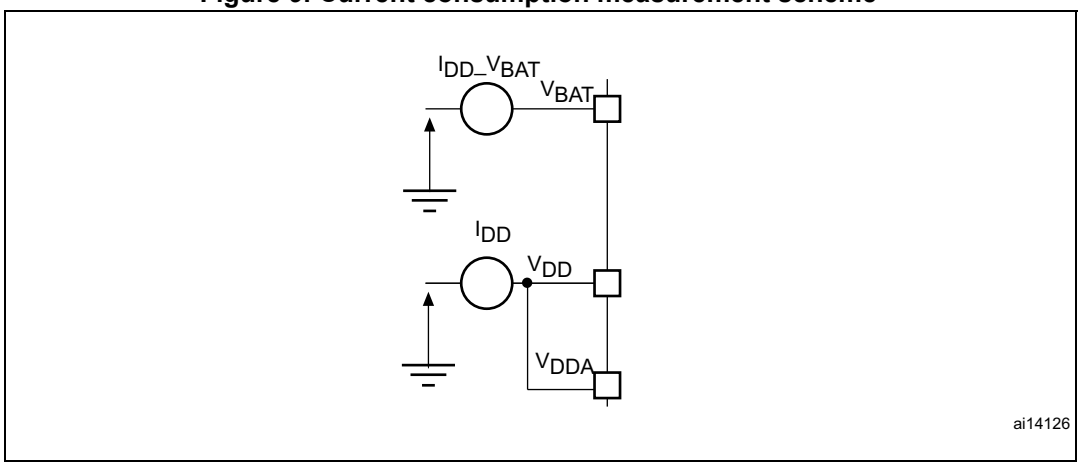
Figure 8. Power supply scheme



Caution: In *Figure 8*, the 4.7 µF capacitor must be connected to V_{DD3}.

5.1.7 Current consumption measurement

Figure 9. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 6: Voltage characteristics*, *Table 7: Current characteristics*, and *Table 8: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five volt tolerant pin	V_{SS} –0.3	V_{DD} +4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.11: Absolute maximum ratings (electrical sensitivity)*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 7: Current characteristics* for the maximum allowed injected current values.

Table 7. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	–25	
$I_{INJ(PIN)}$(2)	Injected current on five volt tolerant pins(3)	-5/+0	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See *Note: on page 76*.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 6: Voltage characteristics* for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 6: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 10. Operating condition at power-up / power down

Symbol	Parameter	Condition	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	-	µs/V
T_J	V_{DD} fall time rate		20	-	

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 11* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 11. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8(1)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	40	-	mV
$T_{RSTTEMPO}$(2)	Reset temporization	-	1	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.

Figure 10. Typical current consumption on V_{BAT} with RTC on vs. temperature at different V_{BAT} values

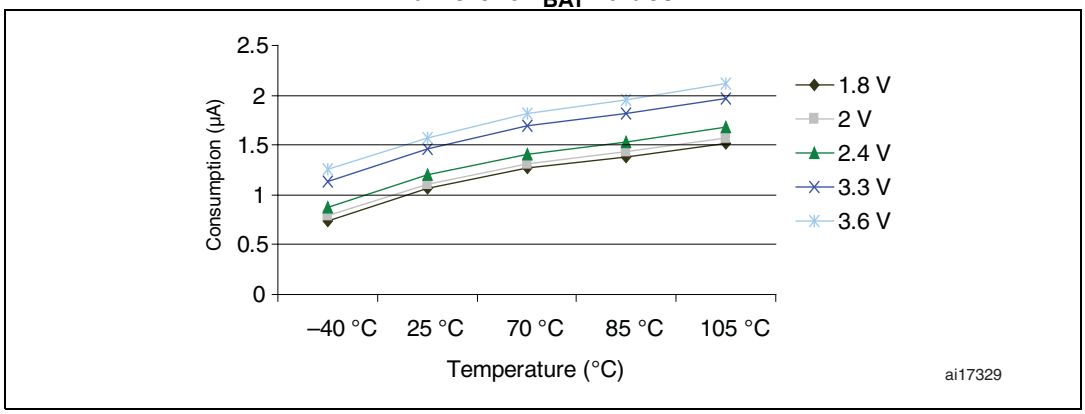
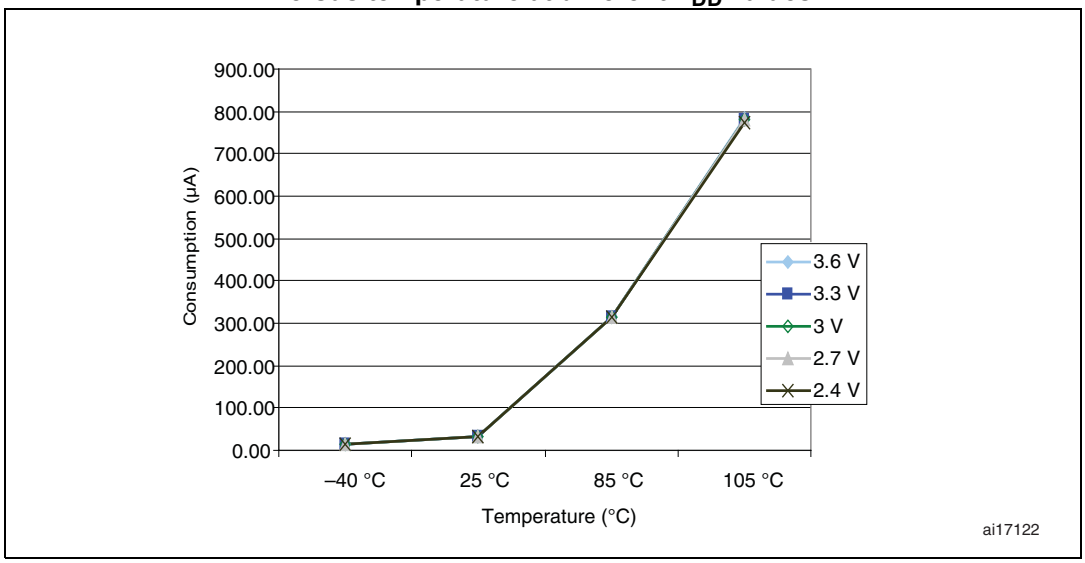


Figure 11. Typical current consumption in Stop mode with regulator in Run mode versus temperature at different V_{DD} values



Low-speed external user clock generated from an external source

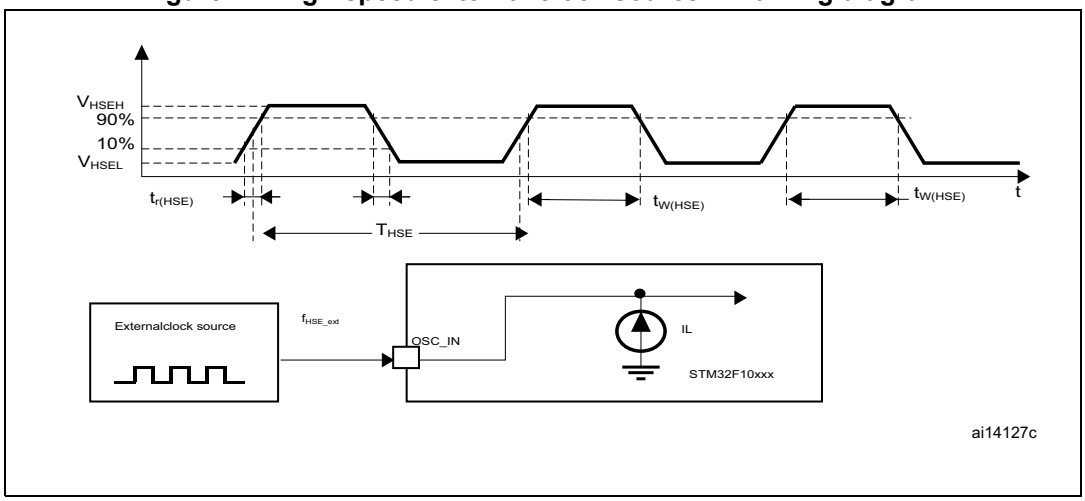
The characteristics given in *Table 21* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 9*.

Table 21. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-		32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	5		pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Figure 14. High-speed external clock source AC timing diagram



All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 26. Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	1.8	µs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	3.6	µs
	Wakeup from Stop mode (regulator in low power mode)	5.4	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	50	µs

1. The wakeup times are measured from the wakeup event to the point in which the user application code reads the first instruction.

5.3.8 PLL, PLL2 and PLL3 characteristics

The parameters given in *Table 27* and *Table 28* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 27. PLL characteristics

Symbol	Parameter	Min(1)	Max(1)	Unit
f_{PLL_IN}	PLL input clock(2)	3	12	MHz
	Pulse width at high level	30	-	ns
f_{PLL_OUT}	PLL multiplier output clock	18	72	MHz
f_{VCO_OUT}	PLL VCO output	36	144	MHz
t_{LOCK}	PLL lock time	-	350	µs
Jitter	Cycle-to-cycle jitter	-	300	ps

1. Based on characterization, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

Table 28. PLL2 and PLL3 characteristics

Symbol	Parameter	Min(1)	Max(1)	Unit
f_{PLL_IN}	PLL input clock(2)	3	5	MHz
	Pulse width at high level	30	-	ns
f_{PLL_OUT}	PLL multiplier output clock	40	74	MHz
f_{VCO_OUT}	PLL VCO output	80	148	MHz
t_{LOCK}	PLL lock time	-	350	µs
Jitter	Cycle-to-cycle jitter	-	400	ps

1. Based on characterization, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 29. Flash memory characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	52.5	70	µs
t_{ERASE}	Page (1 KB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Read mode f_{HCLK} = 72 MHz with 2 wait states, V_{DD} = 3.3 V	-	-	20	mA
		Write / Erase modes f_{HCLK} = 72 MHz, V_{DD} = 3.3 V	-	-	5	mA
		Power-down mode / Halt, V_{DD} = 3.0 to 3.6 V	-	-	50	µA
V_{prog}	Programming voltage	-	2	-	3.6	V

1. Guaranteed by design, not tested in production.

Table 30. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	-	-	Kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	-	-	Years
		1 kcycle(2) at T_A = 105 °C	10	-	-	
		10 kcycles(2) at T_A = 55 °C	20	-	-	

1. Based on characterization, not tested in production.
2. Cycling performed over the whole temperature range.

5.3.10 EMC characteristics

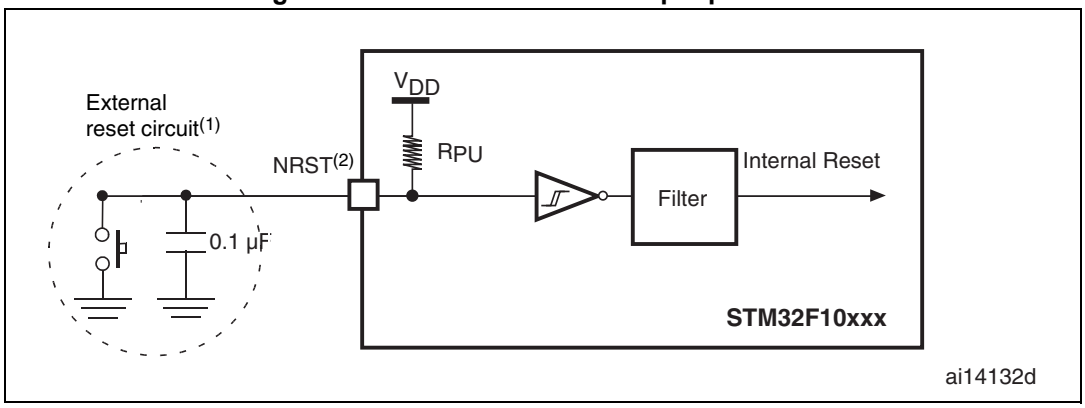
Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

Figure 23. Recommended NRST pin protection



2. The reset network protects the device against parasitic resets.
3. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 39*. Otherwise the reset will not be taken into account by the device.

5.3.15 TIM timer characteristics

The parameters given in *Table 40* are guaranteed by design.

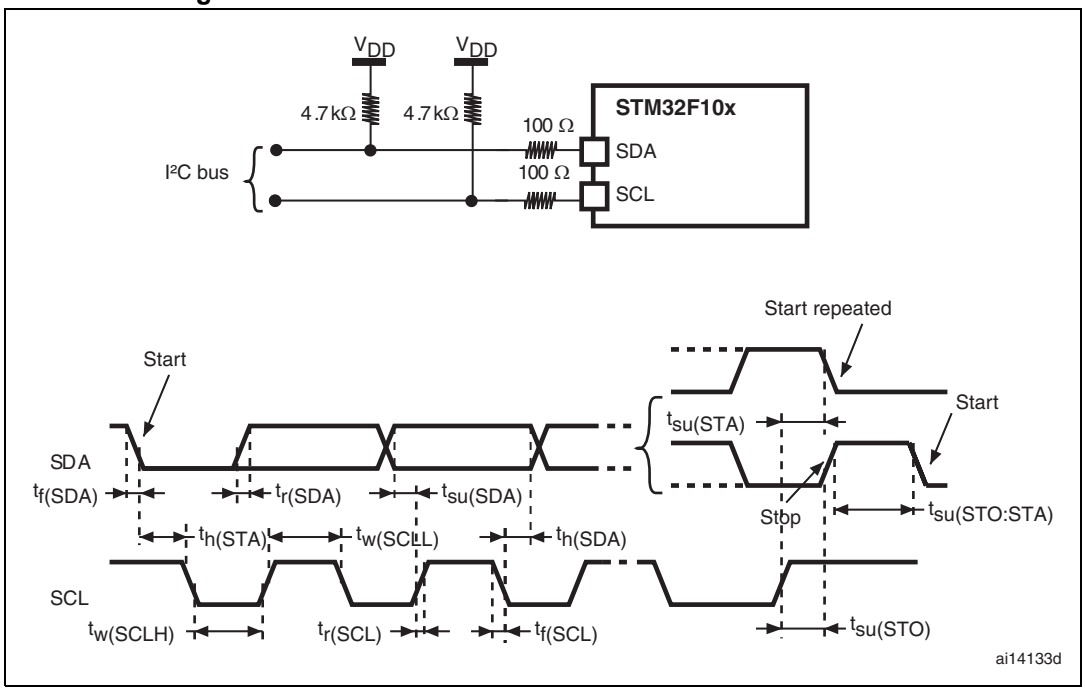
Refer to *Section 5.3.12: I/O current injection characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 40. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	36	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.0139	910	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.6	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM4 and TIM5 timers.

Figure 24. I²C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 42. SCL frequency (f_{PCLK1}= 36 MHz.,V_{DD} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

Table 44. I^2S characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master data: 16 bits, audio freq = 48 K		1.52	1.54	MHz
		Slave		0	6.5	
$t_{r(CK)}$ $t_{f(CK)}$	I^2S clock rise and fall time	capacitive load C_L = 50 pF		-	8	ns
$t_{w(CKH)}$ (1)	I^2S clock high time	Master f_{PCLK} = 16 MHz, audio freq = 48 K		317	320	
$t_{w(CKL)}$ (1)	I^2S clock low time			333	336	
$t_{v(WS)}$ (1)	WS valid time	Master mode		3	-	
$t_{h(WS)}$ (1)	WS hold time	Master mode	I2S2	0	-	
			I2S3	0	-	
$t_{su(WS)}$ (1)	WS setup time	Slave mode	I2S2	4	-	
			I2S3	9	-	
$t_{h(WS)}$ (1)	WS hold time	Slave mode		0	-	
DuCy(SCK)	I2S slave input clock duty cycle	Slave mode		30	70	%
$t_{su(SD\_MR)}$ (1)	Data input setup time	Master receiver	I2S2	8	-	ns
			I2S3	10	-	
$t_{su(SD\_SR)}$ (1)		Slave receiver	I2S2	3	-	
			I2S3	8	-	
$t_{h(SD\_MR)}$ (1)	Data input hold time	Master receiver	I2S2	2	-	
			I2S3	4	-	
$t_{h(SD\_SR)}$ (1)		Slave receiver	I2S2	2	-	
			I2S3	4	-	
$t_{v(SD\_ST)}$ (1)(3)	Data output valid time	Slave transmitter (after enable edge)	I2S2	23	-	
			I2S3	33	-	
$t_{h(SD\_ST)}$ (1)	Data output hold time	Slave transmitter (after enable edge)	I2S2	29	-	
			I2S3	27	-	
$t_{v(SD\_MT)}$ (1)	Data output valid time	Master transmitter (after enable edge)	I2S2	-	5	
			I2S3	-	2	
$t_{h(SD\_MT)}$ (1)	Data output hold time	Master transmitter (after enable edge)	I2S2	11	-	
			I2S3	4	-	

1. Based on design simulation and/or characterization results, not tested in production.

Table 54. ADC accuracy - limited test conditions(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 V to 3.6 V T_A = 25 °C Measurements made after ADC calibration	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	

1. ADC DC accuracy values are measured after internal calibration.
2. Based on characterization, not tested in production.

Table 55. ADC accuracy(1) (2)

Symbol	Parameter	Test conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
3. Based on characterization, not tested in production.

Note: ADC accuracy vs. negative injection current: Injecting a negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative currents.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.

Figure 34. ADC accuracy characteristics

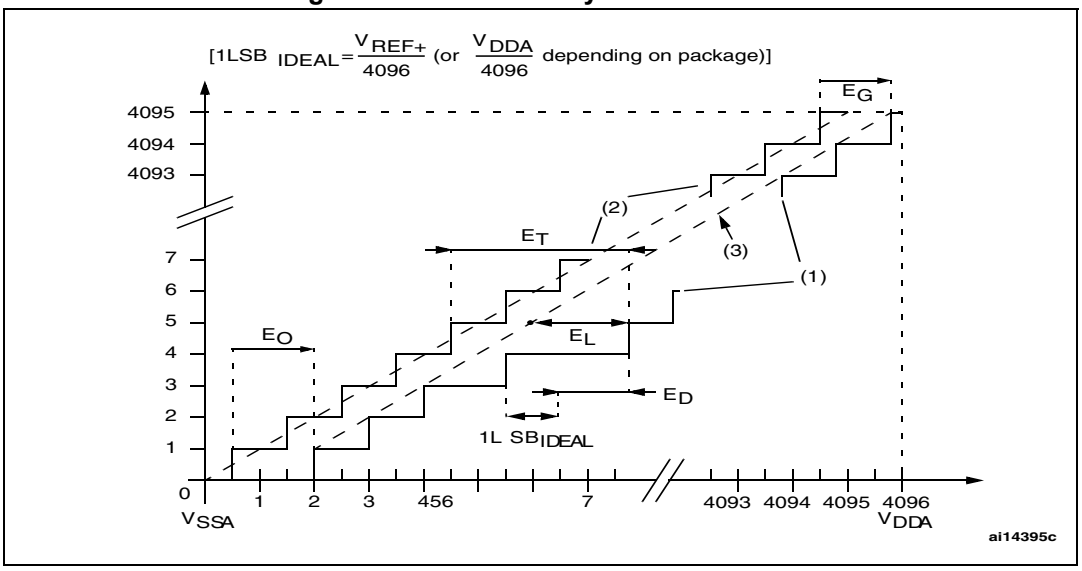
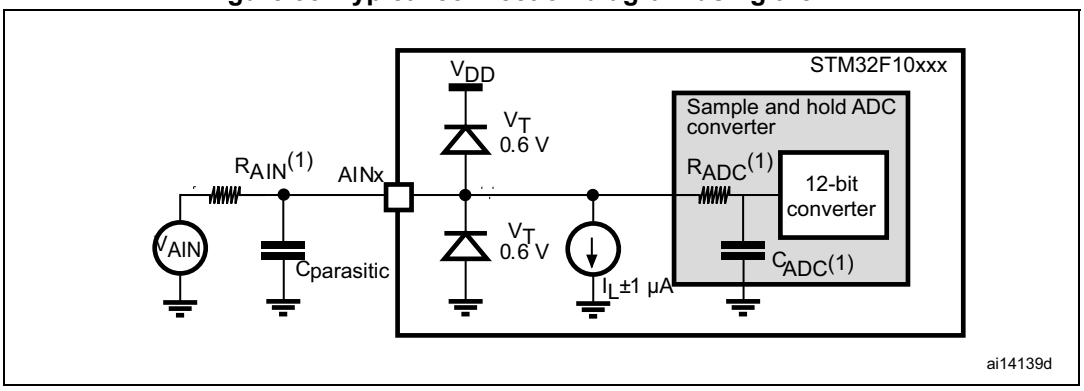


Figure 35. Typical connection diagram using the ADC



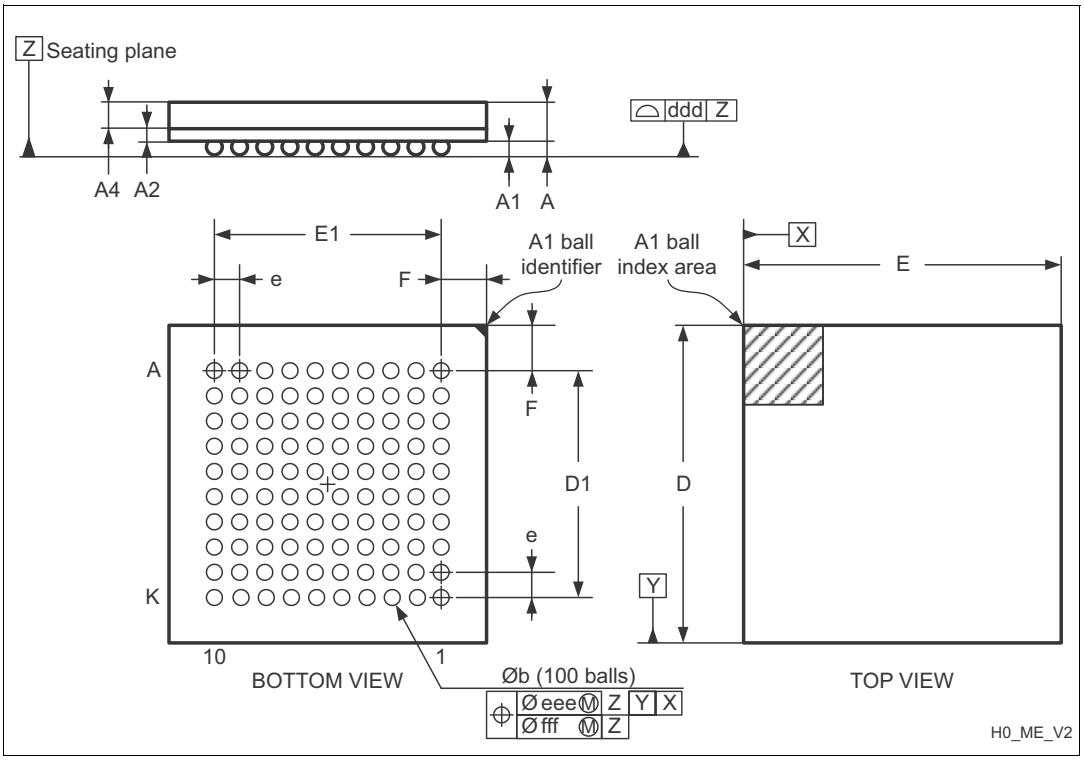
1. Refer to *Table 52* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

6.1 LFBGA100 package information

Figure 39. LFBGA100 - 10 x 10 mm low profile fine pitch ball grid array package outline



Using the values obtained in *Table 61* T_{Jmax} is calculated as follows:

– For LQFP100, 46 °C/W

T_{Jmax} = 115 °C + (46 °C/W × 134 mW) = 115 °C + 6.2 °C = 121.2 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 62: Ordering information scheme*).

Figure 49. LQFP100 P_D max vs. T_A

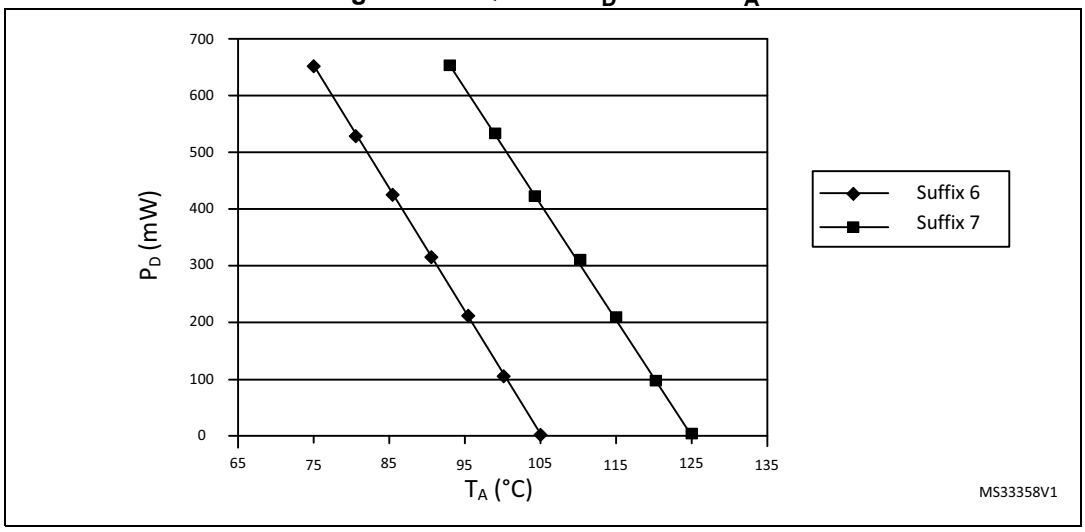
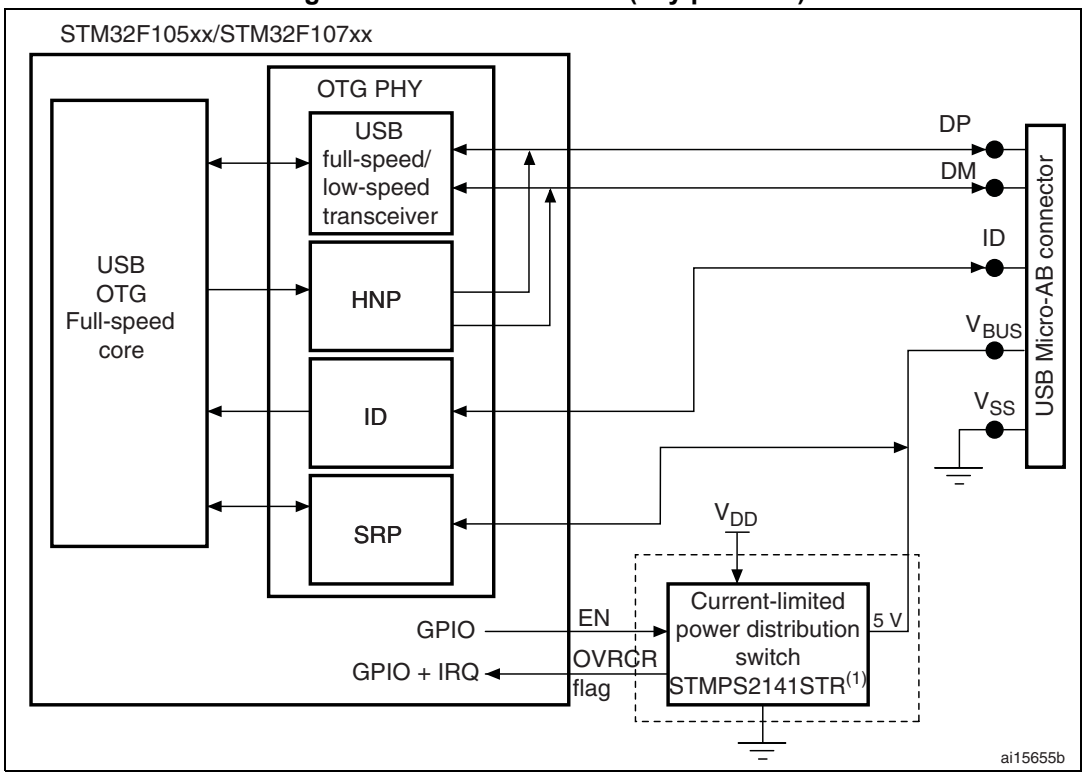


Figure 52. OTG connection (any protocol)



1. STMPS2141STR needed only if the application has to support bus-powered devices.

Table 65. Document revision history (continued)

Date	Revision	Changes
14-Sep-2009	4	Document status promoted from Preliminary data to full datasheet. Number of DACs corrected in *Table 3: STM32F105xx and STM32F107xx family versus STM32F103xx family*. *Note 5* added in *Table 5: Pin definitions*. V_{RERINT} and T_{Coeff} added to *Table 12: Embedded internal reference voltage*. Values added to *Table 13: Maximum current consumption in Run mode, code with data processing running from Flash*, *Table 14: Maximum current consumption in Run mode, code with data processing running from RAM* and *Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM*. Typical I_{DD_VBAT} value added in *Table 16: Typical and maximum current consumptions in Stop and Standby modes*. *Figure 10: Typical current consumption on VBAT with RTC on vs. temperature at different VBAT values* added. Values modified in *Table 17: Typical current consumption in Run mode, code with data processing running from Flash* and *Table 18: Typical current consumption in Sleep mode, code running from Flash or RAM*. f_{HSE_ext} min modified in *Table 20: High-speed external user clock characteristics*. C_{L1} and C_{L2} replaced by C in *Table 22: HSE 3-25 MHz oscillator characteristics* and *Table 23: LSE oscillator characteristics (fLSE = 32.768 kHz)*, notes modified and moved below the tables. *Note 1* modified below *Figure 16: Typical application with an 8 MHz crystal*. Conditions removed from *Table 26: Low-power mode wakeup timings*. Standards modified in *Section 5.3.10: EMC characteristics on page 54*, conditions modified in *Table 31: EMS characteristics*. Jitter maximum values added to *Table 27: PLL characteristics* and *Table 28: PLL2 and PLL3 characteristics*. R_{PU} and R_{PD} modified in *Table 36: I/O static characteristics*. Condition added for $V_{NF(NRST)}$ parameter in *Table 39: NRST pin characteristics*. Note removed and R_{PD}, R_{PU} values added in *Table 46: USB OTG FS DC electrical characteristics*. *Table 48: Ethernet DC electrical characteristics* added. Parameter values added to *Table 49: Dynamic characteristics: Ethernet MAC signals for SMI*, *Table 50: Dynamic characteristics: Ethernet MAC signals for RMII* and *Table 51: Dynamic characteristics: Ethernet MAC signals for MII*. C_{ADC} and R_{AIN} parameters modified in *Table 52: ADC characteristics*. R_{AIN} max values modified in *Table 53: RAIN max for fADC = 14 MHz*. *Table 56: DAC characteristics* modified. *Figure 38: 12-bit buffered /non-buffered DAC* added. *Table 64: Applicative current consumption in Run mode, code with data processing running from Flash* added. Small text changes.

Table 65. Document revision history (continued)

Date	Revision	Changes
11-May-2010	5	Added BGA package. *Table 5: Pin definitions*: ETH_RMII_RXD0 and ETH_RMII_RXD1 added in remap column for PD9 and PD10, respectively. Note added to ETH_MII_RX_DV, ETH_MII_RXD0, ETH_MII_RXD1, ETH_MII_RXD2 and ETH_MII_RXD3 Updated *Table 36: I/O static characteristics on page 57* Added *Figure 18: Standard I/O input characteristics - CMOS port* to *Figure 21: 5 V tolerant I/O input characteristics - TTL port* Updated *Table 43: SPI characteristics on page 66*. Updated *Table 44: I2S characteristics on page 69*. Updated *Table 48: Ethernet DC electrical characteristics on page 72*. Updated *Table 49: Dynamic characteristics: Ethernet MAC signals for SMI on page 72*. Updated *Table 50: Dynamic characteristics: Ethernet MAC signals for RMII on page 73* Updated *Figure 59: USB O44TG FS + Ethernet solution on page 100*. Updated *Figure 60: USB OTG FS + I2S (Audio) solution on page 100*
01-Aug-2011	6	Changed SRAM size to 64 KB on all parts. Updated PD0 and PD1 description in *Table 5: Pin definitions on page 27* Updated footnotes below *Table 6: Voltage characteristics on page 36* and *Table 7: Current characteristics on page 36* Updated tw min in *Table 20: High-speed external user clock characteristics on page 47* Updated startup time in *Table 23: LSE oscillator characteristics (fLSE = 32.768 kHz) on page 50* Added *Section 5.3.12: I/O current injection characteristics on page 56* Updated *Table 36: I/O static characteristics on page 57* Add Interna code V to *Table 62: Ordering information scheme on page 94*
06-Mar-2014	7	Added a “Packing” entry to *Table 62: Ordering information scheme* including “Blank = tray” and “TR = Tape and reel”. Referenced 4 Figures: *Figure 41*, *Figure 49*, *Figure 59* and *Figure 60*. Updated the “Package” line with “BGA100” in *Table 2: STM32F105xx and STM32F107xx features and peripheral counts*.