

Welcome to [E-XFL.COM](https://www.e-xfl.com)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, Ethernet, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LFBGA
Supplier Device Package	100-LFBGA (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f107vch6">https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f107vch6</a>

Table 45.	USB OTG FS startup time	71
Table 46.	USB OTG FS DC electrical characteristics	71
Table 47.	USB OTG FS electrical characteristics	72
Table 48.	Ethernet DC electrical characteristics	72
Table 49.	Dynamic characteristics: Ethernet MAC signals for SMI	72
Table 50.	Dynamic characteristics: Ethernet MAC signals for RMII	73
Table 51.	Dynamic characteristics: Ethernet MAC signals for MII	74
Table 52.	ADC characteristics	74
Table 53.	$R_{AIN}$ max for $f_{ADC} = 14$ MHz	75
Table 54.	ADC accuracy - limited test conditions	76
Table 55.	ADC accuracy	76
Table 56.	DAC characteristics	79
Table 57.	TS characteristics	81
Table 58.	LFBGA100 recommended PCB design rules (0.8 mm pitch BGA)	83
Table 59.	LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data	85
Table 60.	LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data	88
Table 61.	Package thermal characteristics	91
Table 62.	Ordering information scheme	94
Table 63.	PLL configurations	101
Table 64.	Applicative current consumption in Run mode, code with data processing running from Flash	102
Table 65.	Document revision history	103

### 2.3.1 ARM Cortex-M3 core with embedded Flash and SRAM

The ARM Cortex-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

With its embedded ARM core, STM32F105xx and STM32F107xx connectivity line family is compatible with all ARM tools and software.

[Figure 1](#) shows the general block diagram of the device family.

### 2.3.2 Embedded Flash memory

64 to 256 Kbytes of embedded Flash is available for storing programs and data.

### 2.3.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

### 2.3.4 Embedded SRAM

64 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

### 2.3.5 Nested vectored interrupt controller (NVIC)

The STM32F105xx and STM32F107xx connectivity line embeds a nested vectored interrupt controller able to handle up to 67 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

Any of the standard timers can be used to generate PWM outputs. Each of the timers has independent DMA request generations.

### Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

### Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

## 2.3.16 I<sup>2</sup>C bus

Up to two I<sup>2</sup>C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

## 2.3.17 Universal synchronous/asynchronous receiver transmitters (USARTs)

The STM32F105xx and STM32F107xx connectivity line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART1 interface is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s.

USART1, USART2 and USART3 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

### 2.3.18 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC/SDHC<sup>(a)</sup> modes.

All SPIs can be served by the DMA controller.

### 2.3.19 Inter-integrated sound (I<sup>2</sup>S)

Two standard I<sup>2</sup>S interfaces (multiplexed with SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 96 kHz are supported. When either or both of the I<sup>2</sup>S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency with less than 0.5% accuracy error owing to the advanced clock controller (see [Section 2.3.7: Clocks and startup](#)).

Refer to the “Audio frequency precision” tables provided in the “Serial peripheral interface (SPI)” section of the STM32F10xxx reference manual.

### 2.3.20 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

Peripheral not available on STM32F105xx devices.

The STM32F107xx devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard media-independent interface (MII) or a reduced media-independent interface (RMII). The STM32F107xx requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). the PHY is connected to the STM32F107xx MII port using as many as 17 signals (MII) or 9 signals (RMII) and can be clocked using the 25 MHz (MII) or 50 MHz (RMII) output from the STM32F107xx.

The STM32F107xx includes the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors (see the STM32F105xx/STM32F107xx reference manual for details)
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support

---

a. SDHC = Secure digital high capacity.

- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes, that is 4 Kbytes in total
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 with the timestamp comparator connected to the TIM2 trigger input
- Triggers interrupt when system time becomes greater than target time

### 2.3.21 Controller area network (CAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOs with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). The 256 bytes of SRAM which are allocated for each CAN (512 bytes in total) are not shared with any other peripheral.

### 2.3.22 Universal serial bus on-the-go full-speed (USB OTG FS)

The STM32F105xx and STM32F107xx connectivity line devices embed a USB OTG full-speed (12 Mb/s) device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- 1.25 KB of SRAM used exclusively by the endpoints (not shared with any other peripheral)
- 4 bidirectional endpoints
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected
- the SOF output can be used to synchronize the external audio DAC clock in isochronous mode
- in accordance with the USB 2.0 Specification, the supported transfer speeds are:
  - in Host mode: full speed and low speed
  - in Device mode: full speed

### 2.3.23 GPIOs (general-purpose inputs/outputs)

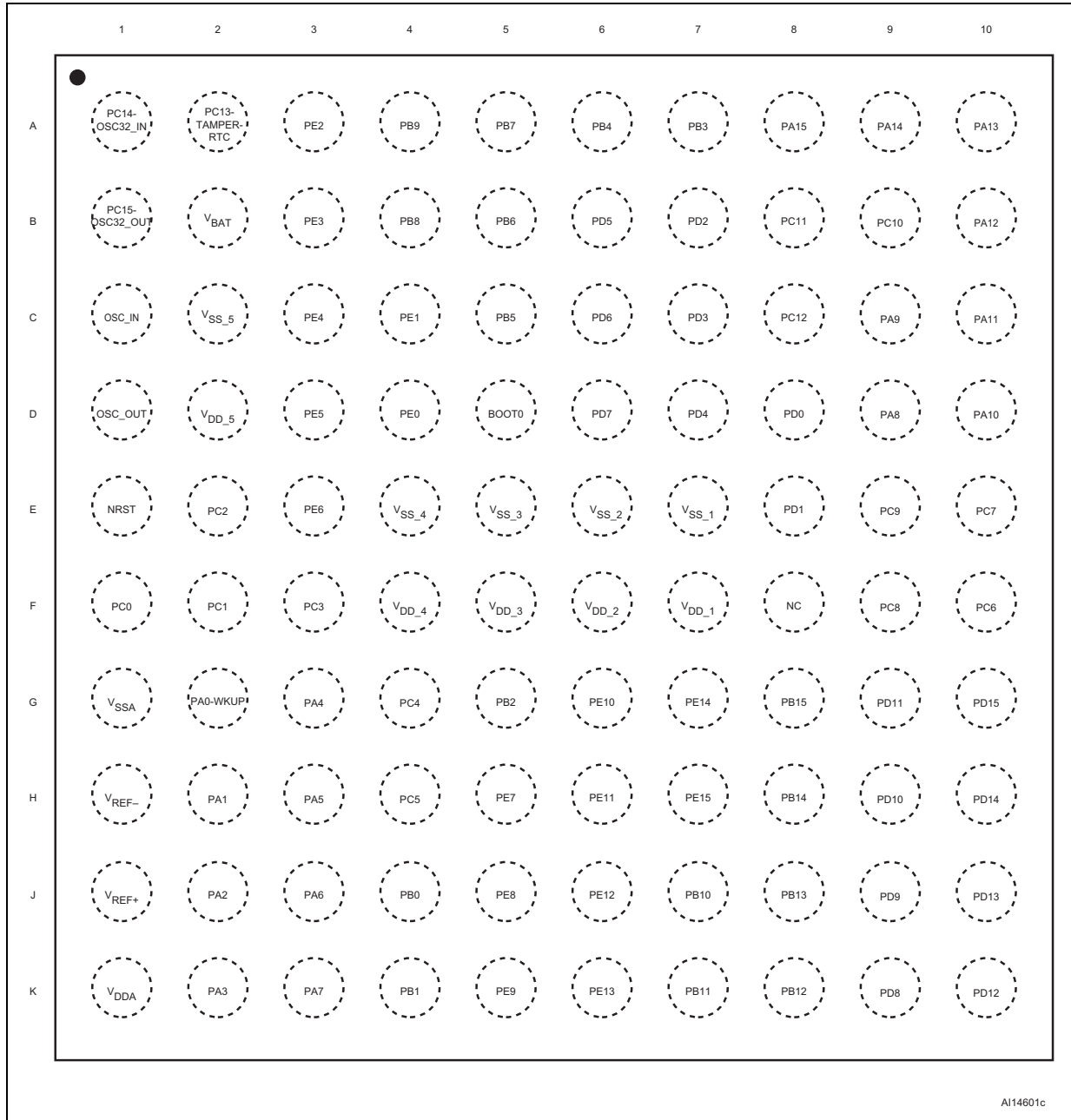
Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

I/Os on APB2 with up to 18 MHz toggling speed

### 3 Pinouts and pin description

Figure 2. STM32F105xx and STM32F107xx connectivity line BGA100 ballout top view



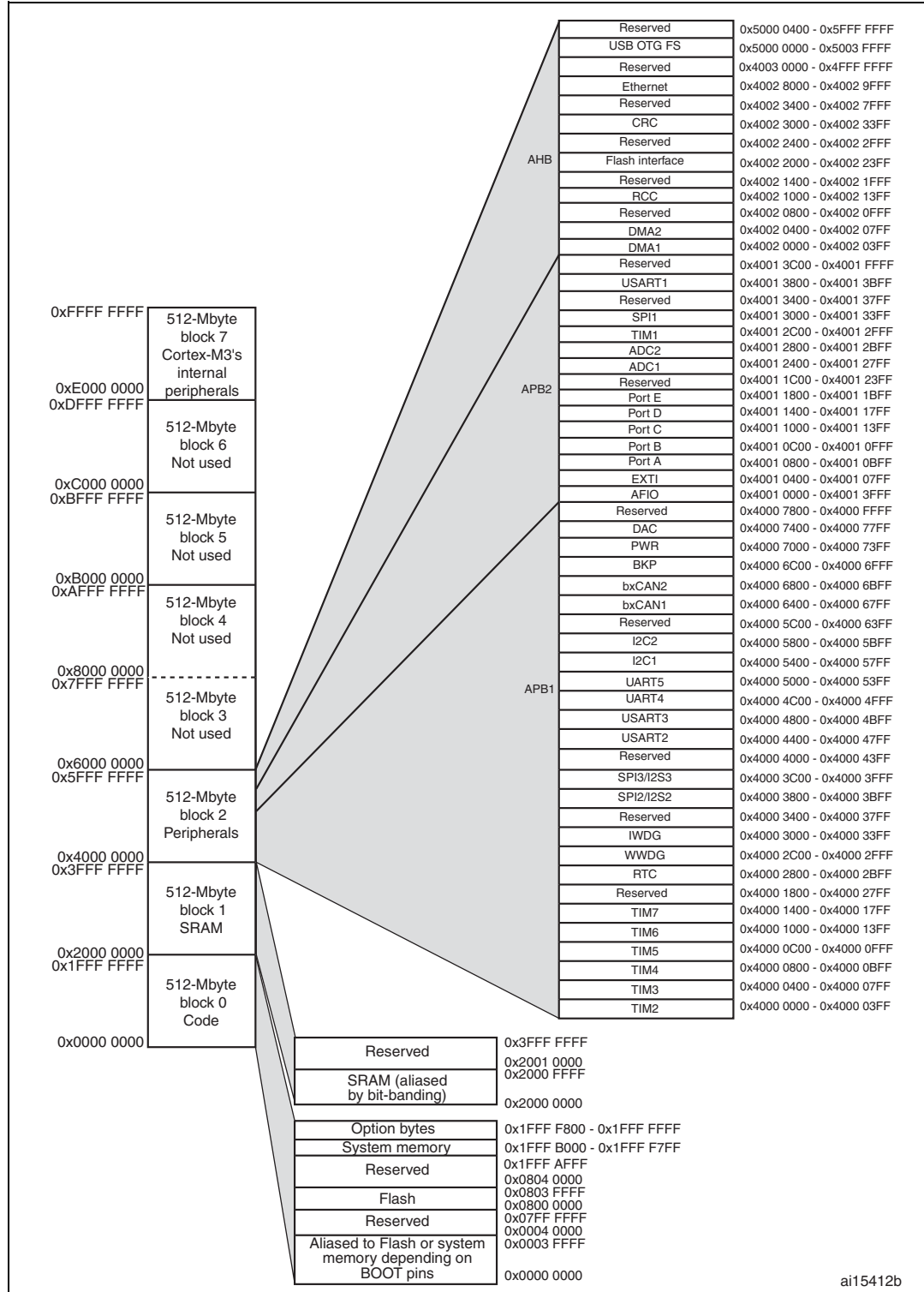
1. I = input, O = output, S = supply, HiZ = high impedance.
2. FT = 5 V tolerant. All I/Os are  $V_{DD}$  capable.
3. Function availability depends on the chosen device.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch, and so their use in output mode is limited: they can be used only in output 2 MHz mode with a maximum load of 30 pF and only one pin can be put in output mode at a time.
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: [www.st.com](http://www.st.com).
7. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: [www.st.com](http://www.st.com).
8. SPI2/I2S2 and I2C2 are not available when the Ethernet is being used.
9. For the LQFP64 package, the pins number 5 and 6 are configured as OSC\_IN/OSC\_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 and BGA100 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.



# 4 Memory mapping

The memory map is shown in *Figure 5*.

Figure 5. Memory map



## 5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 6: Voltage characteristics](#), [Table 7: Current characteristics](#), and [Table 8: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 6. Voltage characteristics**

Symbol	Ratings	Min	Max	Unit
$V_{DD}-V_{SS}$	External main supply voltage (including $V_{DDA}$ and $V_{DD}$ ) <sup>(1)</sup>	-0.3	4.0	V
$V_{IN}$ <sup>(2)</sup>	Input voltage on five volt tolerant pin	$V_{SS}-0.3$	$V_{DD}+4.0$	
	Input voltage on any other pin	$V_{SS}-0.3$	4.0	
$ \Delta V_{DDx} $	Variations between different $V_{DD}$ power pins	-	50	mV
$ V_{SSx}-V_{SS} $	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see <a href="#">Section 5.3.11: Absolute maximum ratings (electrical sensitivity)</a>		-

- All main power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply, in the permitted range.
- $V_{IN}$  maximum must always be respected. Refer to [Table 7: Current characteristics](#) for the maximum allowed injected current values.

**Table 7. Current characteristics**

Symbol	Ratings	Max.	Unit
$I_{VDD}$	Total current into $V_{DD}/V_{DDA}$ power lines (source) <sup>(1)</sup>	150	mA
$I_{VSS}$	Total current out of $V_{SS}$ ground lines (sink) <sup>(1)</sup>	150	
$I_{IO}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	
$I_{INJ(PIN)}$ <sup>(2)</sup>	Injected current on five volt tolerant pins <sup>(3)</sup>	-5/+0	
	Injected current on any other pin <sup>(4)</sup>	$\pm 5$	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) <sup>(5)</sup>	$\pm 25$	

- All main power ( $V_{DD}$ ,  $V_{DDA}$ ) and ground ( $V_{SS}$ ,  $V_{SSA}$ ) pins must always be connected to the external power supply, in the permitted range.
- Negative injection disturbs the analog performance of the device. See [Note: on page 76](#).
- Positive injection is not possible on these I/Os. A negative injection is induced by  $V_{IN}<V_{SS}$ .  $I_{INJ(PIN)}$  must never be exceeded. Refer to [Table 6: Voltage characteristics](#) for the maximum allowed input voltage values.
- A positive injection is induced by  $V_{IN}>V_{DD}$  while a negative injection is induced by  $V_{IN}<V_{SS}$ .  $I_{INJ(PIN)}$  must never be exceeded. Refer to [Table 6: Voltage characteristics](#) for the maximum allowed input voltage values.
- When several inputs are submitted to a current injection, the maximum  $\Sigma I_{INJ(PIN)}$  is the absolute sum of the positive and negative injected currents (instantaneous values).

### 5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for  $T_A$ .

**Table 10. Operating condition at power-up / power down**

Symbol	Parameter	Condition	Min	Max	Unit
$t_{VDD}$	$V_{DD}$ rise time rate	-	0	-	$\mu\text{s/V}$
$T_J$	$V_{DD}$ fall time rate		20	-	

### 5.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 11](#) are derived from tests performed under ambient temperature and  $V_{DD}$  supply voltage conditions summarized in [Table 9](#).

**Table 11. Embedded reset and power control block characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{PVD}$	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V		
$V_{PVDhyst}^{(2)}$	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8 <sup>(1)</sup>	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}^{(2)}$	PDR hysteresis	-	-	40	-	mV
$T_{RSTTEMPO}^{(2)}$	Reset temporization	-	1	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum  $V_{POR/PDR}$  value.

2. Guaranteed by design, not tested in production.

**Table 18. Typical current consumption in Sleep mode, code running from Flash or RAM**

Symbol	Parameter	Conditions	f <sub>HCLK</sub>	Typ <sup>(1)</sup>		Unit
				All peripherals enabled <sup>(2)</sup>	All peripherals disabled	
I <sub>DD</sub>	Supply current in Sleep mode	External clock <sup>(3)</sup>	72 MHz	28.2	6	mA
			48 MHz	19	4.2	
			36 MHz	14.7	3.4	
			24 MHz	10.1	2.5	
			16 MHz	6.7	2	
			8 MHz	3.2	1.3	
			4 MHz	2.3	1.2	
			2 MHz	1.7	1.16	
			1 MHz	1.5	1.1	
			500 kHz	1.3	1.05	
		125 kHz	1.2	1.05		
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	36 MHz	13.7	2.6	
			24 MHz	9.3	1.8	
			16 MHz	6.3	1.3	
			8 MHz	2.7	0.6	
			4 MHz	1.6	0.5	
			2 MHz	1	0.46	
			1 MHz	0.8	0.44	
			500 kHz	0.6	0.43	
125 kHz	0.5	0.42				

1. Typical values are measures at T<sub>A</sub> = 25 °C, V<sub>DD</sub> = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC\_CR2 register).
3. External clock is 8 MHz and PLL is on when f<sub>HCLK</sub> > 8 MHz.

**On-chip peripheral current consumption**

The current consumption of the on-chip peripherals is given in [Table 19](#). The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V<sub>DD</sub> or V<sub>SS</sub> (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with one peripheral clocked on (with only the clock applied)
- ambient operating temperature and V<sub>DD</sub> supply voltage conditions summarized in [Table 6](#)



Table 19. Peripheral current consumption

Peripheral		Typical consumption at 25 °C	Unit
AHB (up to 72 MHz)	DMA1	14.03	μA/MHz
	DMA2	9.31	
	OTG_fs	111.11	
	ETH-MAC	56.25	
	CRC	1.11	
	BusMatrix <sup>(1)</sup>	15.97	
APB1(up to 36MHz)	APB1-Bridge	9.72	μA/MHz
	TIM2	33.61	
	TIM3	33.06	
	TIM4	32.50	
	TIM5	31.94	
	TIM6	6.11	
	TIM7	6.11	
	SPI2/I2S2 <sup>(2)</sup>	7.50	
	SPI3/I2S3 <sup>(2)</sup>	7.50	
	USART2	10.83	
	USART3	11.11	
	UART4	10.83	
	UART5	10.56	
	I2C1	11.39	
	I2C2	11.11	
	CAN1	19.44	
	CAN2	18.33	
	DAC <sup>(3)</sup>	8.61	
	WWDG	3.33	
	PWR	2.22	
BKP	0.83		
IWDG	3.89		

**Table 23. LSE oscillator characteristics ( $f_{LSE} = 32.768 \text{ kHz}$ ) <sup>(1)</sup> (continued)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$t_{SU(LSE)}$ <sub>(4)</sub>	Startup time	$V_{DD}$ is stabilized	$T_A = 50 \text{ }^\circ\text{C}$	-	1.5	-	s
			$T_A = 25 \text{ }^\circ\text{C}$	-	2.5	-	
			$T_A = 10 \text{ }^\circ\text{C}$	-	4	-	
			$T_A = 0 \text{ }^\circ\text{C}$	-	6	-	
			$T_A = -10 \text{ }^\circ\text{C}$	-	10	-	
			$T_A = -20 \text{ }^\circ\text{C}$	-	17	-	
			$T_A = -30 \text{ }^\circ\text{C}$	-	32	-	
			$T_A = -40 \text{ }^\circ\text{C}$	-	60	-	

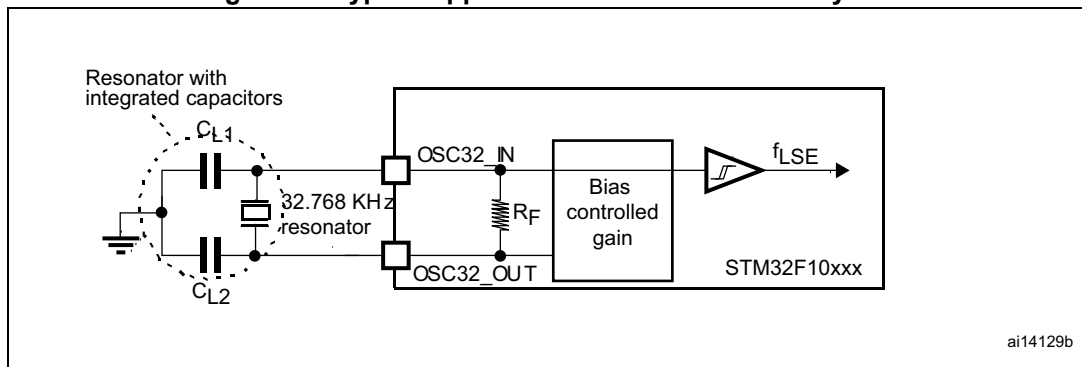
1. Based on characterization, not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small  $R_S$  value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details
4.  $t_{SU(LSE)}$  is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

**Note:** For  $C_{L1}$  and  $C_{L2}$  it is recommended to use high-quality external ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Figure 17).  $C_{L1}$  and  $C_{L2}$  are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of  $C_{L1}$  and  $C_{L2}$ . Load capacitance  $C_L$  has the following formula:  $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$  where  $C_{stray}$  is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

**Caution:** To avoid exceeding the maximum value of  $C_{L1}$  and  $C_{L2}$  (15 pF) it is strongly recommended to use a resonator with a load capacitance  $C_L \leq 7 \text{ pF}$ . Never use a resonator with a load capacitance of 12.5 pF.

**Example:** if you choose a resonator with a load capacitance of  $C_L = 6 \text{ pF}$ , and  $C_{stray} = 2 \text{ pF}$ , then  $C_{L1} = C_{L2} = 8 \text{ pF}$ .

**Figure 17. Typical application with a 32.768 kHz crystal**



ai14129b

**USB OTG FS characteristics**

The USB OTG interface is USB-IF certified (Full-Speed).

**Table 45. USB OTG FS startup time**

Symbol	Parameter	Max	Unit
$t_{STARTUP}^{(1)}$	USB OTG FS transceiver startup time	1	$\mu s$

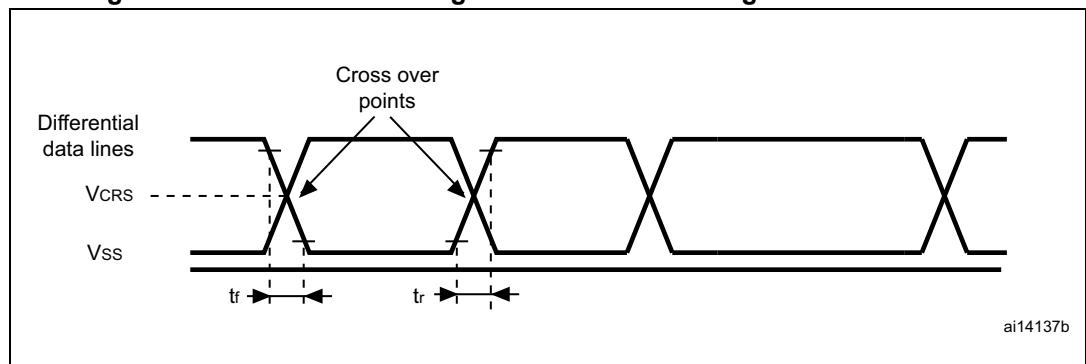
1. Guaranteed by design, not tested in production.

**Table 46. USB OTG FS DC electrical characteristics**

Symbol	Parameter	Conditions	Min. <sup>(1)</sup>	Typ.	Max. <sup>(1)</sup>	Unit	
Input levels	$V_{DD}$	USB OTG FS operating voltage	-	3.0 <sup>(2)</sup>	-	3.6	V
	$V_{DI}^{(3)}$	Differential input sensitivity	I(USBDP, USBDM)	0.2	-	-	V
	$V_{CM}^{(3)}$	Differential common mode range	Includes $V_{DI}$ range	0.8	-	2.5	
	$V_{SE}^{(3)}$	Single ended receiver threshold	-	1.3	-	2.0	
Output levels	$V_{OL}$	Static output level low	$R_L$ of 1.5 k $\Omega$ to 3.6 V <sup>(4)</sup>	-	-	0.3	V
	$V_{OH}$	Static output level high	$R_L$ of 15 k $\Omega$ to $V_{SS}^{(4)}$	2.8	-	3.6	
$R_{PD}$	Pull-down resistance on PA11, PA12	$V_{IN} = V_{DD}$	17	21	24	k $\Omega$	
	Pull-down resistance on PA9		0.65	1.1	2.0		
$R_{PU}$	Pull-up resistance on PA12	$V_{IN} = V_{SS}$	1.5	1.8	2.1		
	Pull-up resistance on PA9	$V_{IN} = V_{SS}$	0.25	0.37	0.55		

1. All the voltages are measured from the local ground potential.
2. The STM32F105xx and STM32F107xx USB OTG FS functionality is ensured down to 2.7 V but not the full USB OTG FS electrical characteristics which are degraded in the 2.7-to-3.0 V  $V_{DD}$  voltage range.
3. Guaranteed by design, not tested in production.
4.  $R_L$  is the load connected on the USB OTG FS drivers

**Figure 30. USB OTG FS timings: definition of data signal rise and fall time**



### 5.3.19 Temperature sensor characteristics

Table 57. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	$V_{SENSE}$ linearity with temperature	-	$\pm 1$	$\pm 2$	$^{\circ}\text{C}$
Avg_Slope <sup>(1)</sup>	Average slope	4.0	4.3	4.6	mV/ $^{\circ}\text{C}$
$V_{25}^{(1)}$	Voltage at 25 $^{\circ}\text{C}$	1.34	1.43	1.52	V
$t_{START}^{(2)}$	Startup time	4	-	10	$\mu\text{s}$
$T_{S\_temp}^{(3)(2)}$	ADC sampling time when reading the temperature	-	-	17.1	$\mu\text{s}$

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

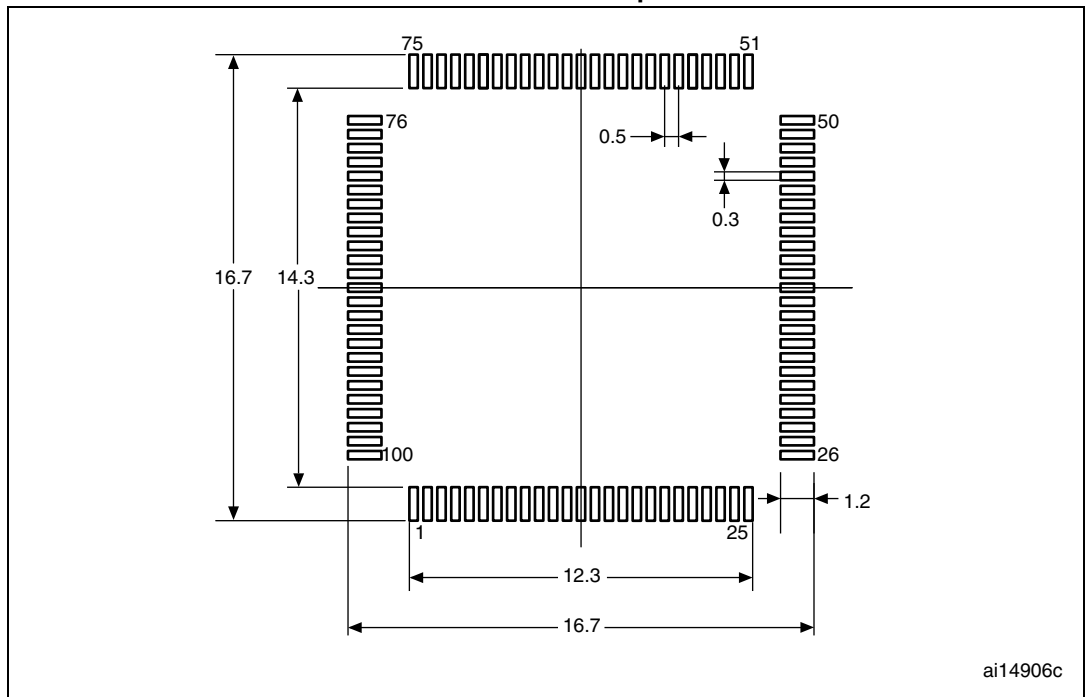


**Table 59. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)**

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 44. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package recommended footprint**



## 6.4.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Table 62: Ordering information scheme](#).

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F103xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

### Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature  $T_{Amax} = 82\text{ °C}$  (measured according to JESD51-2),  
 $I_{DDmax} = 50\text{ mA}$ ,  $V_{DD} = 3.5\text{ V}$ , maximum 20 I/Os used at the same time in output at low level with  $I_{OL} = 8\text{ mA}$ ,  $V_{OL} = 0.4\text{ V}$  and maximum 8 I/Os used at the same time in output at low level with  $I_{OL} = 20\text{ mA}$ ,  $V_{OL} = 1.3\text{ V}$

$$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} + 8 \times 20\text{ mA} \times 1.3\text{ V} = 272\text{ mW}$$

This gives:  $P_{INTmax} = 175\text{ mW}$  and  $P_{IOmax} = 272\text{ mW}$ :

$$P_{Dmax} = 175 + 272 = 447\text{ mW}$$

Thus:  $P_{Dmax} = 447\text{ mW}$

Using the values obtained in [Table 61](#)  $T_{Jmax}$  is calculated as follows:

– For LQFP100,  $46\text{ °C/W}$

$$T_{Jmax} = 82\text{ °C} + (46\text{ °C/W} \times 447\text{ mW}) = 82\text{ °C} + 20.6\text{ °C} = 102.6\text{ °C}$$

This is within the range of the suffix 6 version parts ( $-40 < T_J < 105\text{ °C}$ ).

In this case, parts must be ordered at least with the temperature range suffix 6 (see [Table 62: Ordering information scheme](#)).

### Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature  $T_J$  remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature  $T_{Amax} = 115\text{ °C}$  (measured according to JESD51-2),  
 $I_{DDmax} = 20\text{ mA}$ ,  $V_{DD} = 3.5\text{ V}$ , maximum 20 I/Os used at the same time in output at low level with  $I_{OL} = 8\text{ mA}$ ,  $V_{OL} = 0.4\text{ V}$

$$P_{INTmax} = 20\text{ mA} \times 3.5\text{ V} = 70\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} = 64\text{ mW}$$

This gives:  $P_{INTmax} = 70\text{ mW}$  and  $P_{IOmax} = 64\text{ mW}$ :

$$P_{Dmax} = 70 + 64 = 134\text{ mW}$$

Thus:  $P_{Dmax} = 134\text{ mW}$

Using the values obtained in [Table 61](#)  $T_{Jmax}$  is calculated as follows:

– For LQFP100, 46 °C/W

$$T_{Jmax} = 115\text{ °C} + (46\text{ °C/W} \times 134\text{ mW}) = 115\text{ °C} + 6.2\text{ °C} = 121.2\text{ °C}$$

This is within the range of the suffix 7 version parts ( $-40 < T_J < 125\text{ °C}$ ).

In this case, parts must be ordered at least with the temperature range suffix 7 (see [Table 62: Ordering information scheme](#)).

**Figure 49. LQFP100  $P_D$  max vs.  $T_A$**

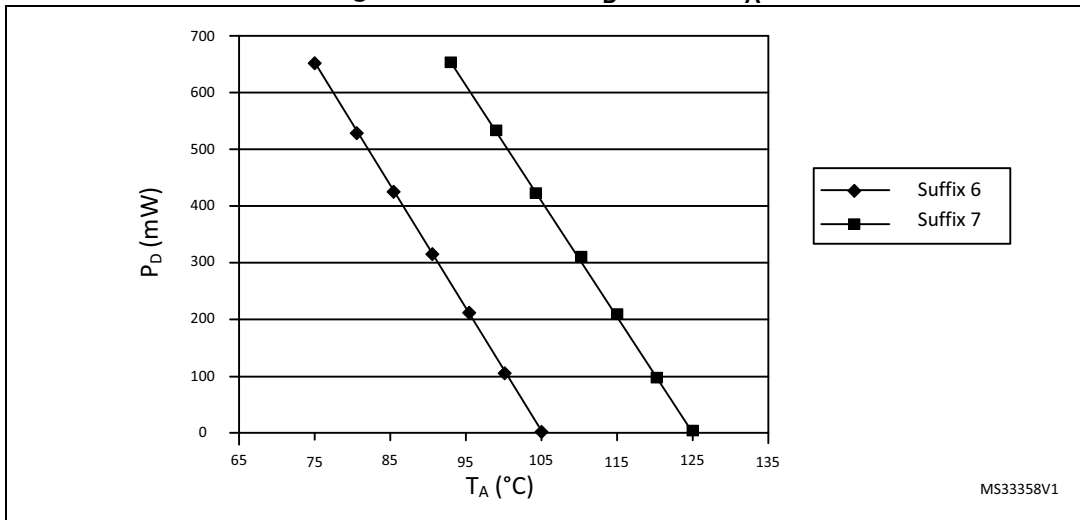


Table 63. PLL configurations

Application	Crystal value in MHz (XT1)	PREDIV2	PLL2MUL	PLLSRC	PREDIV1	PLLMUL	USB prescaler (PLLVCO output)	PLL3MUL	I2Sn clock input	MCO (main clock output)
Ethernet only	25	/5	PLL2ON x8	PLL2	/5	PLLON x9	NA	PLL3ON x10	NA	XT1 (MII) PLL3 (RMII)
Ethernet + OTG	25	/5	PLL2ON x8	PLL2	/5	PLLON x9	/3	PLL3ON x10	NA	XT1 (MII) PLL3 (RMII)
Ethernet + OTG + basic audio	25	/5	PLL2ON x8	PLL2	/5	PLLON x9	/3	PLL3ON x10	PLL	XT1 (MII) PLL3 (RMII)
Ethernet + OTG + Audio class I <sup>2</sup> S <sup>(1)</sup>	14.7456	/4	PLL2ON x12	PLL2	/4	PLLON x6.5	/3	PLL3ON x20	PLL3 VCO Out	NA ETH PHY must use its own crystal
OTG only	8	NA	PLL2OFF	XT1	/1	PLLON x9	/3	PLL3OFF	NA	NA
OTG + basic audio	8	NA	PLL2OFF	XT1	/1	PLLON x9	/3	PLL3OFF	PLL	NA
OTG + Audio class I <sup>2</sup> S <sup>(1)</sup>	14.7456	/4	PLL2ON x12	PLL2	/4	PLLON x6.5	/3	PLL3ON x20	PLL3 VCO Out	NA
Audio class I <sup>2</sup> S only <sup>(1)</sup>	14.7456	/4	PLL2ON x12	PLL2	/4	PLLON x6.5	NA	PLL3ON x20	PLL3 VCO out	NA

1. SYSCLK is set to be at 72 MHz except in this case where SYSCLK is at 71.88 MHz.

Table 64 give the I<sub>DD</sub> run mode values that correspond to the conditions specified in Table 63.

## 8 Revision history

**Table 65. Document revision history**

Date	Revision	Changes
18-Dec-2008	1	Initial release.
20-Feb-2009	2	<p>I/O information clarified <i>on page 1. Figure 4: STM32F105xxx and STM32F107xxx connectivity line BGA100 ballout top view</i> corrected.</p> <p><i>Section 2.3.8: Boot modes</i> updated.</p> <p>PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column, plus small additional changes in <i>Table 5: Pin definitions</i>.</p> <p>Consumption values modified in <i>Section 5.3.5: Supply current characteristics</i>.</p> <p>Note modified in <i>Table 13: Maximum current consumption in Run mode, code with data processing running from Flash</i> and <i>Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM</i>.</p> <p><i>Table 20: High-speed external user clock characteristics</i> and <i>Table 21: Low-speed external user clock characteristics</i> modified.</p> <p><i>Table 27: PLL characteristics</i> modified and <i>Table 28: PLL2 and PLL3 characteristics</i> added.</p>