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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, SPI, UART/USART, USB OTG
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f107vct7

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2.3.15 Timers and watchdogs

The STM32F105xx and STM32F107xx devices include an advanced-control timer, four general-purpose timers, two basic timers, two watchdog timers and a SysTick timer.

Table 4 compares the features of the general-purpose and basic timers.

Table 4. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TIMx (TIM2, TIM3, TIM4, TIM5)	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Advanced-control timer (TIM1)

The advanced control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard TIM timers which have the same architecture. The advanced control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are up to 4 synchronizable standard timers (TIM2, TIM3, TIM4 and TIM5) embedded in the STM32F105xx and STM32F107xx connectivity line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one pulse mode output. This gives up to 16 input captures / output compares / PWMs on the largest packages. They can work together with the Advanced Control timer via the Timer Link feature for synchronization or event chaining.

The counter can be frozen in debug mode.

3 Pinouts and pin description

Figure 2. STM32F105xx and STM32F107xx connectivity line BGA100 ballout top view

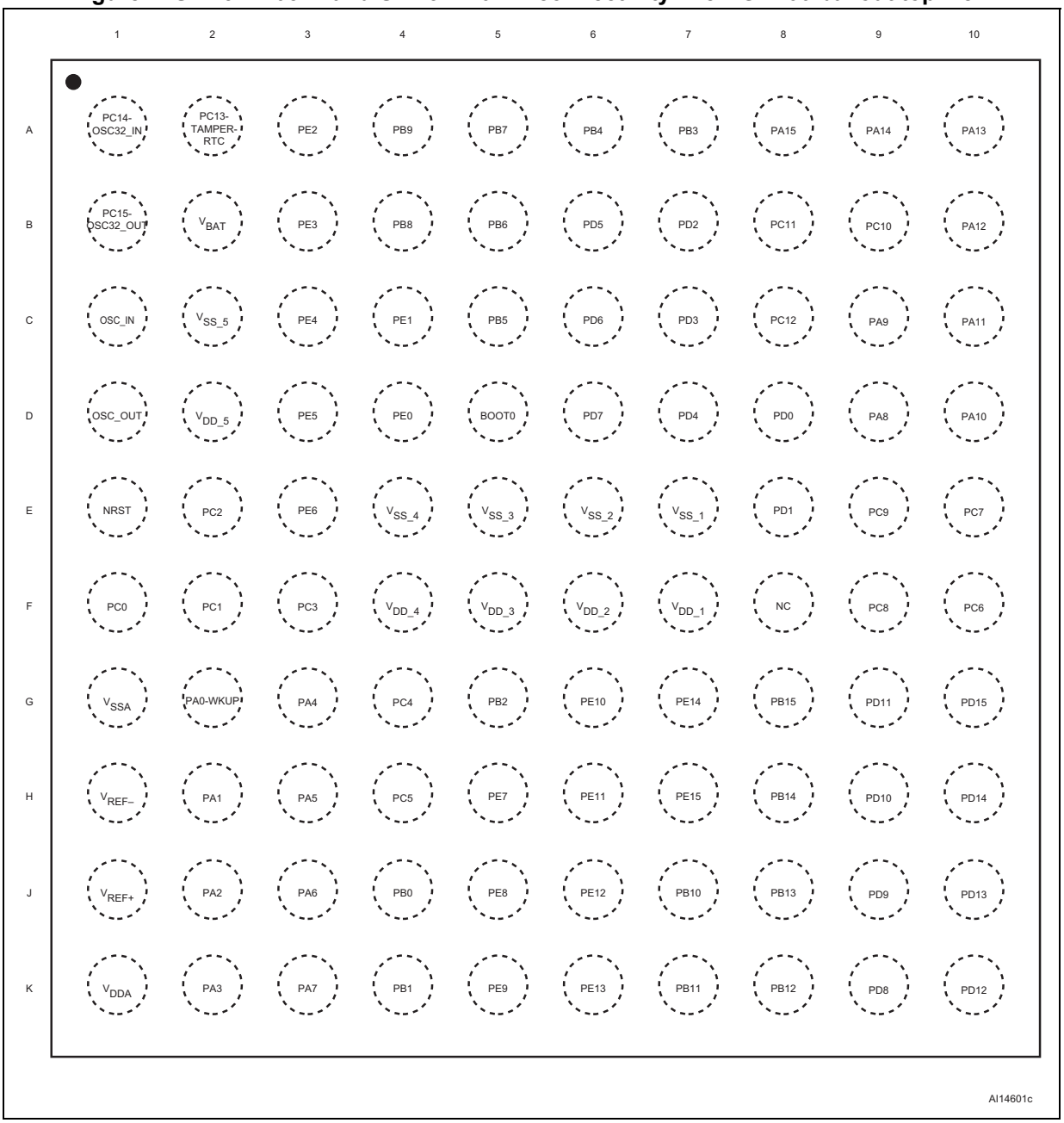
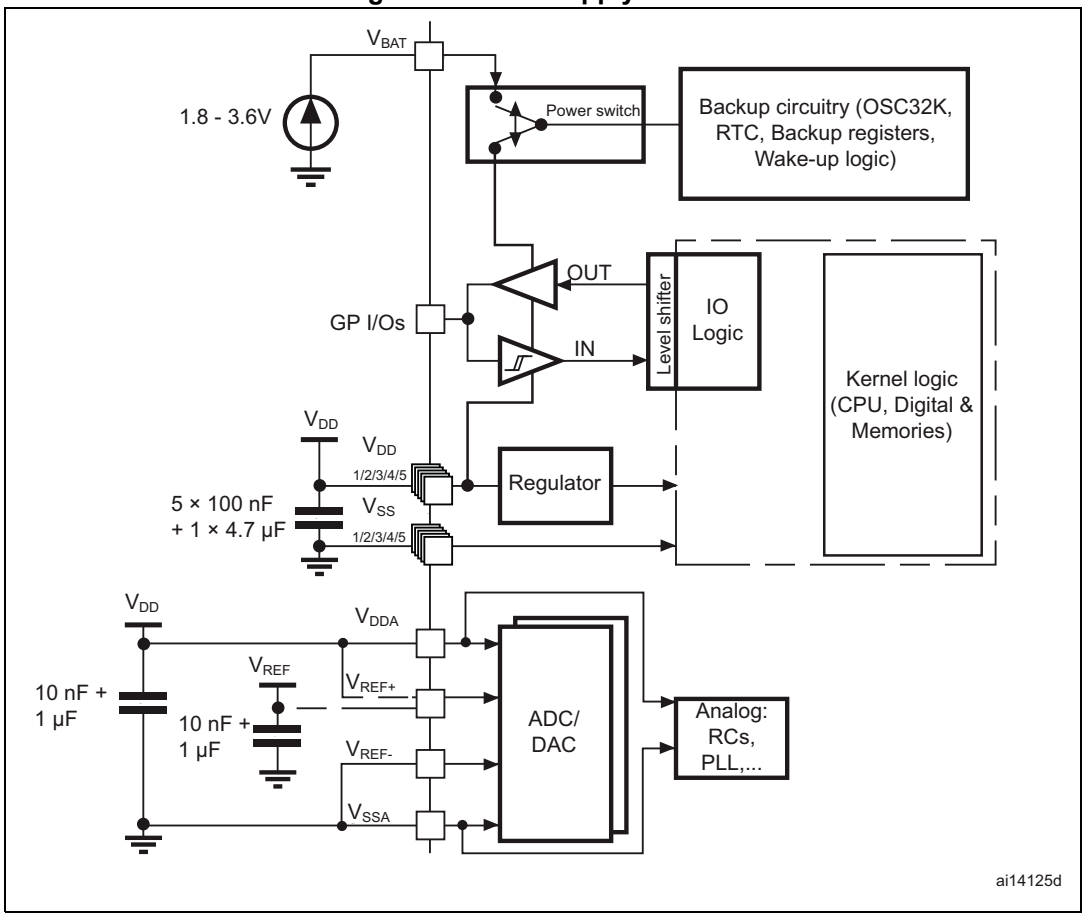


Table 5. Pin definitions

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
BGA100	LQFP64	LQFP100					Default	Remap
A3	-	1	PE2	I/O	FT	PE2	TRACECK	-
B3	-	2	PE3	I/O	FT	PE3	TRACED0	-
C3	-	3	PE4	I/O	FT	PE4	TRACED1	-
D3	-	4	PE5	I/O	FT	PE5	TRACED2	-
E3	-	5	PE6	I/O	FT	PE6	TRACED3	-
B2	1	6	V_{BAT}	S	-	V_{BAT}	-	-
A2	2	7	PC13-TAMPER-RTC(5)	I/O	-	PC13(6)	TAMPER-RTC	-
A1	3	8	PC14-OSC32_IN(5)	I/O	-	PC14(6)	OSC32_IN	-
B1	4	9	PC15-OSC32_OUT(5)	I/O	-	PC15(6)	OSC32_OUT	-
C2	-	10	V_{SS_5}	S	-	V_{SS_5}	-	-
D2	-	11	V_{DD_5}	S	-	V_{DD_5}	-	-
C1	5	12	OSC_IN	I	-	OSC_IN	-	-
D1	6	13	OSC_OUT	O	-	OSC_OUT	-	-
E1	7	14	NRST	I/O	-	NRST	-	-
F1	8	15	PC0	I/O	-	PC0	ADC12_IN10	-
F2	9	16	PC1	I/O	-	PC1	ADC12_IN11/ ETH_MII_MDC/ ETH_RMII_MDC	-
E2	10	17	PC2	I/O	-	PC2	ADC12_IN12/ ETH_MII_TXD2	-
F3	11	18	PC3	I/O	-	PC3	ADC12_IN13/ ETH_MII_TX_CLK	-
G1	12	19	V_{SSA}	S	-	V_{SSA}	-	-
H1	-	20	V_{REF-}	S	-	V_{REF-}	-	-
J1	-	21	V_{REF+}	S	-	V_{REF+}	-	-
K1	13	22	V_{DDA}	S	-	V_{DDA}	-	-
G2	14	23	PA0-WKUP	I/O	-	PA0	WKUP/USART2_CTS(7) ADC12_IN0/TIM2_CH1_ETR TIM5_CH1/ ETH_MII_CRS_WKUP	-

5.1.6 Power supply scheme

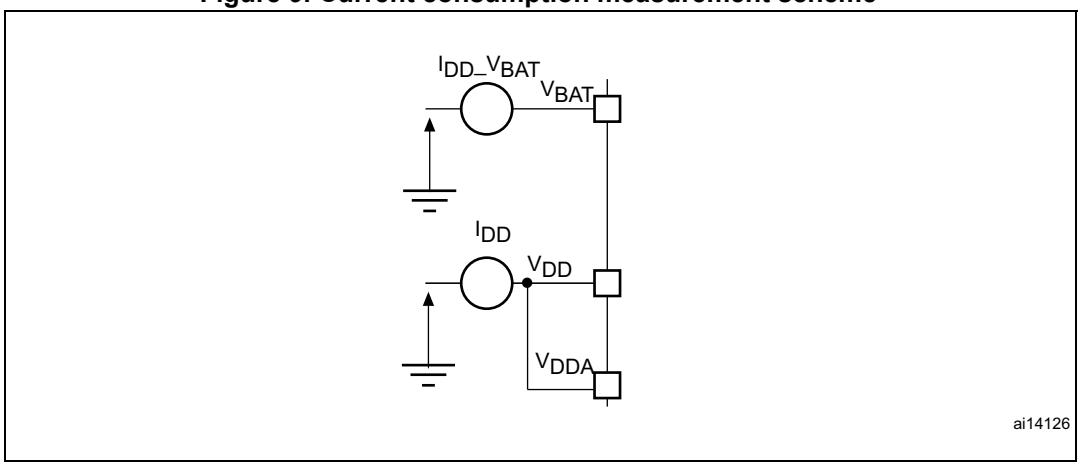
Figure 8. Power supply scheme



Caution: In *Figure 8*, the 4.7 µF capacitor must be connected to V_{DD3}.

5.1.7 Current consumption measurement

Figure 9. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 6: Voltage characteristics*, *Table 7: Current characteristics*, and *Table 8: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five volt tolerant pin	V_{SS} –0.3	V_{DD} +4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.11: Absolute maximum ratings (electrical sensitivity)*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 7: Current characteristics* for the maximum allowed injected current values.

Table 7. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	–25	
$I_{INJ(PIN)}$(2)	Injected current on five volt tolerant pins(3)	-5/+0	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device. See *Note: on page 76*.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 6: Voltage characteristics* for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 6: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

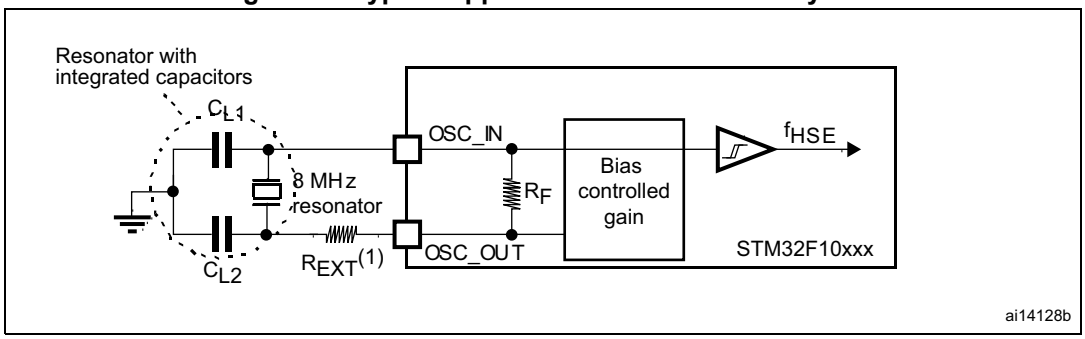
Table 17. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Run mode	External clock(3)	72 MHz	47.3	28.3	mA
			48 MHz	32	19.6	
			36 MHz	24.6	15.4	
			24 MHz	16.8	10.6	
			16 MHz	11.8	7.4	
			8 MHz	5.9	3.7	
			4 MHz	3.7	2.9	
			2 MHz	2.5	2	
			1 MHz	1.8	1.53	
			500 kHz	1.5	1.3	
			125 kHz	1.3	1.2	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	36 MHz	23.9	14.8	mA
			24 MHz	16.1	9.7	
			16 MHz	11.1	6.7	
			8 MHz	5.6	3.8	
			4 MHz	3.1	2.1	
			2 MHz	1.8	1.3	
			1 MHz	1.16	0.9	
			500 kHz	0.8	0.67	
			125 kHz	0.6	0.5	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 16*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Figure 16. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 23*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 23. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	5	-	MΩ
$C^{(2)}$	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 kΩ	-	-	15	pF
I_2	LSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS}	-	-	1.4	µA
g_m	Oscillator Transconductance	-	5	-	-	µA/V

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 22* and *Table 38*, respectively.

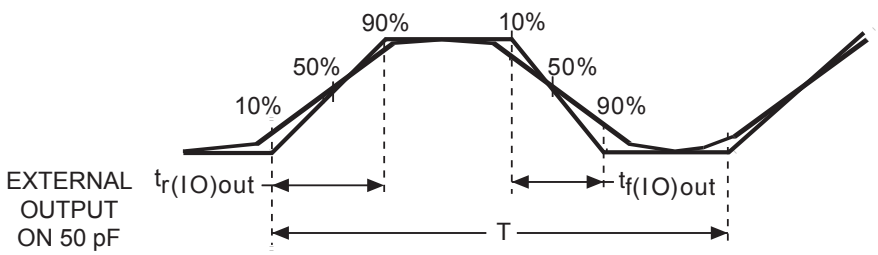
Unless otherwise specified, the parameters given in *Table 38* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 38. I/O AC characteristics(1)

MODEx[1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25(3)	
11	$F_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 22*.
3. Guaranteed by design, not tested in production.

Figure 22. I/O AC characteristics definition



Maximum frequency is achieved if (t_r + t_f) < (2/3)T and if the duty cycle is (45-55%) when loaded by 50 pF

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5.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 36*).

Unless otherwise specified, the parameters given in *Table 39* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 39. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	–0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	V_{DD} > 2.7 V	300	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

5.3.16 Communications interfaces

I^2C interface characteristics

Unless otherwise specified, the parameters given in *Table 41* are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

The STM32F105xx and STM32F107xx I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I^2C characteristics are described in *Table 41*. Refer also to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 41. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(3)	-	0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	20 + 0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I^2C frequencies. It must be at least 4 MHz to achieve the fast mode I^2C frequencies and it must be a mulitple of 10 MHz in order to reach I^2C fast mode maximum clock 400 kHz.
3. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

USB OTG FS characteristics

The USB OTG interface is USB-IF certified (Full-Speed).

Table 45. USB OTG FS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB OTG FS transceiver startup time	1	µs

1. Guaranteed by design, not tested in production.

Table 46. USB OTG FS DC electrical characteristics

Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input levels	V_{DD}	USB OTG FS operating voltage	-	3.0(2)	-	3.6	V
	V_{DI}(3)	Differential input sensitivity	I(USBDP, USBDM)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold	-	1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)		-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PD}		Pull-down resistance on PA11, PA12	$V_{IN} = V_{DD}$	17	21	24	kΩ
		Pull-down resistance on PA9		0.65	1.1	2.0	
R_{PU}		Pull-up resistance on PA12	$V_{IN} = V_{SS}$	1.5	1.8	2.1	
		Pull-up resistance on PA9	$V_{IN} = V_{SS}$	0.25	0.37	0.55	

1. All the voltages are measured from the local ground potential.
2. The STM32F105xx and STM32F107xx USB OTG FS functionality is ensured down to 2.7 V but not the full USB OTG FS electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design, not tested in production.
4. R_L is the load connected on the USB OTG FS drivers

Figure 30. USB OTG FS timings: definition of data signal rise and fall time

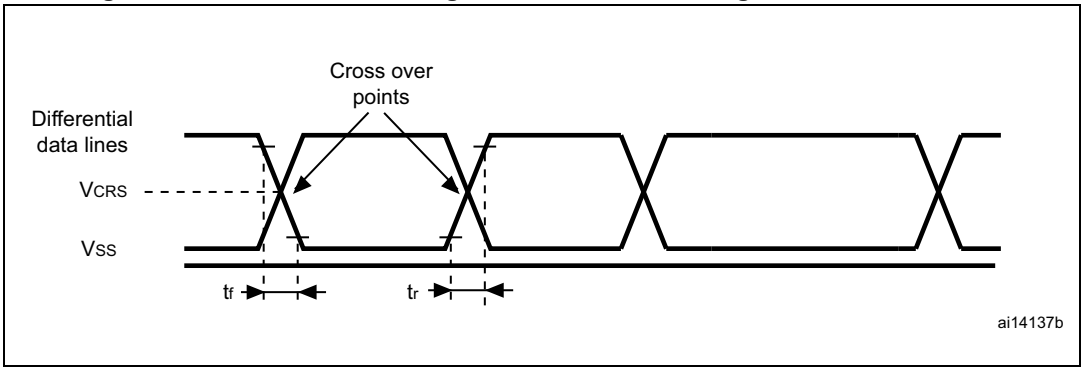


Table 47. USB OTG FS electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, refer to USB Specification - Chapter 7 (version 2.0).

Ethernet characteristics

Table 48 showns the Ethernet operating voltage.

Table 48. Ethernet DC electrical characteristics

Symbol		Parameter	Min.(1)	Max.(1)	Unit
Input level	V_{DD}	Ethernet operating voltage	3.0	3.6	V

1. All the voltages are measured from the local ground potential.

Table 49 gives the list of Ethernet MAC signals for the SMI (station management interface) and *Figure 31* shows the corresponding timing diagram.

Figure 31. Ethernet SMI timing diagram

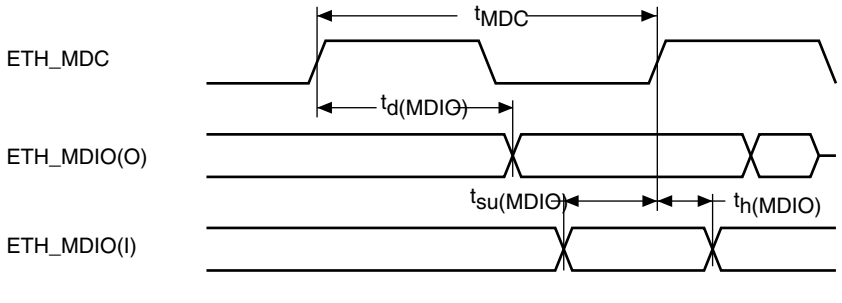


Table 49. Dynamic characteristics: Ethernet MAC signals for SMI

Symbol	Rating	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time (1.71 MHz, AHB = 72 MHz)	583	583.5	584	ns
$t_{d(MDIO)}$	MDIO write data valid time	13.5	14.5	15.5	ns
$t_{su(MDIO)}$	Read data setup time	35	-	-	ns
$t_{h(MDIO)}$	Read data hold time	0	-	-	ns

Table 52. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 52*.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 53. R_{AIN} max for f_{ADC} = 14 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

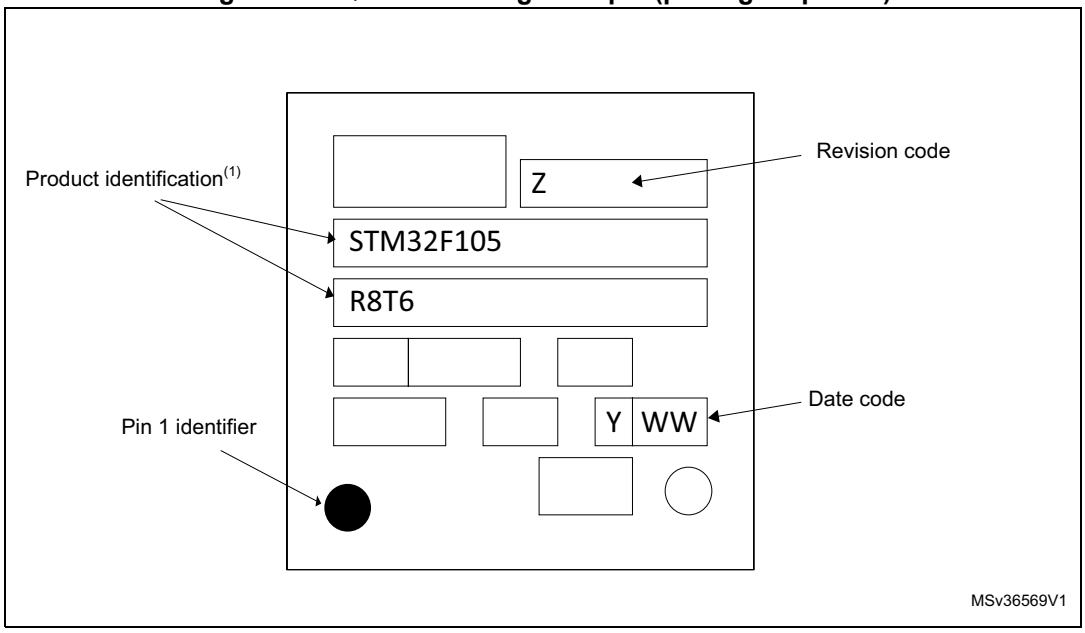
1. Based on characterization, not tested in production.

Device marking for LQFP64

The following figure shows the device marking for the LQFP64 package.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 48.LQFP64 marking example (package top view)

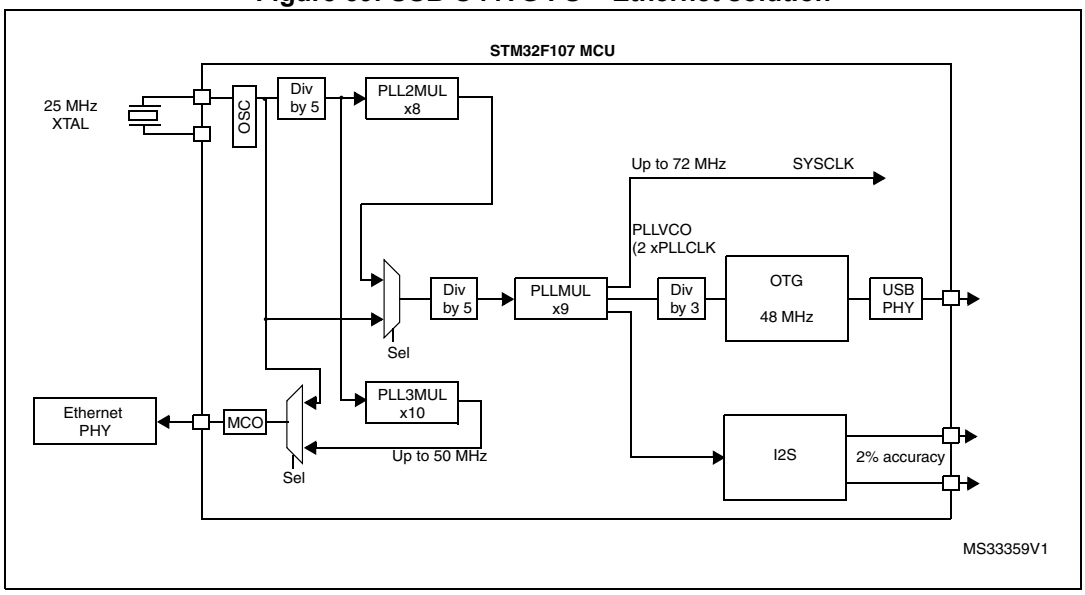


1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

A.4 USB OTG FS interface + Ethernet/I²S interface solutions

With the clock tree implemented on the STM32F107xx, only one crystal is required to work with both the USB (host/device/OTG) and the Ethernet (MII/RMII) interfaces. *Figure 59* illustrate the solution.

Figure 59. USB O44TG FS + Ethernet solution



With the clock tree implem1ented on the STM32F107xx, only one crystal is required to work with both the USB (host/device/OTG) and the I²S (Audio) interfaces. *Figure 60* illustrate the solution.

Figure 60. USB OTG FS + I²S (Audio) solution

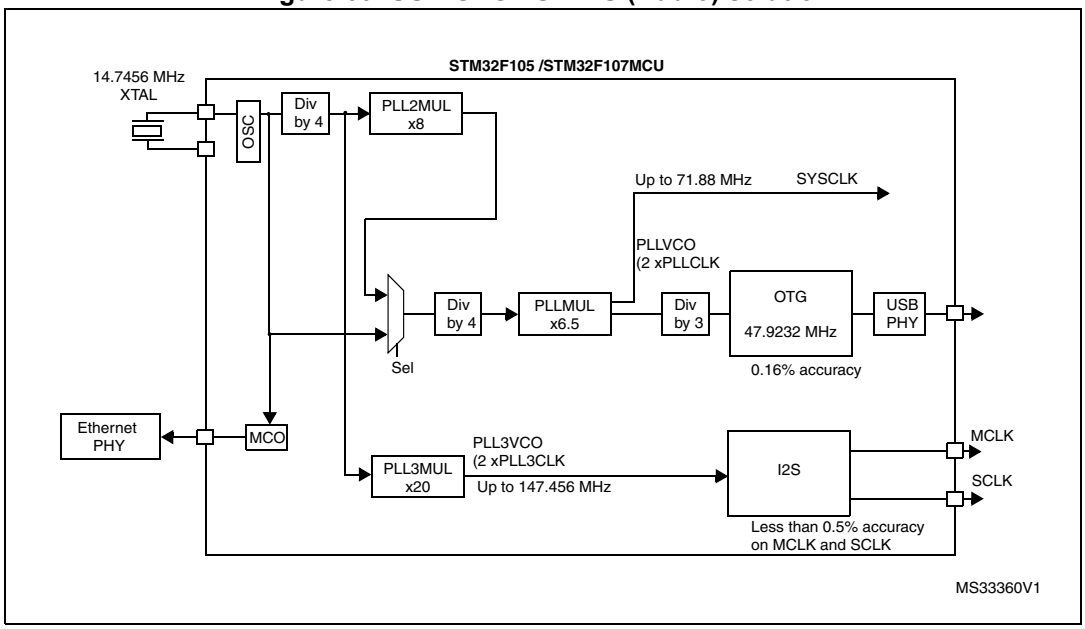


Table 64. Applicative current consumption in Run mode, code with data processing running from Flash

Symbol	parameter	Conditions[1]	Typ[2]	Max[2]		Unit
				85 °C	105 °C	
I_{DD}	Supply current in run mode	External clock, all peripherals enabled except ethernet, HSE = 8 MHz, f_{HCLK} = 72 MHz, no MCO	57	63	64	mA
		External clock, all peripherals enabled except ethernet, HSE = 14.74 MHz, f_{HCLK} = 72 MHz, no MCO	60.5	67	68	
		External clock, all peripherals enabled except OTG, HSE = 25 MHz, f_{HCLK} = 72 MHz, MCO = 25 MHz	53	60.7	61	
		External clock, all peripherals enabled, HSE = 25 MHz, f_{HCLK} = 72 MHz, MCO = 25 MHz	60.5	65.5	66	
		External clock, all peripherals enabled, HSE = 25 MHz, f_{HCLK} = 72 MHz, MCO = 50 MHz	64	69.7	70	
		External clock, all peripherals enabled, HSE = 50 MHz[3], f_{HCLK} = 72 MHz, no MCO	62.5	67.5	68	
		External clock, only OTG enabled, HSE = 8 MHz, f_{HCLK} = 48 MHz, no MCO	26.7	None	None	
		External clock, only ethernet enabled, HSE = 25 MHz, f_{HCLK} = 25 MHz, MCO = 25 MHz	14.3	None	None	

1. V_{DD} = 3.3 V.
2. Based on characterization, not tested in production.
3. External oscillator.