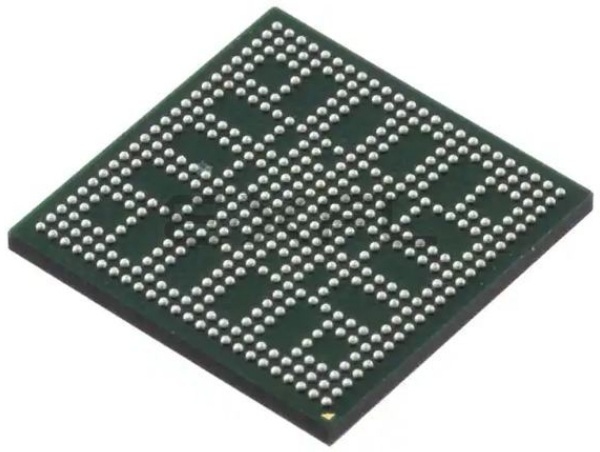

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (3)
Voltage - I/O	1.2V, 1.8V, 3.0V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	432-TFBGA
Supplier Device Package	432-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6l2dvn10ab

1.1 Ordering Information

Table 1 shows the orderable part numbers covered by this datasheet. Table 1 does not include all possible orderable part numbers. The latest part numbers are available on freescale.com/imx6series. If your desired part number is not listed in Table 1, or you have questions about available parts, see freescale.com/imx6series or contact your Freescale representative.

Table 1. Orderable Part Numbers

Part Number[1]	Mask Set	Options	Speed Grade	Temperature (Tj)	Package[2]
MCIMX6L8DVN10AA	N20G	With GPU, E-ink	1 GHz	0 to +95C	13x13mm, 0.5mm pitch BGA
MCIMX6L7DVN10SA	N20G	With Sipix	1 GHz	0 to +95C	13x13mm, 0.5mm pitch BGA
MCIMX6L3EVN10AA	N20G	With GPU	1 GHz	-40 to +105C	13x13mm, 0.5mm pitch BGA
MCIMX6L2EVN10AA	N20G		1 GHz	-40 to +105C	13x13mm, 0.5mm pitch BGA

1 Part numbers with a PC prefix indicate non-production engineering parts.

2 Case 2240 is RoHS compliant, lead-free MSL (moisture sensitivity level) 3.

Figure 1 describes the part number nomenclature so that users can identify the characteristics of the specific part number they have (for example, Cores, Frequency, Temperature Grade, Fuse options, Silicon revision).

Ensure that you have the right datasheet for your specific part by checking the Temperature Grade (Junction) field and matching it to the right datasheet. If you have questions, see freescale.com/imx6series or contact your Freescale representative.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6SoloLite processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6SoloLite processor system.

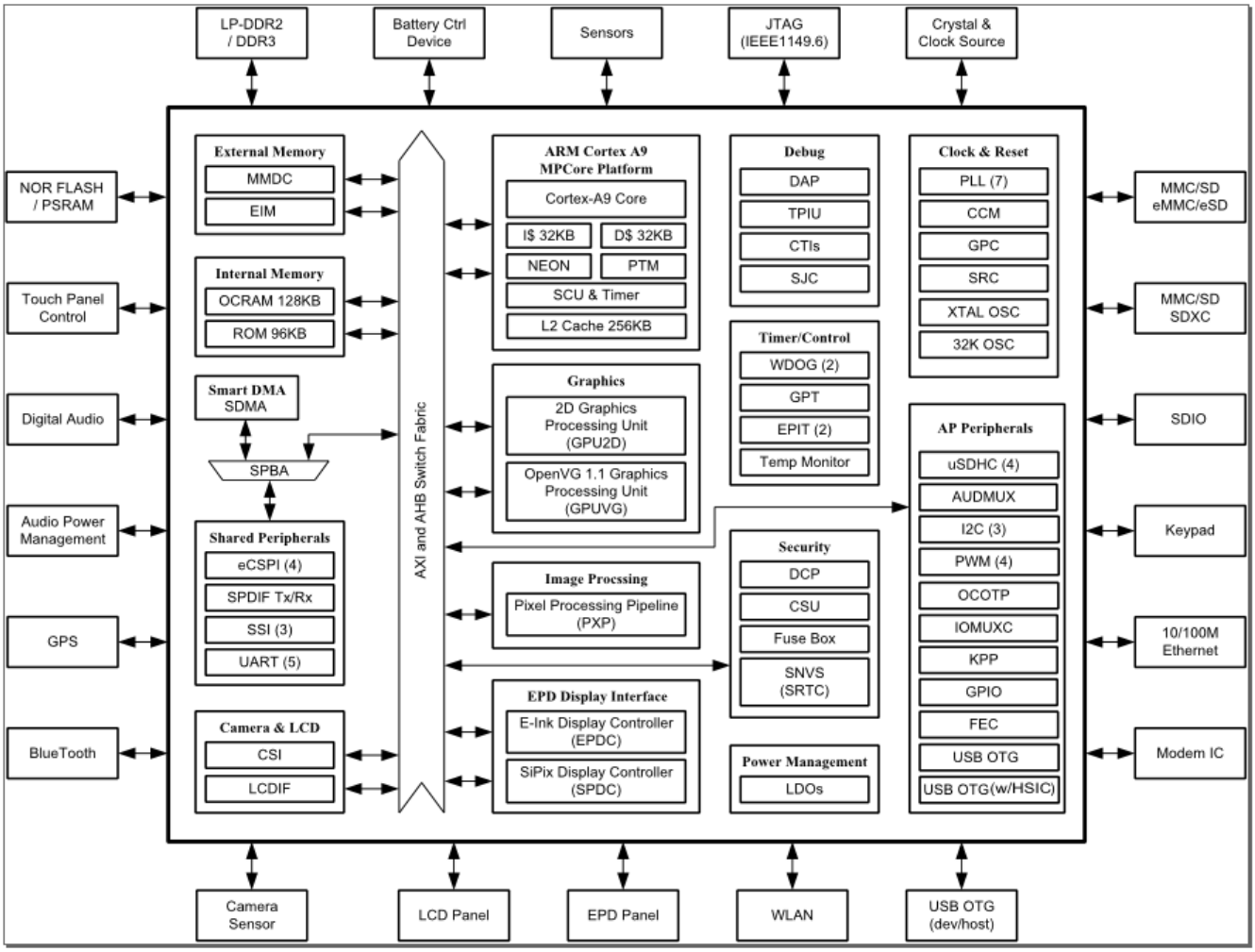

Figure 2. i.MX 6SoloLite System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (4) indicates four separate PWM peripherals.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SPDC	Electrophoretic Display Controller	Peripherals	The SPDC is a feature-rich, low power, and high-performance direct-drive, active matrix EPD controller. It is specifically designed to drive SiPix™ EPD panels, supporting a wide variety of TFT backplanes.
SPDIF	Sony Phillips Digital Interface	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface, which is used on the AP to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options. The SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream that reduces CPU overhead in use cases where two time slots are being used simultaneously.
TEMPMON	Temperature Monitor	System Control Peripherals	The temperature monitor/sensor IP, for detecting high temperature conditions. The Temperature sensor IP for detecting die temperature. The temperature read out does not reflect case or ambient temperature, but the proximity of the temperature sensor location on the die. Temperature distribution may not be uniformly distributed, therefore the read out value may not be the reflection of the temperature value of the entire die.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 4 MHz. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard and the i.MX31 UART modules. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOH2A	2x USB 2.0 High Speed OTG and 1x HS Hosts	Connectivity Peripherals	USBO2H contains: • One Two high-speed OTG module with integrated HS USB PHY • One identical high-speed Host modules connected to HSIC USB ports.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC-1 uSDHC-2 uSDHC-2 uSDHC-4	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6SoloLite specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.2/4.3/4.4 including high-capacity (size > 2 GB) cards HC MMC. HW reset as specified for eMMC cards is supported at ports #3 and #4 only. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v1.10 • Fully compliant with SD Card Specification, Part A2, SD Host Controller Standard Specification, v2.00 All four ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) However, the SoC level integration and I/O muxing logic restrict the functionality to the following: • Instances #1 and #2 are primarily intended to serve as external slots or interfaces to on-board SDIO devices. These ports are equipped with “Card detection” and “Write Protection” pads and do not support HW reset • All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for Ports #1 and #2 in four bit configuration (SD interface). Port #3 is placed in his own independent power domain and port #4 shares power domain with some other interfaces.
WDOG-1	Watchdog	Timer Peripherals	The Watchdog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG-2 (TZ)	Watchdog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system’s security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode Software.
XTALOSC	Crystal Oscillator I/F	Clocking	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator.

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
ONOFF	In normal mode may be connected to ON/OFF button (De-bouncing provided at this input). Internally this pad is pulled up. Short connection to GND in OFF mode causes internal power management state machine to change state to ON. In ON mode short connection to GND generates interrupt (intended to Software controllable power down). Long above ~5s connection to GND causes “forced” OFF.
POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low)
RTC_XTALI/RTC_XTALO	If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal (≤100 kΩ ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI the RTC_XTALO pin should be left floating or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level and the frequency should be <100 kHz under typical conditions. In case when high accuracy real time clock are not required system may use internal low frequency ring oscillator. It is recommended to connect RTC_XTALI to GND and keep RTC_XTALO floating.
TEST_MODE	TEST_MODE is for Freescale factory use. This signal is internally connected to an on-chip pull-down device. The user must either float this signal or tie it to GND.
XTALI/XTALO	A 24.0 MHz crystal should be connected between XTALI and XTALO. level and the frequency should be <32 MHz under typical conditions. The crystal must be rated for a maximum drive level of 250 μW. An ESR (equivalent series resistance) of typically 80 Ω is recommended. Freescale BSP (board support package) software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALI must be directly driven by the external oscillator and XTALO is floated. The XTALI signal level must swing from ~0.8 x NVCC_PLL_OUT to ~0.2 V. This clock is used as a reference for USB, PCIe, and SATA, so there are strict frequency tolerance and jitter requirements. See the XTALOSC chapter and relevant interface specifications chapters of the i.MX 6SoloLite reference manual, for details.
ZQPAD	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND.

Table 4. JTAG Controller Interface Summary

JTAG	I/O Type	On-Chip Termination
JTAG_TCK	Input	47 kΩ pull-up
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	3-state output	Keeper

Table 11. Maximal Supply Currents (continued)

Power Line	Conditions	Max Current	Unit
USB_OTG1_VBUS USB_OTG2_VBUS	—	25[3]	mA
Primary Interface (IO) Supplies			
NVCC_DRAM	—	—[4]	
NVCC33_IO	N=156	Use maximal IO Equation[5]	
NVCC18_IO	N=156	Use maximal IO Equation[5]	
MISC			
DRAM_VREF	—	1	mA

1 The actual maximum current drawn from VDDHIGH_IN will be as shown plus any additional current drawn from the VDDHIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_DRAM_2P5 supplies).

2 The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA, if available. VDD_SNVS_CAP charge time will increase if less than 1 mA is available.

3 This is the maximum current per active USB physical interface.

4 The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take in account factors, such as signal termination.
See the i.MX 6SoloLite Power Consumption Measurement Application Note or examples of DRAM power consumption during specific use case scenarios.

5 General equation for estimated, maximal power consumption of an IO power supply:

Imax = N x C x V x (0.5 x F)

Where:

N—Number of IO pins supplied by the power line

C—Equivalent external capacitive load

V—IO voltage

(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)

In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

4.1.6 Low Power Mode Supply Currents

Table 12 shows the current core consumption (not including I/O) of i.MX 6SoloLite processor in selected low power modes.

Table 12. Stop Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical[1]	Unit
WAIT	• ARM, SoC, and PU LDOs are set to 1.225 V • HIGH LDO set to 2.5 V • Clocks are gated • DDR is in self refresh • PLLs are active in bypass (24 MHz) • Supply voltages remain ON	VDD_ARM_IN (1.375 V)	4	mA
		VDD_SOC_IN (1.375 V)	7.5	
		VDD_PU_IN (1.375 V)	1.5	
		VDD_HIGH_IN(3.0 V)	9	
		Total	44.9	mW

Table 21. DVGPIO I/O DC Parameters (continued)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Sink current in Open Drain mode	Iskod	—	—	7	mA
Sink/source current in Push-Pull mode	Isspp	—	—	7	mA

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 DSE is the Drive Strength Field setting in the associated IOMUX control register.

3 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

4 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.6.2 Single Volatge General Purpose I/O (GPIO) DC Parameters

Table 22 shows DC parameters for GPIO pads. The parameters in Table 22 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

Table 22. GPIO I/O DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage[1]	Voh	Ioh = -0.1 mA (DSE[2] = 001, 010) Ioh = -1 mA (DSE = 011, 100, 101, 110, 111)	OVDD – 0.15	—	V
Low-level output voltage[1]	Vol	Iol = 0.1 mA (DSE[2] = 001, 010) Iol = 1mA (DSE = 011, 100, 101, 110, 111)	—	0.15	V
High-Level DC input voltage[1, 3]	Vih	—	0.7 × OVDD	OVDD	V
Low-Level DC input voltage[1, 3]	Vil	—	0	0.3 × OVDD	V
Input Hysteresis	Vhys	OVDD = 3.3 V	0.25	—	V
Schmitt trigger VT+[3, 4]	VT+	—	0.5 × OVDD	—	V
Schmitt trigger VT–[3, 4]	VT–	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	Iin	Vin = OVDD or 0	-1.25	1.25	µA
Input current (22 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	212 1	µA
Input current (47 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	100 1	µA
Input current (100 kΩ pull-up)	Iin	Vin = 0 V Vin= OVDD	—	48 1	µA
Input current (100 kΩ pull-down)	Iin	Vin = 0 V Vin = OVDD	—	1 48	µA
Keeper circuit resistance	Rkeep	Vin = 0.3 x OVDD Vin = 0.7 x OVDD	105	205	kΩ

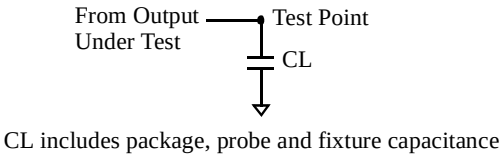

Figure 5. Load Circuit for Output

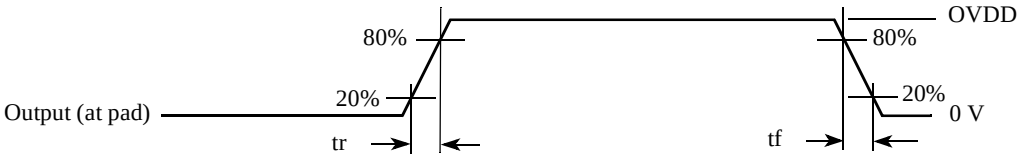

Figure 6. Output Transition Time Waveform

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 25 and Table 26, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 25. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 26. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.9.3.3 General EIM Timing-Synchronous Mode

Figure 10, Figure 11, and Table 37 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the BCLK rising edge according to corresponding assertion/negation control fields.

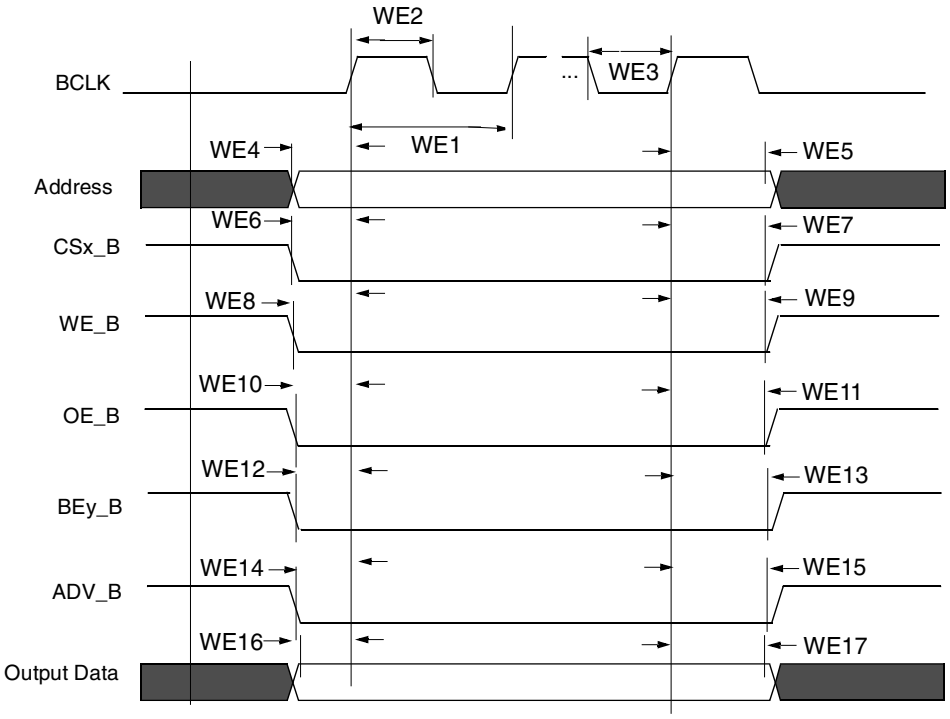

Figure 10. EIM Output Timing Diagram

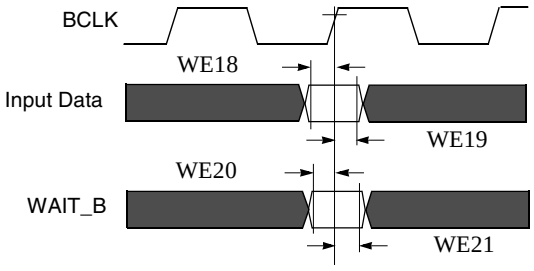

Figure 11. EIM Input Timing Diagram

4.9.3.4 Examples of EIM Synchronous Accesses

Table 37. EIM Bus Timing Parameters

ID	Parameter	Min[1]	Max[1]	Unit
WE1	BCLK cycle time[2]	t*(k+1)	—	ns
WE2	BCLK high level width	0.4*t*(k+1)	—	ns

4.9.3.5 General EIM Timing-Asynchronous Mode

Figure 16 through Figure 20, and Table 38 help you determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 16 through Figure 19 as RWSC, OEN & CSN is configured differently. See the i.MX 6SoloLite reference manual for the EIM programming model.

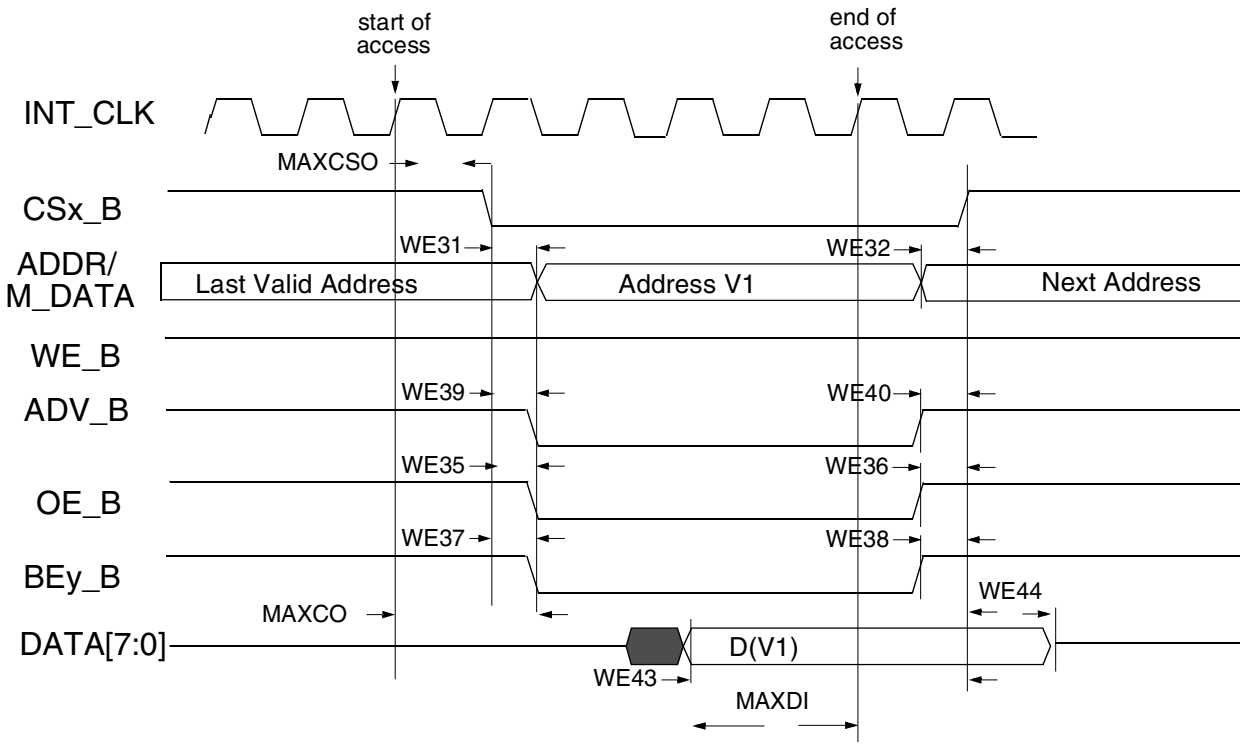

Figure 16. Asynchronous Memory Read Access (RWSC = 5)

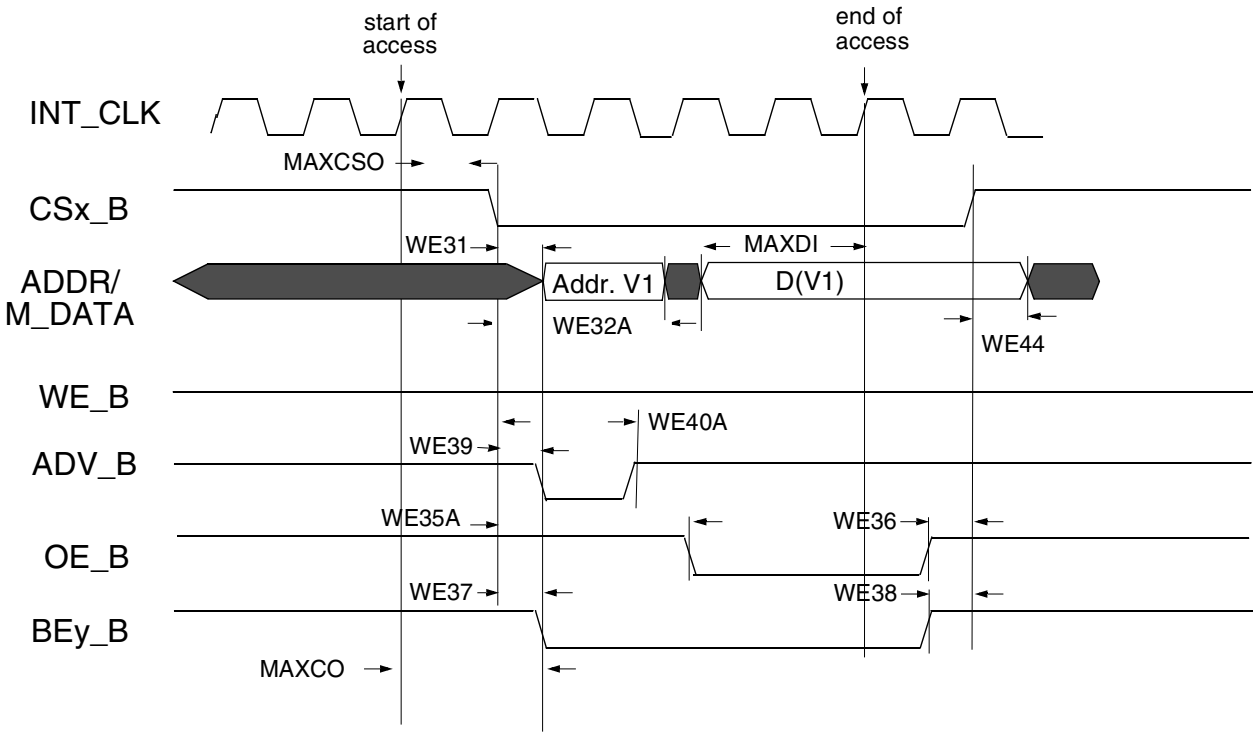

Figure 17. Asynchronous A/D Muxed Read Access (RWSC = 5)

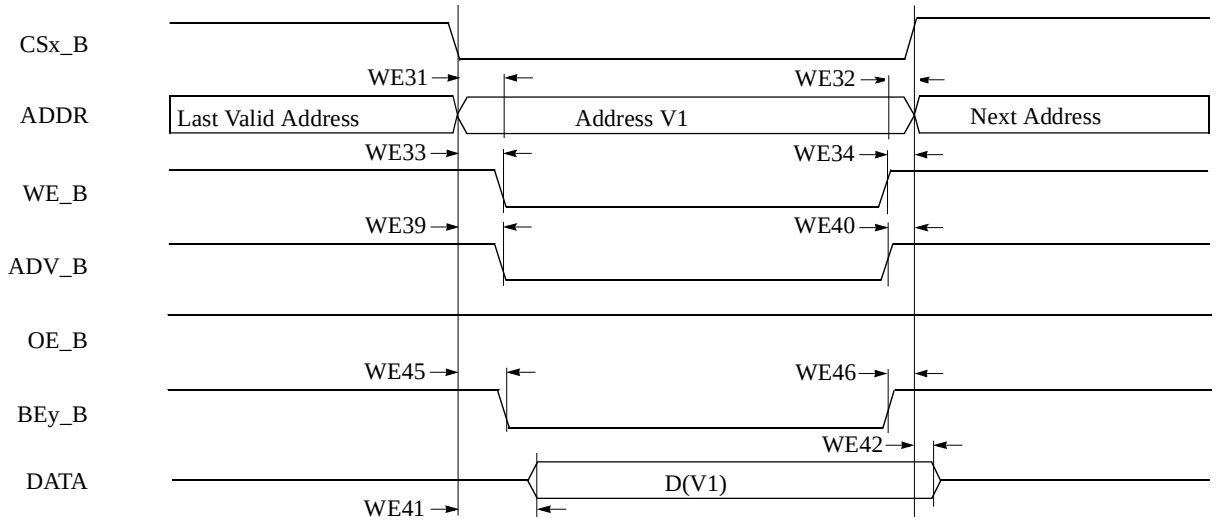

Figure 18. Asynchronous Memory Write Access

Figure 26 shows the LPDDR2 write timing diagram. The timing parameters for this diagram appear in Table 43.

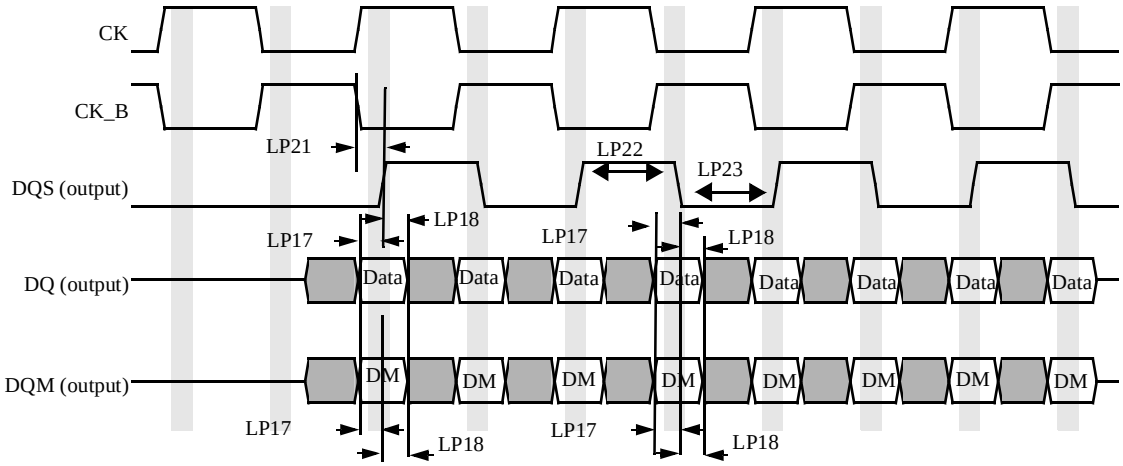

Figure 26. LPDDR2 Write Cycle

Table 43. LPDDR2 Write Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP17	DQ and DQM setup time to DQS (differential strobe)	t_{DS}	375	—	ps
LP18	DQ and DQM hold time to DQS (differential strobe)	t_{DH}	375	—	ps
LP21	DQS latching rising transitions to associated clock edges	t_{DQSS}	-0.25	+0.25	tCK
LP22	DQS high level width	t_{DQSH}	0.4	-	tCK
LP23	DQS low level width	t_{DQSL}	0.4	-	tCK

1 To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

2 All measurements are in reference to Vref level.

3 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

4.10.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4 (Dual Date Rate) timing.

4.10.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 33 depicts the timing of SD/eMMC4.3, and Table 49 lists the SD/eMMC4.3 timing characteristics.

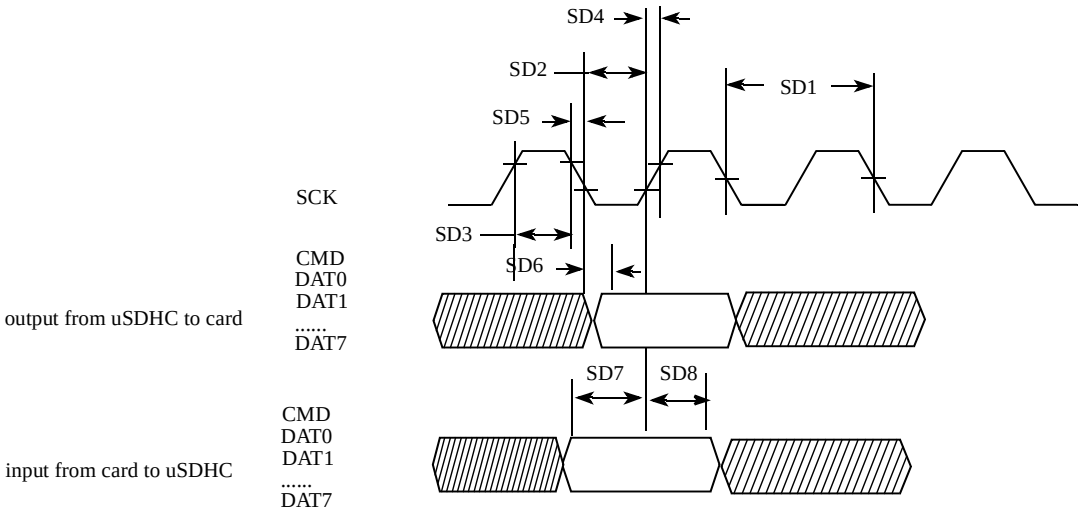

Figure 33. SD/eMMC4.3 Timing

Table 49. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
eSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	eSDHC Output Delay	t_{OD}	–6.6	3.6	ns
eSDHC Input/Card Outputs CMD, DAT (Reference to CLK)					

Figure 42 depicts the timing of the PWM, and Table 58 lists the PWM timing parameters.

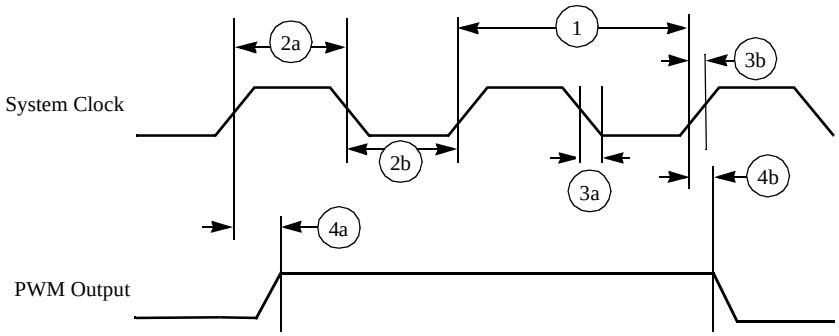

Figure 42. PWM Timing

Table 58. PWM Output Timing Parameters

Reference Number	Parameter	Min	Max	Unit
1	System CLK frequency[1]	0	ipg_clk	MHz
2a	Clock high time	12.29	—	ns
2b	Clock low time	9.91	—	ns

[1] CL of PWMO = 30 pF

4.10.8 SCAN JTAG Controller (SJC) Timing Parameters

Figure 43 depicts the SJC test clock input timing. Figure 44 depicts the SJC boundary scan timing. Figure 45 depicts the SJC test access port. Signal parameters are listed in Table 59.

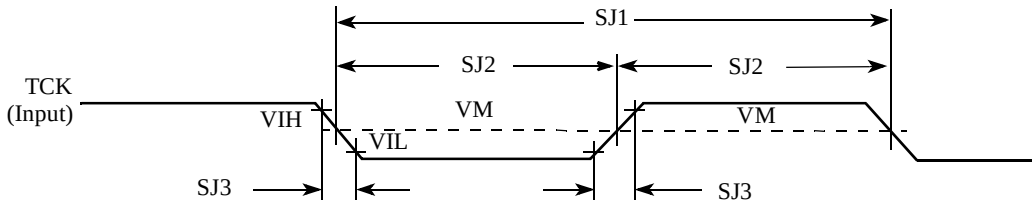

Figure 43. Test Clock Input Timing Diagram

4.10.10.2 SSI Receiver Timing with Internal Clock

Figure 50 depicts the SSI receiver internal clock timing and Table 63 lists the timing parameters for the receiver timing with the internal clock.

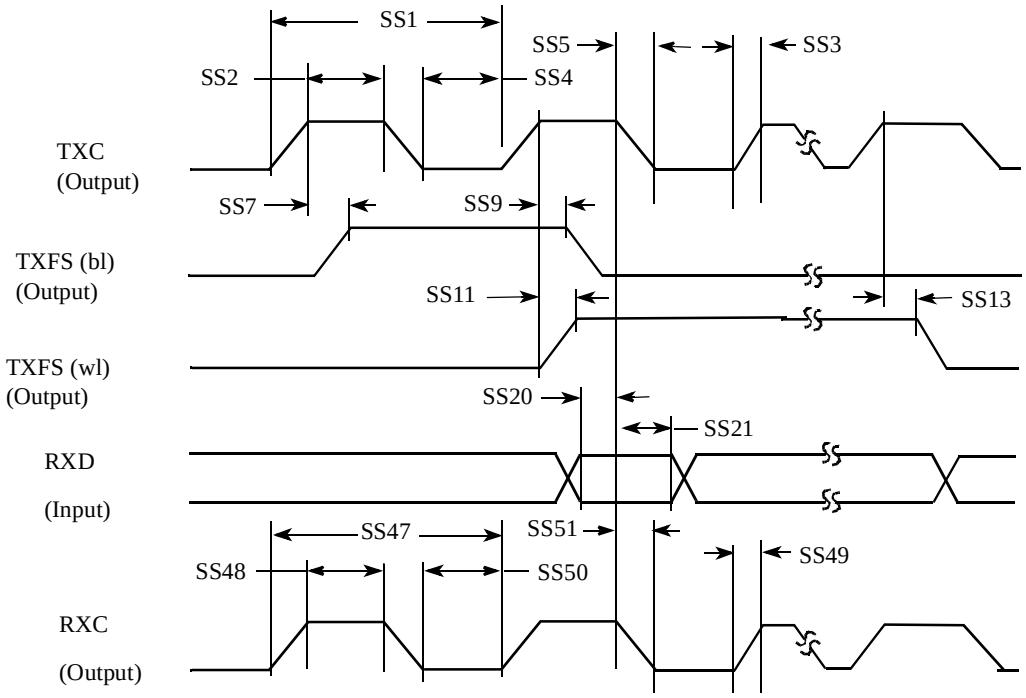

Figure 50. SSI Receiver Internal Clock Timing Diagram

Table 63. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	10.0	—	ns
SS21	SRXD hold time after (Rx) CK low	0.0	—	ns
Oversampling Clock Operation				

4.10.12 USB HSIC Timings

This section describes the electrical information of the USB HSIC port.

NOTE

HSIC is DDR signal, following timing spec is for both rising and falling edge.

4.10.12.1 Transmit Timing

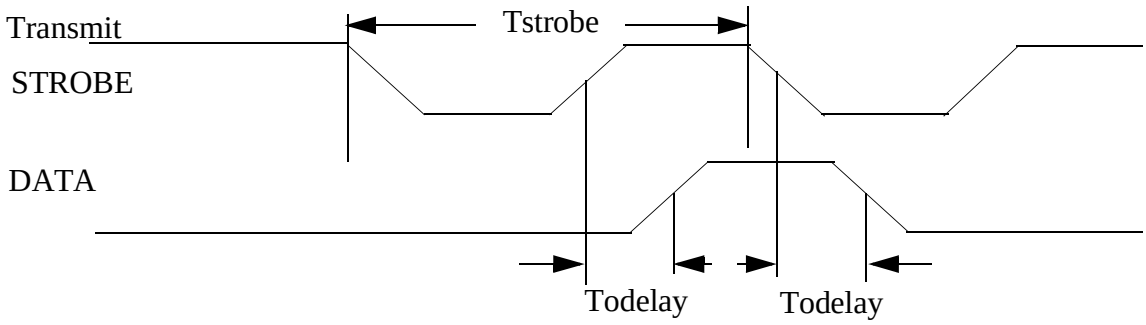

Figure 57. USB HSIC Transmit Waveform

Table 71. USB HSIC Transmit Parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	
Todelay	data output delay time	550	1350	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

4.10.12.2 Receive Timing

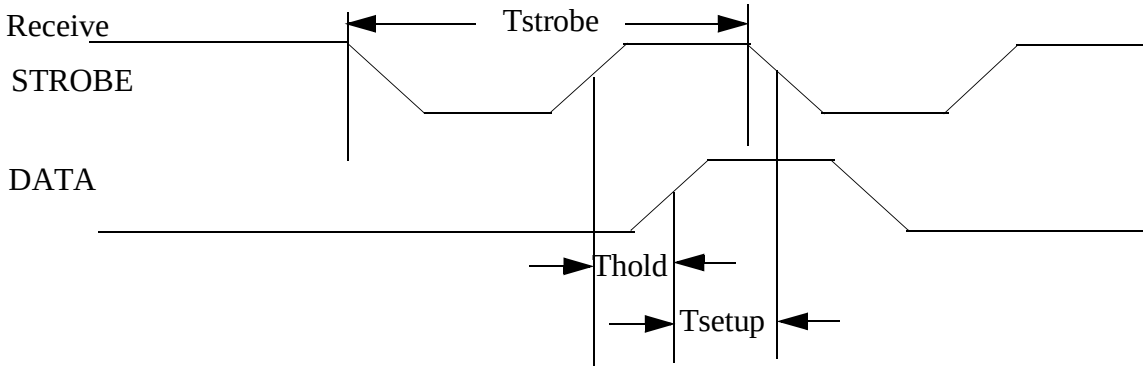

Figure 58. USB HSIC Receive Waveform

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 76 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6SoloLite Fuse Map document and the System Boot chapter of the i.MX 6SoloLite reference manual.

Table 76. Fuses and Associated Pins Used for Boot

Pin	Direction at Reset	eFuse Name	Details
BOOT_MODE1	Input	Boot Mode Selection	Boot Mode selection
BOOT_MODE0	Input	Boot Mode Selection	Boot Mode Selection

Table 79. 13 x 13 mm Supplies Contact Assignment (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
VDD_SNVS_CAP	AD20	Secondary Supply for the SNVS (internal regulator output—requires capacitor if internal regulator is used)
VDD_SNVS_IN	AC20	Primary Supply, for the SNVS Regulator
VDD_SOC_CAP	J7, J8, J9, K7, K8, K9, N18, P18, R18	Secondary Supply for the SoC and PU (internal regulator output—requires capacitor if internal regulator is used)
VDD_SOC_IN	J10, J11, K10, K11, R16, R17, T16, T17, T18	Primary Supply, for the SoC and PU Regulators
VDD_USB_CAP	U14	Secondary Supply for the 3V Domain (USBPHY, MLPBPHY, eFuse), internal regulator output, requires capacitor if internal regulator is used.
USB_OTG1_VBUS	AA18	
USB_OTG2_VBUS	AD18	
ZQPAD	AE17	
NC	C4, C5, C8, C9, C12, C13, C16, C17, C20, C21, D4, D5, D8, D9, D12, D13, D16, D17, D20, D21, E8, E9, E12, E13, E16, E17, F3, F4, F5, F6, F8, F9, F12, F13, F16, F17, F19, F20, F21, F22, G3, G4, G5, G6, G19, G20, G21, G22, H8, H9, H12, H13, H16, H17, K3, K4, K5, K6, K19, K20, K21, K22, L3, L4, L5, L6, L8, L17, L19, L20, L21, L22, P3, P4, P5, P6, P8, P17, P19, P20, P21, P22, R3, R4, R5, R6, R19, R20, R21, R22, U8, U9, U12, U13, U16, U17, V3, V4, V5, V6, V19, V20, V21, V22, W3, W4, W5, W6, W8, W9, W12, W13, W16, W17, W19, W20, W21, W22, Y8, Y9, Y12, Y13, Y16, Y17, AA4, AA5, AA8, AA9, AA12, AA13, AA16, AA17, AA20, AA21, AB4, AB5, AB8, AB9, AB12, AB13, AB16, AB17 AB20, AB21	No Connections.

Table 80 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 80. 13 x 13 mm Functional Contact Assignments

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
AUD_MCLK	H19	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[6]	Input	Keeper
AUD_RXC	J21	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[1]	Input	Keeper
AUD_RXD	J20	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[2]	Input	Keeper
AUD_RXFS	J19	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[0]	Input	Keeper

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
TAMPER	Y18	VDD_SNVS_IN	GPIO	ALT0	snvs_lp_wrapper_SNVS_TD1	Input	
TEST_MODE	U15	VDD_SNVS_IN	GPIO	ALT0	Reserved—Factory Use Only	Input	
UART1_RXD	B19	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[16]	Input	Keeper
UART1_TXD	D19	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[17]	Input	Keeper
USB_OTG_CHD_B	AC22	USB_OTG_VBUS	ANALOG		USB_OTG_CHD_B	—	—
USB_OTG1_DN	AD19	USB_OTG_VBUS	ANALOG		USB_OTG1_DN	—	—
USB_OTG1_DP	AC19	USB_OTG_VBUS	ANALOG		USB_OTG1_DP	—	—
USB_OTG2_DN	AD17	USB_OTG_VBUS	ANALOG		USB_OTG2_DN	—	—
USB_OTG2_DP	AC17	USB_OTG_VBUS	ANALOG		USB_OTG2_DP	—	—
WDOG_B	F18	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[18]	Input	Keeper
XTALI	AD21	NVCC_PLL	ANALOG		XTALI	—	—
XTALO	AC21	NVCC_PLL	ANALOG		XTALO	—	—
ZQPAD	H2	NVCC_DRAM	ZQPAD		ZQPAD	Input	Hi-Z

[1] The state immediately after reset and before ROM firmware or software has executed.

6.1.3 13 x 13 mm, 0.5 mm Pitch Ball Map

Table 81 shows the MAPBGA 13 x 13mm, 0.5 mm pitch ball map.

Table 81. 13 x 13 mm, 0.5 mm Pitch Ball Map

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD
24	GND	KEY_ROW7	KEY_ROW6	KEY_COL5	KEY_ROW2	KEY_ROW1	KEY_ROW0	LCD_RESET	LCD_ENABLE	LCD_DAT23	LCD_DAT21	LCD_DAT19	LCD_DAT16	LCD_DAT13	LCD_DAT11	LCD_DAT9	LCD_DAT7	LCD_DAT4	LCD_DAT2	LCD_DAT0	SD2_DAT4	SD2_CMD	SD2_CLK	GND
23	SD1_DAT1	SD1_DAT0	KEY_COL7	KEY_ROW5	KEY_COL2	KEY_COL1	KEY_COL0	LCD_HSYNC	LCD_VSYNC	LCD_DAT22	LCD_DAT20	LCD_DAT18	LCD_DAT15	LCD_DAT12	LCD_DAT10	LCD_DAT8	LCD_DAT6	LCD_DAT3	LCD_DAT1	SD2_RST	SD2_DAT3	SD2_DAT1	CLK1_P	CLK1_N