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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (3)
Voltage - I/O	1.2V, 1.8V, 3.0V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	432-TFBGA
Supplier Device Package	432-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx6l2evn10aa

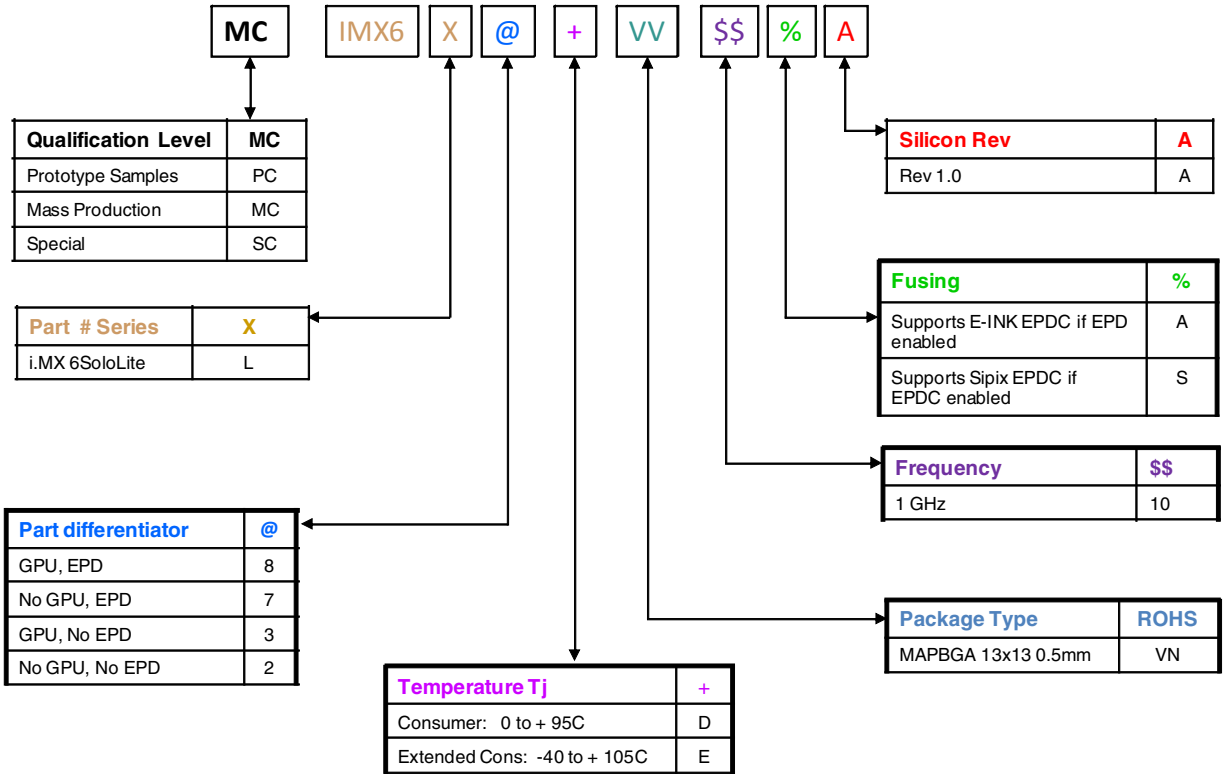


Figure 1. Part Number Nomenclature—i.MX 6SoloLite

Table 8. Package Thermal Resistance Data (continued)

Rating	Board	Symbol	No Lid	Unit
Junction to Ambient[1] (at 200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	40	°C/W
	Four layer board (2s2p)	$R_{\theta JMA}$	24	°C/W
Junction to Board[2]	—	$R_{\theta JB}$	14	°C/W
Junction to Case[3] (Top)	—	$R_{\theta JCtop}$	9	°C/W
Junction to Package Top[4]	Natural Convection	Ψ_{JT}	2	°C/W

1 Junction-to-Ambient Thermal Resistance was determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-Board Thermal Resistance was determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

3 Junction-to-Case at the top of the package was determined by using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1.7 USB PHY Current Consumption

4.1.7.1 Power Down Mode

In power down mode, everything is powered down, including the VBUS valid detectors, typ condition. Table 13 shows the USB interface current consumption in power down mode.

Table 13. USB PHY Current Consumption in Power Down Mode

	VDDUSB_CAP (3.0 V)	VDDHIGH_CAP (2.5 V)	NVCC_PLL_OUT (1.1 V)
Current	5.1 µA	1.7 µA	<0.5 µA

NOTE

The currents on the VDDHIGH_CAP and VDDUSB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

4.2.1 Power-Up Sequence

For power-up sequence, the restrictions are as follows:

- VDD_SNVS_IN supply must be turned ON before any other power supply. It may be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- If VDD_ARM_IN and VDD_SOC_IN are connected to different external supply sources, then VDD_ARM_IN supply must be turned ON together with VDD_SOC_IN supply or not delayed more than 1 ms.

NOTE

The POR_B input (if used) must be immediately asserted at power-up and remain asserted until the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the i.MX 6SoloLite reference manual for further details and to ensure that all necessary requirements are being met.

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

4.2.2 Power-Down Sequence

Table 14 shows the power down sequence orders. The two cases shown are, using the i.MX6 SoloLite internal supplies (non-bypass) and bypassing the internal LDO supplies.

Table 14. Power-Down Sequencing Order

Power Rail Name	Using all internal LDOs (non-bypass mode)	Internal LDOs Bypassed
VDD_SNVS_IN	7	9
VDD_HIGH_IN / NVCC33_IO	6	8
VDD_HIGH_CAP	6	7
NVCC18_IO	5	6
NVCC_PLL	6	5
NVCC_DRAM	4	4
VDD_ARM_IN	3	3
VDD_PU_IN	2	2
VDD_SOC_IN	1	1
USB_VBUS	N/A	N/A

NOTE

- VDD_ARM_IN, VDD_PU_IN, and VDD_SOC_IN can startup at the same. However, VDD_ARM_IN and VDD_PU_IN must be at their target values within 0.5 ms of VDD_SOC_IN.
- There are no special timing requirements for USB_VBUS.

4.2.3 Power Supplies Usage

- All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Group” column of Table 80, "13 x 13 mm Functional Contact Assignments," on page 101.

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the i.MX 6SoloLite reference manual for details on the power tree scheme recommended operation.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Digital Regulators (LDO_ARM, LDO_PU, LDO_SOC)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of their input supply ripple rejection and their on die trimming. This translates into more voltage for the die producing higher operating frequencies. These regulators have three basic modes.

- Bypass. The regulation FET is switched fully on passing the external voltage, DCDC_LOW, to the load unaltered. The analog part of the regulator is powered down in this state, removing any loss other than the IR drop through the power grid and FET.
- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

For additional information, see the i.MX 6SoloLite reference manual.

4.3.2 Analog Regulators

4.3.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDDHIGH_IN (see Table 9 for min and max input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. Since we are not testing the accuracy or the % regulation, and only testing with the LDO set to either 1.0V or 1.2V, this is the only range that is guaranteed. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 µF (2.2 µF should be considered the recommended minimum value), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For additional information, see the i.MX 6SoloLite reference manual.

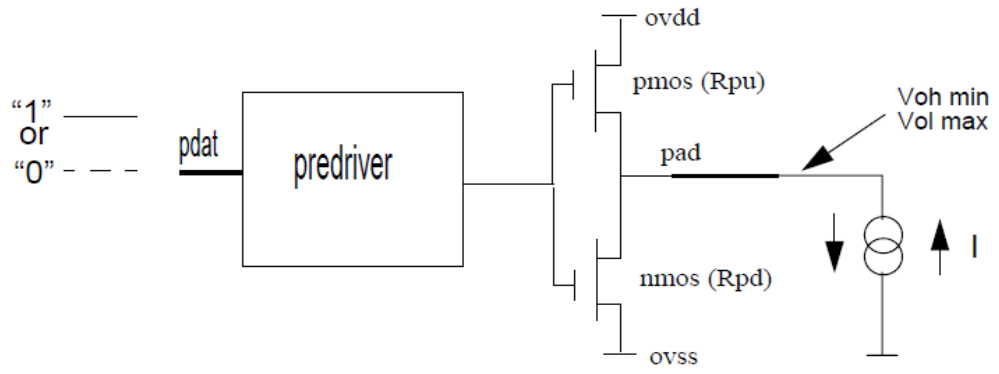


Figure 4. Circuit for Parameters Voh and Vol for I/O Cells

4.6.1 Dual Voltage General Purpose IO cell set (DVGPIO) DC parameters

Table 21 shows DC parameters for GPIO pads. The parameters in Table 22 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

Table 21. DVGPIO I/O DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage[1]	Voh	Ioh = -0.1 mA (DSE[2] = 001, 010) Ioh = -1 mA (DSE = 011, 100, 101, 110, 111)	OVDD – 0.15	—	V
Low-level output voltage[1]	Vol	Iol = 0.1 mA (DSE[2] = 001, 010) Iol = 1mA (DSE = 011, 100, 101, 110, 111)	—	0.15	V
High-Level DC input voltage[1, 3]	Vih	—	0.7 × OVDD	OVDD	V
Low-Level DC input voltage[1, 3]	Vil	—	0	0.3 × OVDD	V
Input Hysteresis	Vhys	OVDD = 1.8 V OVDD = 3.3 V	0.25	—	V
Schmitt trigger VT+[3, 4]	VT+	—	0.5 × OVDD	—	V
Schmitt trigger VT–[3, 4]	VT–	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	Iin	Vin = OVDD or 0	-1.25	1.25	µA
Input current (22 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	212 1	µA
Input current (47 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	100 1	µA
Input current (100 kΩ pull-up)	Iin	Vin = 0 V Vin= OVDD	—	48 1	µA
Input current (100 kΩ pull-down)	Iin	Vin = 0 V Vin = OVDD	—	1 48	µA
Keeper circuit resistance	Rkeep	Vin = 0.3 x OVDD Vin = 0.7 x OVDD	105	205	kΩ

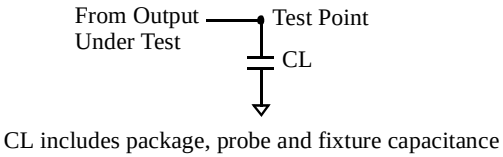


Figure 5. Load Circuit for Output

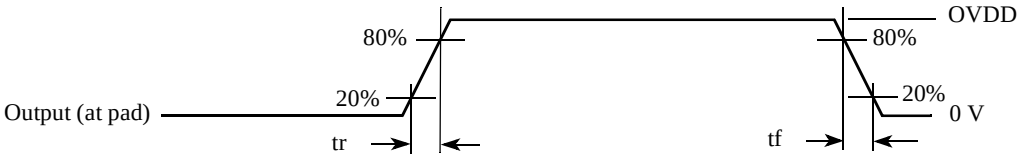
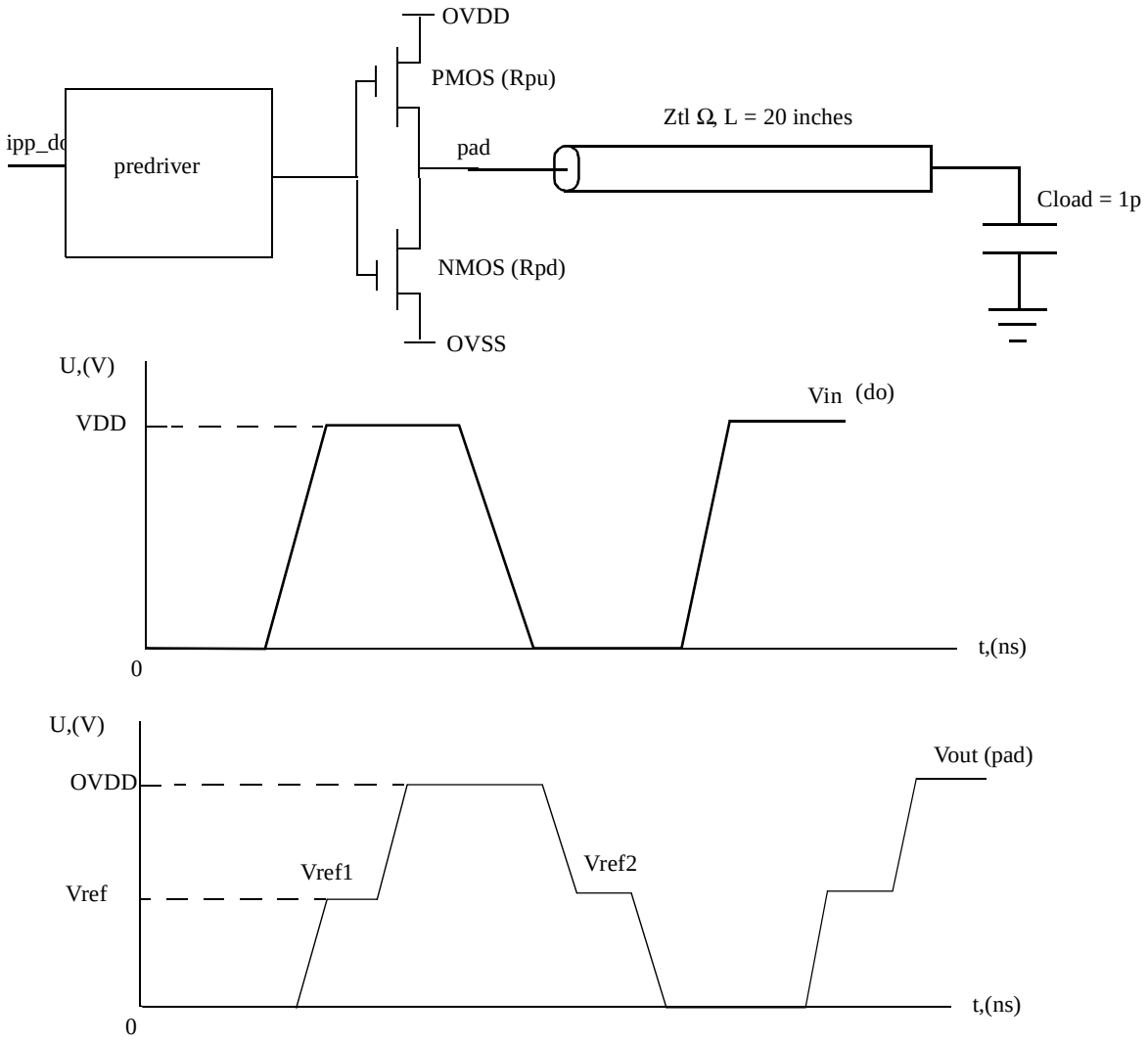


Figure 6. Output Transition Time Waveform



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 7. Impedance Matching Load for Measurement

4.8.1 Dual Voltage GPIO Output Buffer Impedance

Table 29 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 29. DVGPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	260 130 90 60 50 40 33	Ω

Table 30 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 30. DVGPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	150 75 50 37 30 25 20	Ω

4.8.2 Single Voltage GPIO Output Buffer Impedance

Table 31 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 31. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	150 75 50 37 30 25 20	Ω

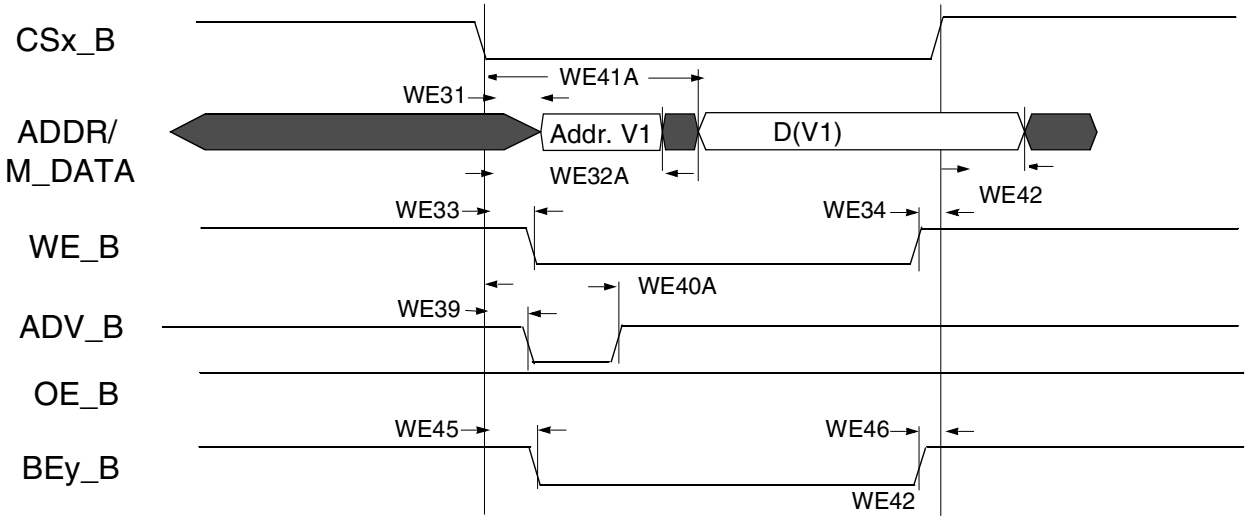


Figure 19. Asynchronous A/D Muxed Write Access

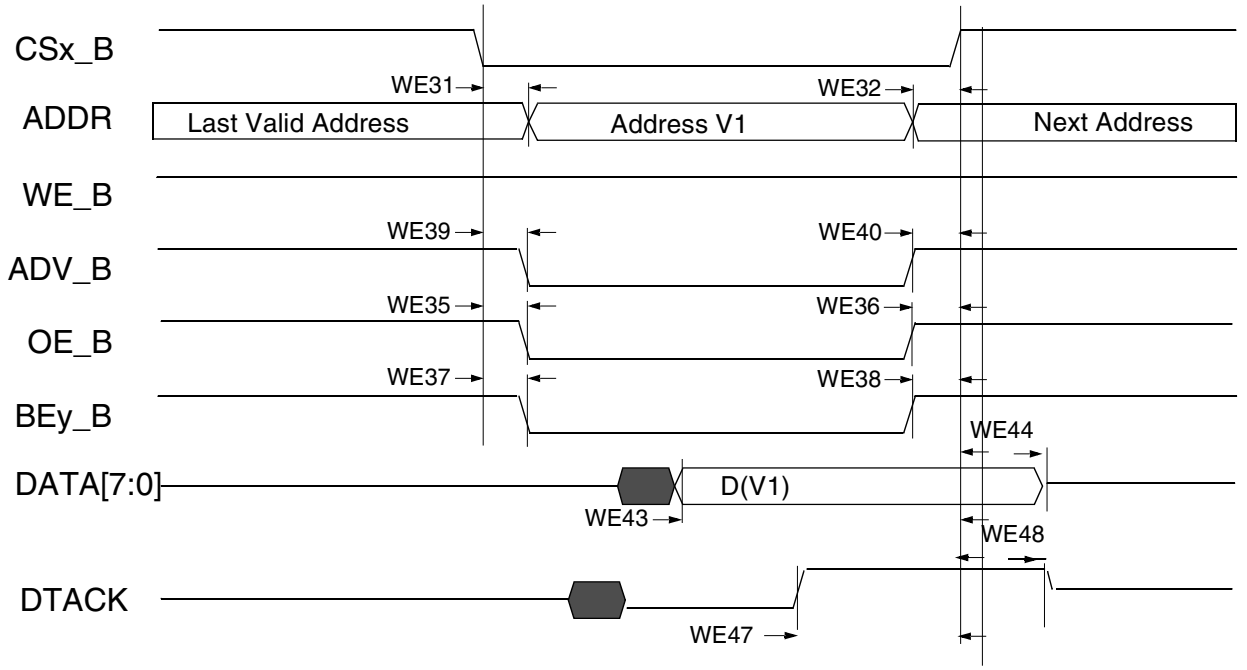


Figure 20. DTACK Read Access (DAP=0)

Table 39. DDR3 Timing Parameter Table (continued)

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR6	Address output setup time	t_{IS}	800	—	ps
DDR7	Address output hold time	t_{IH}	580	—	ps

1 All measurements are in reference to Vref level.

2 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Figure 23 shows the DDR3 write timing diagram. The timing parameters for this diagram appear in Table 40.

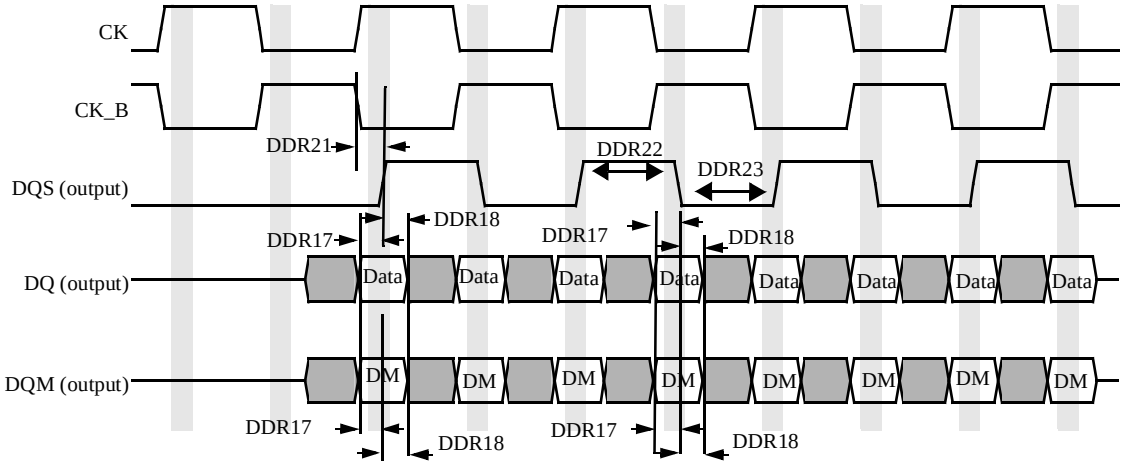


Figure 23. DDR3 Write Cycle

Table 40. DDR3 Write Cycle

ID	Parameter	Symbol	CK = 400MHz		Unit
			Min	Max	
DDR17	DQ and DQM setup time to DQS (differential strobe)	t_{DS}	420	—	ps
DDR18	DQ and DQM hold time to DQS (differential strobe)	t_{DH}	345	—	ps
DDR21	DQS latching rising transitions to associated clock edges	t_{DQSS}	-0.25	+0.25	tCK
DDR22	DQS high level width	t_{DQSH}	0.45	0.55	tCK
DDR23	DQS low level width	t_{DQSL}	0.45	0.55	tCK

1 To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

2 All measurements are in reference to Vref level.

3 Measurements were taken using balanced load and 25 Ω resistor from outputs to VDD_REF.

The CSI enables the chip to connect directly to external CMOS image sensors, which are classified as dumb or smart as follows:

- Dumb sensors only support traditional sensor timing (vertical sync (VSYNC) and horizontal sync(HSYNC)) and output-only Bayer and statistics data.
- Smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats).

The following subsections describe the CSI timing in gated and ungated clock modes.

4.10.3 ECSPI Timing Parameters

This section describes the timing parameters of the ECSPI block. The ECSPI has separate timing parameters for master and slave modes.

4.10.3.1 ECSPI Master Mode Timing

Figure 31 depicts the timing of ECSPI in master mode and Table 47 lists the ECSPI master mode timing characteristics.

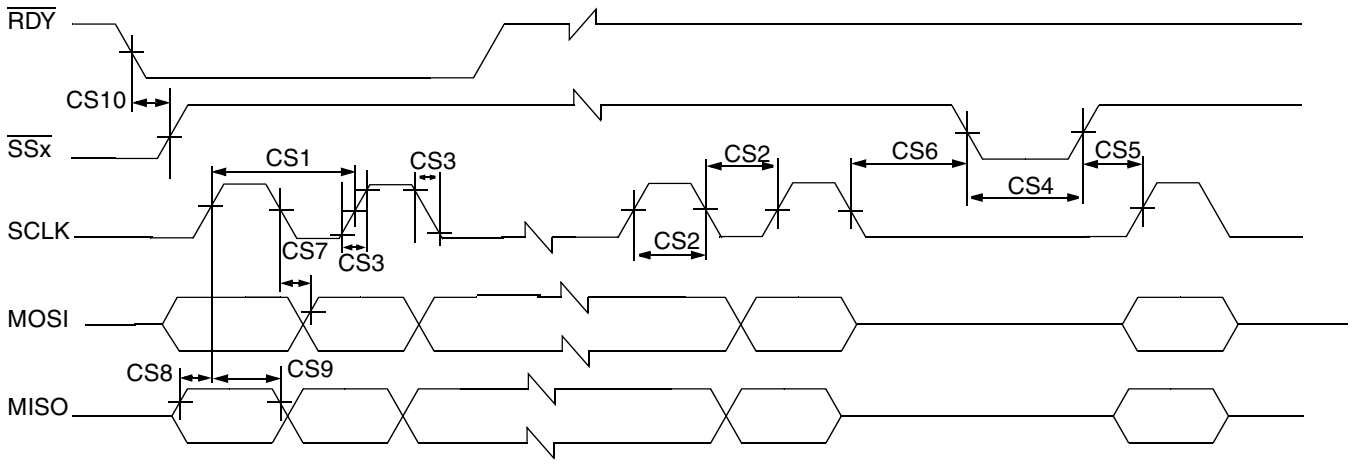


Figure 31. ECSPI Master Mode Timing Diagram

Table 47. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time–Read • Slow group[1] • Fast group[2] SCLK Cycle Time–Write	t_{clk}	 46 40 15	—	ns
CS2	SCLK High or Low Time–Read • Slow group[1] • Fast group[2] SCLK High or Low Time–Write	t_{SW}	 22 20 7	—	ns

Table 62. SSI Transmitter Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.10.11 UART I/O Configuration and Timing Parameters

4.10.11.1 UART RS-232 I/O Configuration in Different Modes

The i.MX 6SoloLite UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0 – DCE mode). Table 66 shows the UART I/O configuration based on the enabled mode.

Table 66. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
RTS	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
CTS	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
DTR	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
DSR	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
DCD	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
RI	Input	RING from DCE to DTE	Output	RING from DCE to DTE
TXD_MUX	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
RXD_MUX	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.10.11.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.10.11.2.1 UART Transmitter

Figure 53 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 67 lists the UART RS-232 serial mode transmit timing characteristics.

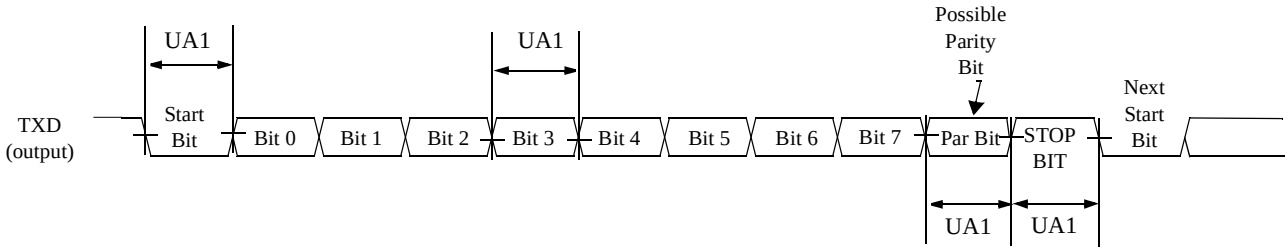


Figure 53. UART RS-232 Serial Mode Transmit Timing Diagram

Table 67. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.10.11.2.2 UART Receiver

Figure 54 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 68 lists serial mode receive timing characteristics.

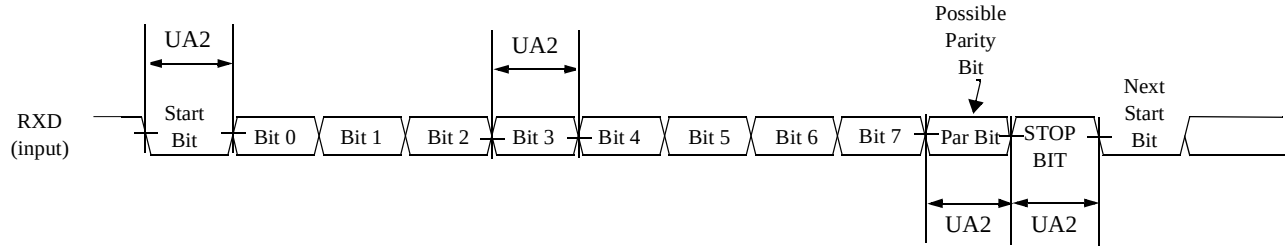


Figure 54. UART RS-232 Serial Mode Receive Timing Diagram

Table 68. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] – $1/(16*F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16*F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16*F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16*F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.10.12 USB HSIC Timings

This section describes the electrical information of the USB HSIC port.

NOTE

HSIC is DDR signal, following timing spec is for both rising and falling edge.

4.10.12.1 Transmit Timing

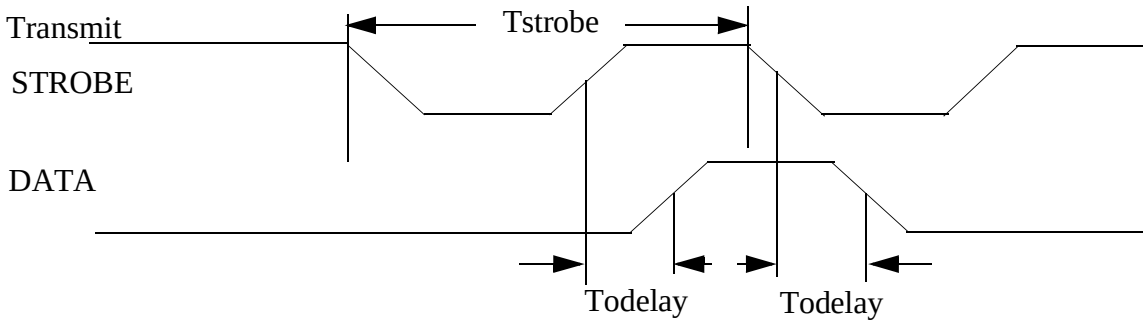


Figure 57. USB HSIC Transmit Waveform

Table 71. USB HSIC Transmit Parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	
Todelay	data output delay time	550	1350	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

4.10.12.2 Receive Timing

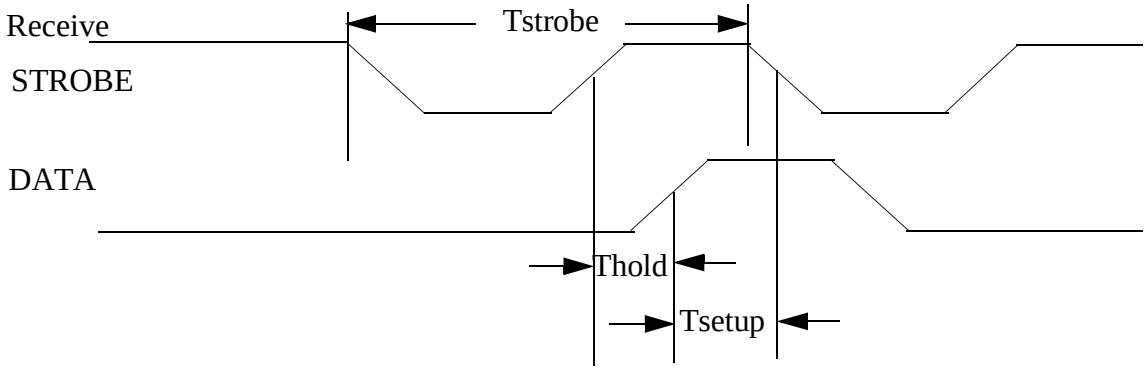


Figure 58. USB HSIC Receive Waveform

Table 79. 13 x 13 mm Supplies Contact Assignment (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
VDD_SNVS_CAP	AD20	Secondary Supply for the SNVS (internal regulator output—requires capacitor if internal regulator is used)
VDD_SNVS_IN	AC20	Primary Supply, for the SNVS Regulator
VDD_SOC_CAP	J7, J8, J9, K7, K8, K9, N18, P18, R18	Secondary Supply for the SoC and PU (internal regulator output—requires capacitor if internal regulator is used)
VDD_SOC_IN	J10, J11, K10, K11, R16, R17, T16, T17, T18	Primary Supply, for the SoC and PU Regulators
VDD_USB_CAP	U14	Secondary Supply for the 3V Domain (USBPHY, MLPBPHY, eFuse), internal regulator output, requires capacitor if internal regulator is used.
USB_OTG1_VBUS	AA18	
USB_OTG2_VBUS	AD18	
ZQPAD	AE17	
NC	C4, C5, C8, C9, C12, C13, C16, C17, C20, C21, D4, D5, D8, D9, D12, D13, D16, D17, D20, D21, E8, E9, E12, E13, E16, E17, F3, F4, F5, F6, F8, F9, F12, F13, F16, F17, F19, F20, F21, F22, G3, G4, G5, G6, G19, G20, G21, G22, H8, H9, H12, H13, H16, H17, K3, K4, K5, K6, K19, K20, K21, K22, L3, L4, L5, L6, L8, L17, L19, L20, L21, L22, P3, P4, P5, P6, P8, P17, P19, P20, P21, P22, R3, R4, R5, R6, R19, R20, R21, R22, U8, U9, U12, U13, U16, U17, V3, V4, V5, V6, V19, V20, V21, V22, W3, W4, W5, W6, W8, W9, W12, W13, W16, W17, W19, W20, W21, W22, Y8, Y9, Y12, Y13, Y16, Y17, AA4, AA5, AA8, AA9, AA12, AA13, AA16, AA17, AA20, AA21, AB4, AB5, AB8, AB9, AB12, AB13, AB16, AB17 AB20, AB21	No Connections.

Table 80 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 80. 13 x 13 mm Functional Contact Assignments

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
AUD_MCLK	H19	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[6]	Input	Keeper
AUD_RXC	J21	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[1]	Input	Keeper
AUD_RXD	J20	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[2]	Input	Keeper
AUD_RXFS	J19	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[0]	Input	Keeper

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
AUD_TXC	H20	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[3]	Input	Keeper
AUD_TXD	J22	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[5]	Input	Keeper
AUD_TXFS	H21	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[4]	Input	Keeper
BOOT_MODE0	AC15	VDD_SNVS_IN	GPIO	ALT0	src_BOOT_MODE[0]	Input	Keeper
BOOT_MODE1	AB15	VDD_SNVS_IN	GPIO	ALT0	src_BOOT_MODE[1]	Input	Keeper
CLK1_N	AD23	VDDHIGH_CAP			CLK1_N	—	—
CLK1_P	AC23	VDDHIGH_CAP			CLK1_P	—	—
DRAM_A0	U4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[0]	Output	0
DRAM_A1	U5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[1]	Output	0
DRAM_A10	J2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[10]	Output	0
DRAM_A11	T2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[11]	Output	0
DRAM_A12	U2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[12]	Output	0
DRAM_A13	H5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[13]	Output	0
DRAM_A14	R2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[14]	Output	0
DRAM_A15	K2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[15]	Output	0
DRAM_A2	T3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[2]	Output	0
DRAM_A3	T4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[3]	Output	0
DRAM_A4	N4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[4]	Output	0
DRAM_A5	M3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[5]	Output	0
DRAM_A6	M4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[6]	Output	0
DRAM_A7	H4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[7]	Output	0
DRAM_A8	J3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[8]	Output	0
DRAM_A9	J4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[9]	Output	0
DRAM_CAS_B	P1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_CAS	Output	0
DRAM_CS0_B	N2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_CS[0]	Output	0
DRAM_CS1_B	L2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_CS[1]	Output	0
DRAM_D0	AC2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[0]	Input	PU (100K)
DRAM_D1	AC1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[1]	Input	PU (100K)
DRAM_D10	E3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[10]	Input	PU (100K)
DRAM_D11	D3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[11]	Input	PU (100K)

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
JTAG_MOD	Y14	NVCC_JTAG	GPIO	ALT5	sjc_MOD		PU (100K)
JTAG_TCK	AA14	NVCC_JTAG	GPIO	ALT5	sjc_TCK		PU (47K)
JTAG_TDI	W14	NVCC_JTAG	GPIO	ALT5	sjc_TDI		PU (47K)
JTAG_TDO	W15	NVCC_JTAG	GPIO	ALT5	sjc_TDO		Keeper
JTAG_TMS	Y15	NVCC_JTAG	GPIO	ALT5	sjc_TMS		PU (47K)
JTAG_TRSTB	AA15	NVCC_JTAG	GPIO	ALT5	sjc_TRSTB		PU (47K)
KEY_COL0	G23	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[24]	Input	Keeper
KEY_COL1	F23	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[26]	Input	Keeper
KEY_COL2	E23	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[28]	Input	Keeper
KEY_COL3	E22	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[30]	Input	Keeper
KEY_COL4	E20	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[0]	Input	Keeper
KEY_COL5	D24	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[2]	Input	Keeper
KEY_COL6	D22	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[4]	Input	Keeper
KEY_COL7	C23	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[6]	Input	Keeper
KEY_ROW0	G24	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[25]	Input	Keeper
KEY_ROW1	F24	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[27]	Input	Keeper
KEY_ROW2	E24	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[29]	Input	Keeper
KEY_ROW3	E21	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[31]	Input	Keeper
KEY_ROW4	E19	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[1]	Input	Keeper
KEY_ROW5	D23	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[3]	Input	Keeper
KEY_ROW6	C24	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[5]	Input	Keeper
KEY_ROW7	B24	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[7]	Input	Keeper
LCD_CLK	T22	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[15]	Input	Keeper
LCD_DAT0	Y24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[20]	Input	Keeper
LCD_DAT1	W23	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[21]	Input	Keeper
LCD_DAT10	R23	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[30]	Input	Keeper
LCD_DAT11	R24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[31]	Input	Keeper
LCD_DAT12	P23	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[0]	Input	Keeper
LCD_DAT13	P24	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[1]	Input	Keeper
LCD_DAT14	N21	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[2]	Input	Keeper

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
LCD_DAT15	N23	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[3]	Input	Keeper
LCD_DAT16	N24	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[4]	Input	Keeper
LCD_DAT17	M22	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[5]	Input	Keeper
LCD_DAT18	M23	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[6]	Input	Keeper
LCD_DAT19	M24	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[7]	Input	Keeper
LCD_DAT2	W24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[22]	Input	Keeper
LCD_DAT20	L23	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[8]	Input	Keeper
LCD_DAT21	L24	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[9]	Input	Keeper
LCD_DAT22	K23	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[10]	Input	Keeper
LCD_DAT23	K24	NVCC_LCD	GPIO	ALT5	gpio3_GPIO[11]	Input	Keeper
LCD_DAT3	V23	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[23]	Input	Keeper
LCD_DAT4	V24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[24]	Input	Keeper
LCD_DAT5	U21	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[25]	Input	Keeper
LCD_DAT6	U23	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[26]	Input	Keeper
LCD_DAT7	U24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[27]	Input	Keeper
LCD_DAT8	T23	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[28]	Input	Keeper
LCD_DAT9	T24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[29]	Input	Keeper
LCD_ENABLE	J24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[16]	Input	Keeper
LCD_HSYNC	H23	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[17]	Input	Keeper
LCD_RESET	H24	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[19]	Input	Keeper
LCD_VSYNC	J23	NVCC_LCD	GPIO	ALT5	gpio2_GPIO[18]	Input	Keeper
ONOFF	W18	VDD_SNVS_IN	GPIO		src_ONOFF	Input	PU (100K)
PMIC_ON_REQ	AD15	VDD_SNVS_IN	GPIO	ALT0	snvs_lp_wrapper_SNVS_WAKEUP_ALARM	Output	Open Drain with PU (100K)
PMIC_STBY_REQ	AD16	VDD_SNVS_IN	GPIO	ALT0	ccm_PMIC_VSTBY_REQ	Output	0
POR_B	AC16	VDD_SNVS_IN	GPIO	ALT0	src_POR_B	Input	PU (100K)
PWM1	Y7	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[23]	Input	Keeper
REF_CLK_24M	AC14	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[21]	Input	Keeper
REF_CLK_32K	AD14	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[22]	Input	Keeper