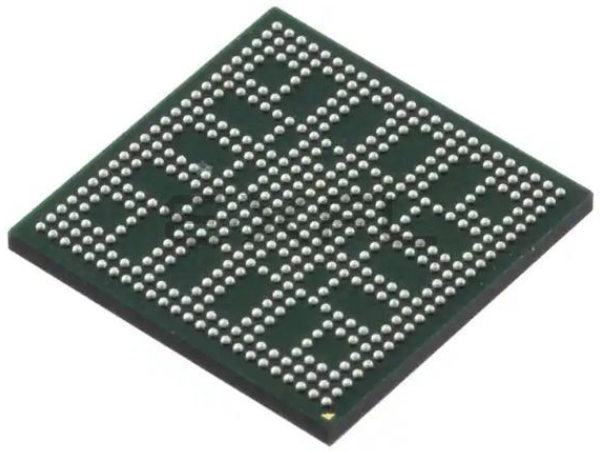

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (3)
Voltage - I/O	1.2V, 1.8V, 3.0V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	432-TFBGA
Supplier Device Package	432-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6l2evn10ab

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SPDC	Electrophoretic Display Controller	Peripherals	The SPDC is a feature-rich, low power, and high-performance direct-drive, active matrix EPD controller. It is specifically designed to drive SiPix™ EPD panels, supporting a wide variety of TFT backplanes.
SPDIF	Sony Phillips Digital Interface	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface, which is used on the AP to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options. The SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream that reduces CPU overhead in use cases where two time slots are being used simultaneously.
TEMPMON	Temperature Monitor	System Control Peripherals	The temperature monitor/sensor IP, for detecting high temperature conditions. The Temperature sensor IP for detecting die temperature. The temperature read out does not reflect case or ambient temperature, but the proximity of the temperature sensor location on the die. Temperature distribution may not be uniformly distributed, therefore the read out value may not be the reflection of the temperature value of the entire die.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 4 MHz. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard and the i.MX31 UART modules. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOH2A	2x USB 2.0 High Speed OTG and 1x HS Hosts	Connectivity Peripherals	USBO2H contains: • One Two high-speed OTG module with integrated HS USB PHY • One identical high-speed Host modules connected to HSIC USB ports.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC-1 uSDHC-2 uSDHC-2 uSDHC-4	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6SoloLite specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.2/4.3/4.4 including high-capacity (size > 2 GB) cards HC MMC. HW reset as specified for eMMC cards is supported at ports #3 and #4 only. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v1.10 • Fully compliant with SD Card Specification, Part A2, SD Host Controller Standard Specification, v2.00 All four ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) However, the SoC level integration and I/O muxing logic restrict the functionality to the following: • Instances #1 and #2 are primarily intended to serve as external slots or interfaces to on-board SDIO devices. These ports are equipped with “Card detection” and “Write Protection” pads and do not support HW reset • All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for Ports #1 and #2 in four bit configuration (SD interface). Port #3 is placed in his own independent power domain and port #4 shares power domain with some other interfaces.
WDOG-1	Watchdog	Timer Peripherals	The Watchdog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG-2 (TZ)	Watchdog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system’s security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode Software.
XTALOSC	Crystal Oscillator I/F	Clocking	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator.

Table 8. Package Thermal Resistance Data (continued)

Rating	Board	Symbol	No Lid	Unit
Junction to Ambient[1] (at 200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	40	°C/W
	Four layer board (2s2p)	$R_{\theta JMA}$	24	°C/W
Junction to Board[2]	—	$R_{\theta JB}$	14	°C/W
Junction to Case[3] (Top)	—	$R_{\theta JCtop}$	9	°C/W
Junction to Package Top[4]	Natural Convection	Ψ_{JT}	2	°C/W

1 Junction-to-Ambient Thermal Resistance was determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-Board Thermal Resistance was determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

3 Junction-to-Case at the top of the package was determined by using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 9 provides the operating ranges of the i.MX 6SoloLite processor.

Table 9. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
Run mode: LDO enabled	VDD_ARM_IN	1.375[2]		1.5	V	LDO output set at 1.250V minimum for operation up to 996MHz.
		1.275[2]		1.5	V	LDO output set at 1.150V minimum for operation up to 792MHz
		1.075[2]		1.5	V	LDO output set at 0.95V minimum for operation up to 396MHz
		1.075[2]		1.5	V	LDO output set at 0.950V minimum for operation up to 192MHz
		1.050[2]		1.5	V	LDO output set at 0.9250V minimum for operation up to 24MHz
	VDD_SOC_IN[3] VDD_PU_IN	1.275[2,4]		1.5	V	VDD_SOC and VDD_PU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.15 V minimum.
Run mode: LDO bypassed	VDD_ARM_IN	1.250		1.3	V	LDO bypassed for operation up to 996 MHz.
		1.150		1.3	V	LDO bypassed for operation up to 792 MHz.
		0.950		1.3	V	LDO bypassed for operation up to 396 MHz.
		0.950		1.3	V	LDO bypassed for operation up to 192MHz
		0.925		1.3	V	LDO bypassed for operation up to 24MHz
	VDD_SOC_IN[3] VDD_PU_IN	1.15[4]		1.3	V	
Standby/DSM Mode	VDD_ARM_IN	0.9		1.3	V	See Table 12, "Stop Mode Current and Power Consumption," on page 24.
	VDD_SOC_IN VDD_PU_IN	0.9		1.3	V	
VDDHIGH internal Regulator	VDD_HIGH_IN[5]	2.8		3.3	V	Must match the range of voltges that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[5]	2.8		3.3	V	Should be supplied from the same supply as VDDHIGH_IN if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG1_VBUS USB_OTG2_VBUS	4.4		5.25	V	
DDR I/O supply	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2
		1.425	1.5	1.575	V	DDR3
	NVCC_DRAM_2P5	2.5	2.5	2.75	V	

[3] Recommended nominal frequency 32.768 kHz.

[4] External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 10 are required for use with Freescale BSPs to ensure precise time keeping and USB operation. For RTC_XTAL operation, two clock sources are available:

- On-chip 40 kHz ring oscillator: This clock source has the following characteristics:
  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit
  - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator
  - If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision timeout.

4.1.5 Maximal Supply Currents

The Power Virus numbers shown in Table 11 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The MMPF0100xxxx, Freescale's power management IC targeted for the i.MX 6x family, supports the Power Virus mode operating at 1% duty cycle. Higher duty cycles are allowed, but a robust thermal design is required for the increased system power dissipation.

See the i.MX 6SoloLite Power Consumption Measurement Application Note for more details on typical power consumption under various use case definitions.

Table 11. Maximal Supply Currents

Power Line	Conditions	Max Current	Unit
VDD_ARM_IN	1 GHz ARM clock based on Power Virus operation	1100	mA
VDD_SOC_IN	1 GHz ARM clock	650	mA
VDD_PU_IN	1 GHz ARM clock	150	mA
VDD_HIGH_IN	—	30[1]	mA
VDD_SNVS_IN	—	250[2]	µA

Table 28. DDR I/O DDR3 Mode AC Parameters[1] (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	Driver impedance = 34 Ω	2.5	—	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

1 Note that the JEDEC JESD79_3C specification supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) – Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 * OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4.8 Output Buffer Impedance Parameters

This section defines the I/O impedance parameters of the i.MX 6SoloLite processor for the following I/O types:

- Dual Voltage General Purpose I/O cell set (DVGPIO)
- Single Voltage General Purpose I/O cell set (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2, and DDR3 modes

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 7).

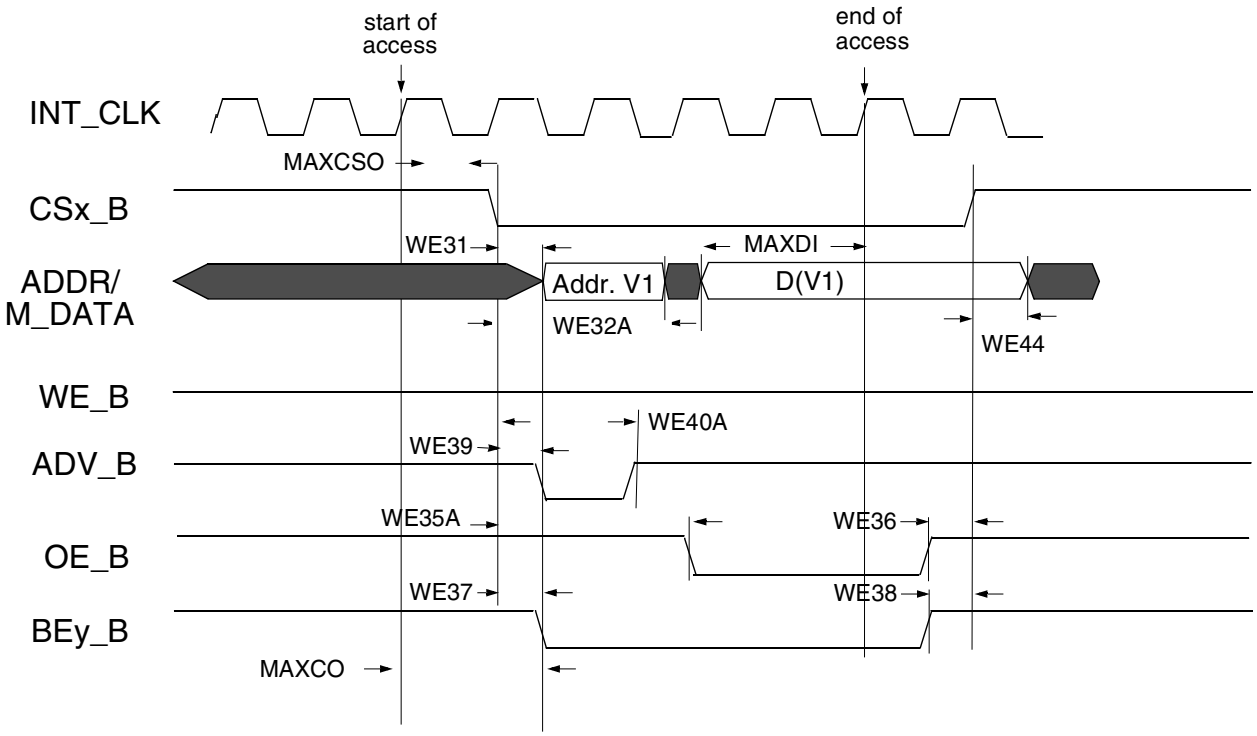


Figure 17. Asynchronous A/D Muxed Read Access (RWSC = 5)

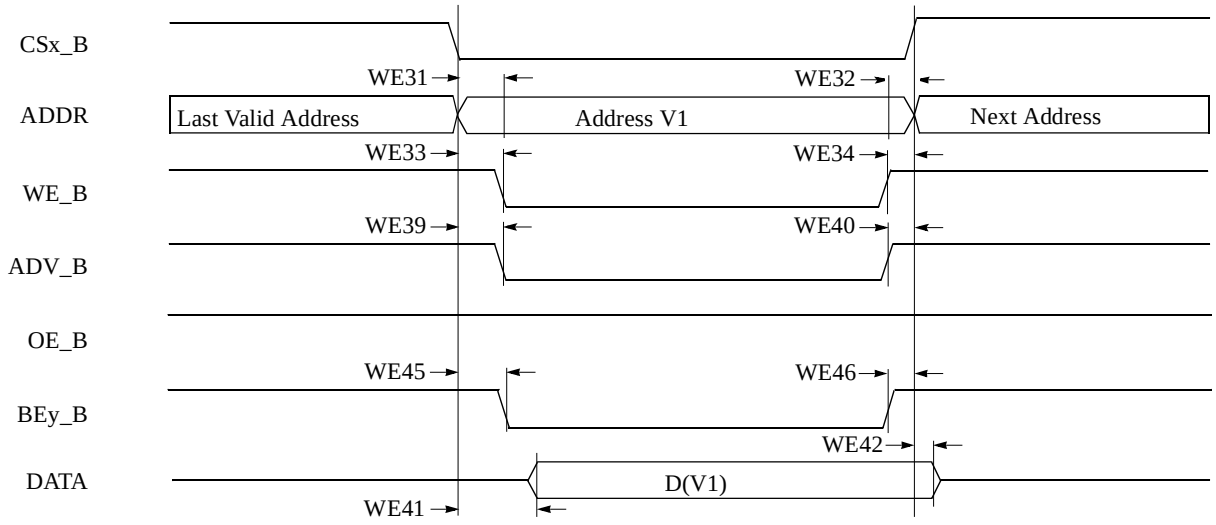


Figure 18. Asynchronous Memory Write Access

4.9.4 DDR SDRAM Specific Parameters (DDR3 and LPDDR2)

4.9.4.1 DDR3 Parameters

Figure 22 shows the DDR3 basic timing diagram. The timing parameters for this diagram appear in Table 39.

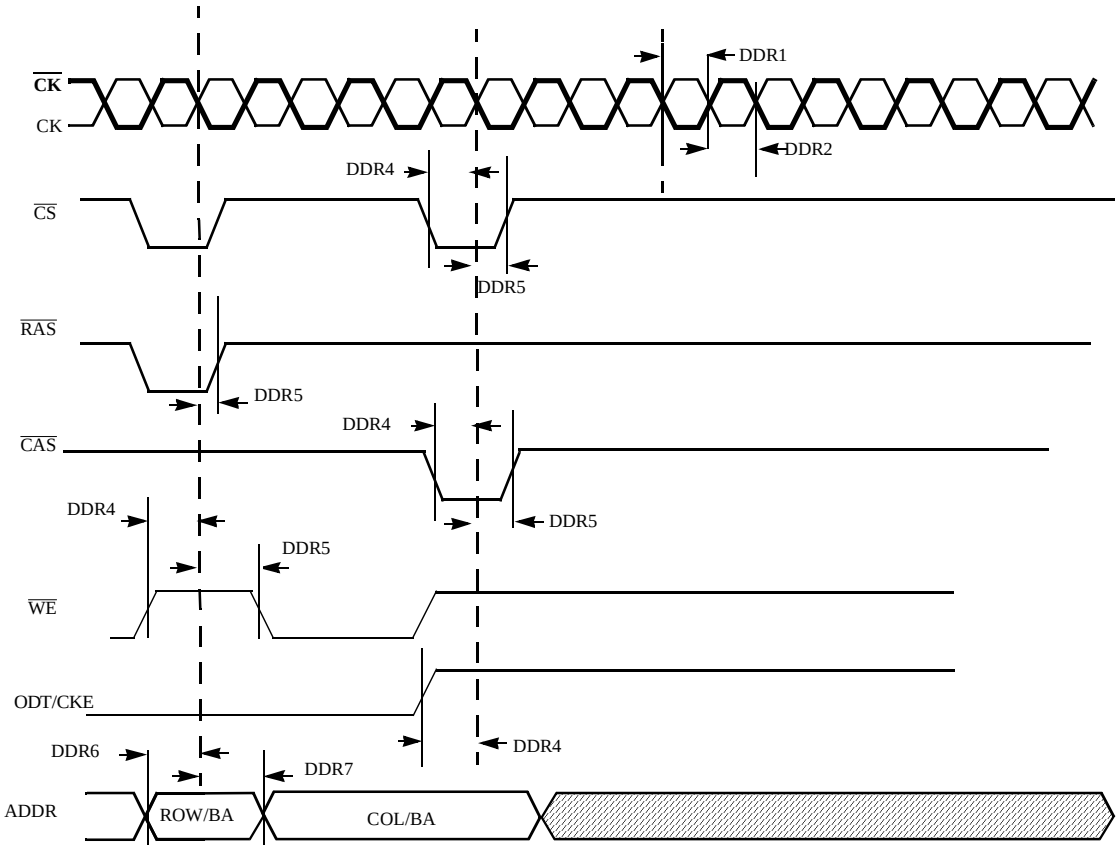


Figure 22. DDR3 Command and Address Timing Diagram

Table 39. DDR3 Timing Parameter Table

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR1	CK clock high-level width	t_{CH}	0.47	0.53	t_{CK}
DDR2	CK clock low-level width	t_{CL}	0.47	0.53	t_{CK}
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	t_{IS}	800	—	ps
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	t_{IH}	580	—	ps

Table 39. DDR3 Timing Parameter Table (continued)

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR6	Address output setup time	t_{IS}	800	—	ps
DDR7	Address output hold time	t_{IH}	580	—	ps

1 All measurements are in reference to Vref level.

2 Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Figure 23 shows the DDR3 write timing diagram. The timing parameters for this diagram appear in Table 40.

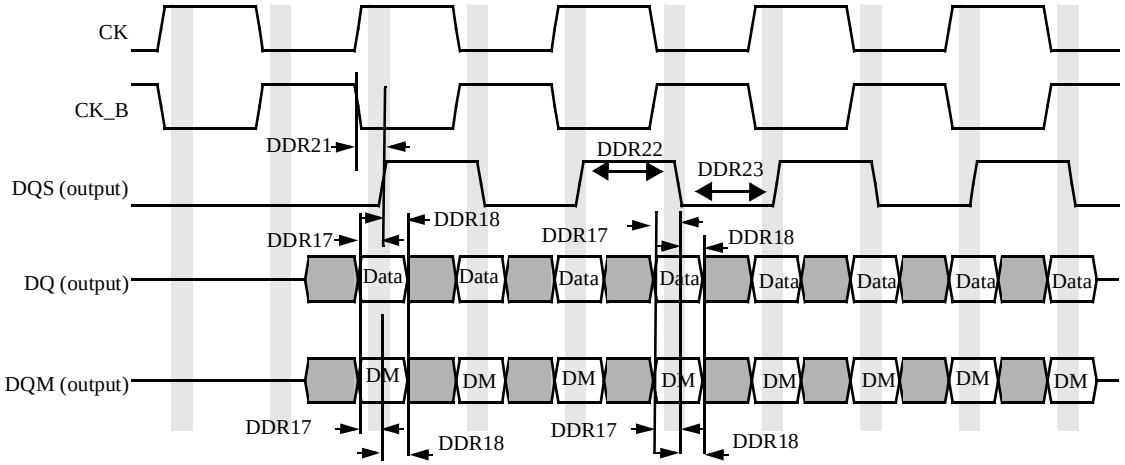


Figure 23. DDR3 Write Cycle

Table 40. DDR3 Write Cycle

ID	Parameter	Symbol	CK = 400MHz		Unit
			Min	Max	
DDR17	DQ and DQM setup time to DQS (differential strobe)	t_{DS}	420	—	ps
DDR18	DQ and DQM hold time to DQS (differential strobe)	t_{DH}	345	—	ps
DDR21	DQS latching rising transitions to associated clock edges	t_{DQSS}	-0.25	+0.25	tCK
DDR22	DQS high level width	t_{DQSH}	0.45	0.55	tCK
DDR23	DQS low level width	t_{DQSL}	0.45	0.55	tCK

1 To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

2 All measurements are in reference to Vref level.

3 Measurements were taken using balanced load and 25 Ω resistor from outputs to VDD_REF.

Table 45. CSI Gated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI VSYNC to HSYNC time	tV2H	67.5	—	ns
P2	CSI HSYNC setup time	tHsu	2	—	ns
P3	CSI DATA setup time	tDsu	2.5	—	ns
P4	CSI DATA hold time	tDh	1.2	—	ns
P5	CSI pixel clock high time	tCLKh	10	—	ns
P6	CSI pixel clock low time	tCLKl	10	—	ns
P7	CSI pixel clock frequency	fCLK	—	66 ± 10%	MHz

4.10.2.0.2 Ungated Clock Mode Timing

Figure 30 shows the ungated clock mode timings of CSI, and Table 46 describes the timing parameters (P1–P6) that are shown in the figure. In ungated mode the VSYNC and PIXCLK signals are used, and the HSYNC signal is ignored.

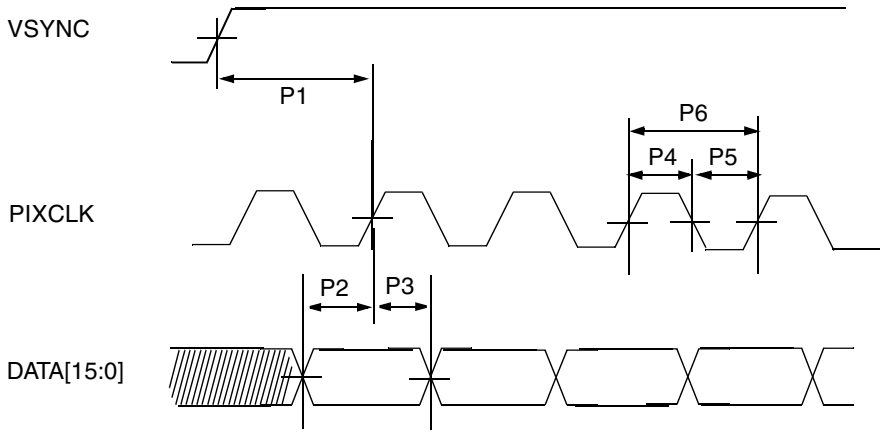


Figure 30. CSI Ungated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

Table 46. CSI Ungated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min.	Max.	Units
P1	CSI VSYNC to pixel clock time	tVSYNC	67.5	—	ns
P2	CSI DATA setup time	tDsu	2.5	—	ns
P3	CSI DATA hold time	tDh	1.2	—	ns
P4	CSI pixel clock high time	tCLKh	10	—	ns
P5	CSI pixel clock low time	tCLKl	10	—	ns
P6	CSI pixel clock frequency	fCLK	—	66 ± 10%	MHz

Table 51. SDR50/SDR104 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input/Card Outputs CMD, DAT in SDR104 (Reference to CLK)[2]					
SD8	Card Output Data Window	t_{ODW}	$0.5*t_{CLK}$	—	ns

[1] If using KEY_COL1, KEY_ROW1, KEY_COL2 and KEY_ROW2 for USDHC3_DAT4 - USDHC3_DAT7, please note that the timing is differnt. t_{od} min is -1.1 and t_{od} max is 1.5

[2]Data window in SDR100 mode is variable.

4.10.5 FEC AC Timing Parameters

This section describes the electrical information of the Fast Ethernet Controller (FEC) module. The FEC is designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports the 10/100 Mbps MII (18 pins in total) and the 10 Mbps (only 7-wire interface, which uses 7 of the MII pins), for connection to an external Ethernet transceiver. For the pin list of MII and 7-wire, see the i.MX 6SoloLite Reference Manual.

This section describes the AC timing specifications of the FEC. The MII signals are compatible with transceivers operating at a voltage of 3.3 V.

4.10.5.1 MII Receive Signal Timing

The MII receive signal timing involves the FEC_RX_DATA3,2,1,0, FEC_RX_DV, FEC_RX_ER, and FEC_RX_CLK signals. The receiver functions correctly up to a FEC_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement but the processor clock frequency must exceed twice the FEC_RX_CLK frequency. Table 52 lists the MII receive channel signal timing parameters and Figure 36 shows MII receive signal timings.

Table 52. MII Receive Signal Timing

No.	Characteristics[1 2]	Min	Max	Unit
M1	FEC_RX_DATA3,2,1,0, FEC_RX_DV, FEC_RX_ER to FEC_RX_CLK setup	5	—	ns
M2	FEC_RX_CLK to FEC_RX_DATA3,2,1,0, FEC_RX_DV, FEC_RX_ER hold	5	—	ns
M3	FEC_RX_CLK pulse width high	35%	65%	FEC_RX_CLK period
M4	FEC_RX_CLK pulse width low	35%	65%	FEC_RX_CLK period

[1] FEC_RX_DV, FEC_RX_CLK, and FEC_RXD0 have same timing in 10 Mbps 7-wire interface mode.

[2] Test conditions: 25pF on each output signal.

Figure 42 depicts the timing of the PWM, and Table 58 lists the PWM timing parameters.

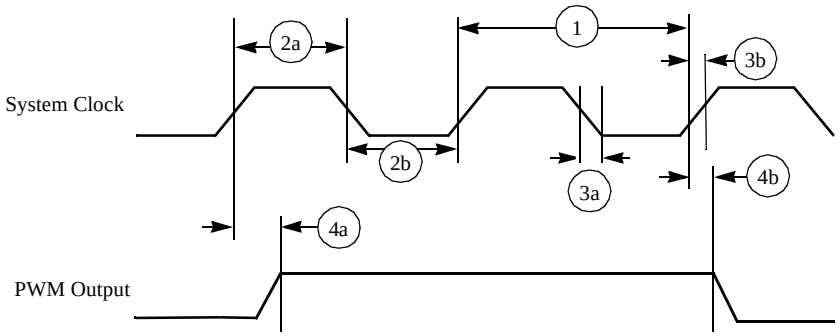


Figure 42. PWM Timing

Table 58. PWM Output Timing Parameters

Reference Number	Parameter	Min	Max	Unit
1	System CLK frequency[1]	0	ipg_clk	MHz
2a	Clock high time	12.29	—	ns
2b	Clock low time	9.91	—	ns

[1] CL of PWMO = 30 pF

4.10.8 SCAN JTAG Controller (SJC) Timing Parameters

Figure 43 depicts the SJC test clock input timing. Figure 44 depicts the SJC boundary scan timing. Figure 45 depicts the SJC test access port. Signal parameters are listed in Table 59.

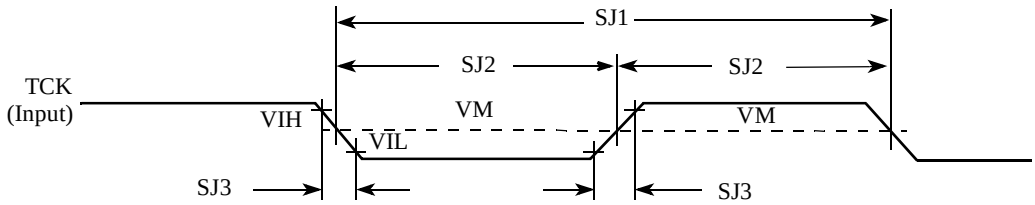
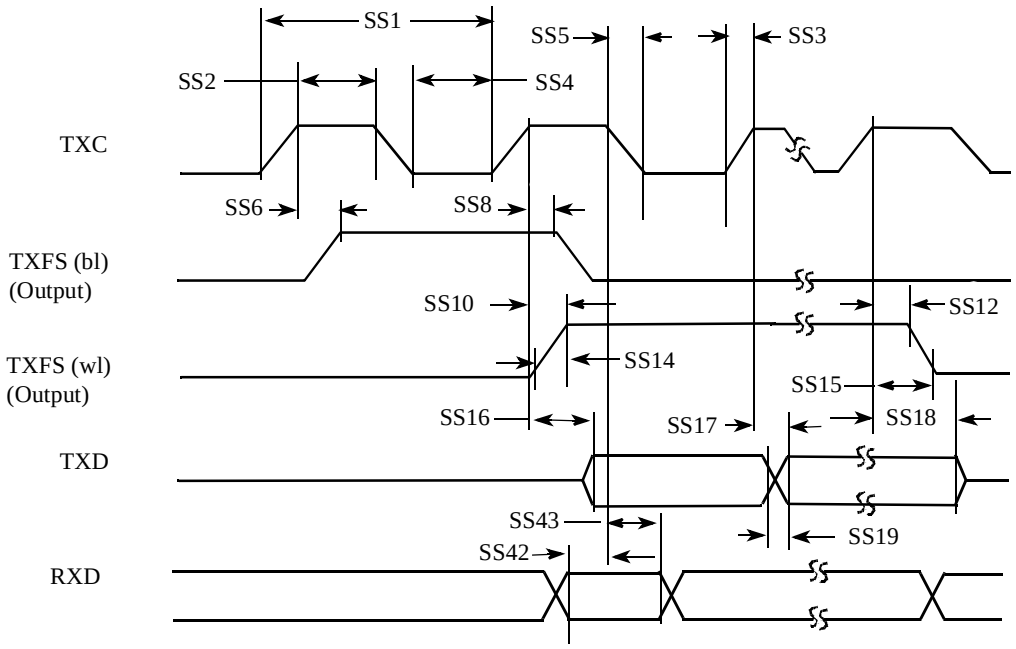


Figure 43. Test Clock Input Timing Diagram

4.10.10.1 SSI Transmitter Timing with Internal Clock

Figure 49 depicts the SSI transmitter internal clock timing and Table 62 lists the timing parameters for the SSI transmitter internal clock.



Note: SRXD input in synchronous mode only

Figure 49. SSI Transmitter Internal Clock Timing Diagram

Table 62. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) Internal FS rise time	—	6.0	ns
SS15	(Tx/Rx) Internal FS fall time	—	6.0	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS17	(Tx) CK high to STXD high/low	—	15.0	ns
SS18	(Tx) CK high to STXD high impedance	—	15.0	ns

4.10.10.2 SSI Receiver Timing with Internal Clock

Figure 50 depicts the SSI receiver internal clock timing and Table 63 lists the timing parameters for the receiver timing with the internal clock.

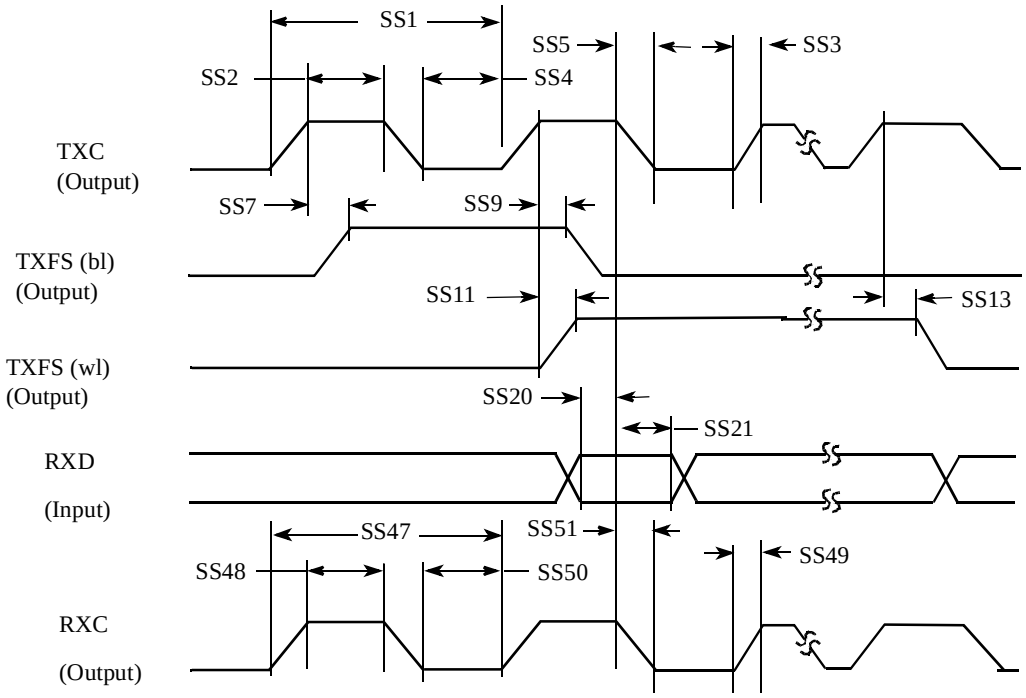


Figure 50. SSI Receiver Internal Clock Timing Diagram

Table 63. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	10.0	—	ns
SS21	SRXD hold time after (Rx) CK low	0.0	—	ns
Oversampling Clock Operation				

Table 64. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.10.10.4 SSI Receiver Timing with External Clock

Figure 52 depicts the SSI receiver external clock timing and Table 65 lists the timing parameters for the receiver timing with the external clock.

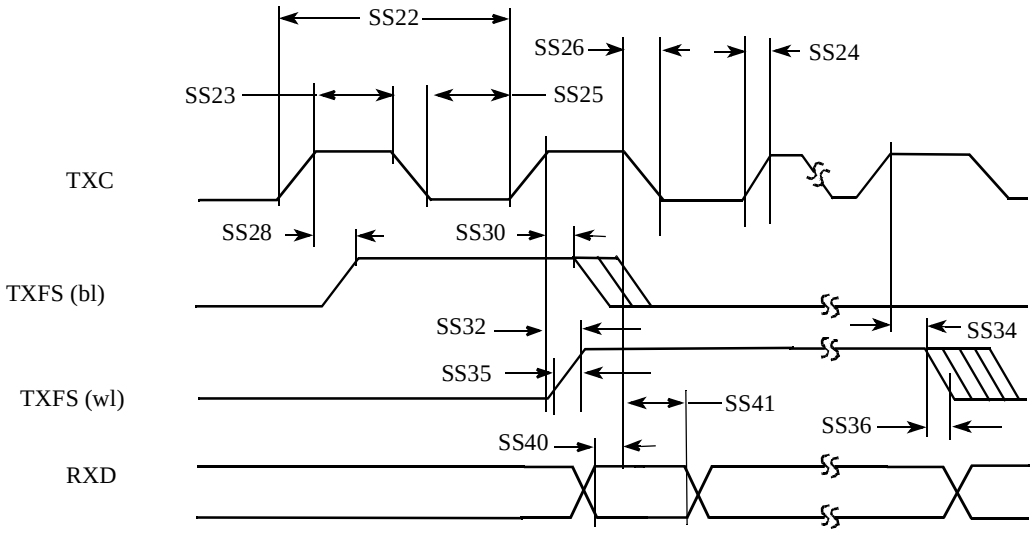


Figure 52. SSI Receiver External Clock Timing Diagram

Table 65. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	(Rx) CK high to FS (bl) high	–10	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10	—	ns
SS32	(Rx) CK high to FS (wl) high	–10	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10	—	ns
SS41	SRXD hold time after (Rx) CK low	2	—	ns

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
AUD_TXC	H20	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[3]	Input	Keeper
AUD_TXD	J22	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[5]	Input	Keeper
AUD_TXFS	H21	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[4]	Input	Keeper
BOOT_MODE0	AC15	VDD_SNVS_IN	GPIO	ALT0	src_BOOT_MODE[0]	Input	Keeper
BOOT_MODE1	AB15	VDD_SNVS_IN	GPIO	ALT0	src_BOOT_MODE[1]	Input	Keeper
CLK1_N	AD23	VDDHIGH_CAP			CLK1_N	—	—
CLK1_P	AC23	VDDHIGH_CAP			CLK1_P	—	—
DRAM_A0	U4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[0]	Output	0
DRAM_A1	U5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[1]	Output	0
DRAM_A10	J2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[10]	Output	0
DRAM_A11	T2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[11]	Output	0
DRAM_A12	U2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[12]	Output	0
DRAM_A13	H5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[13]	Output	0
DRAM_A14	R2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[14]	Output	0
DRAM_A15	K2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[15]	Output	0
DRAM_A2	T3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[2]	Output	0
DRAM_A3	T4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[3]	Output	0
DRAM_A4	N4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[4]	Output	0
DRAM_A5	M3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[5]	Output	0
DRAM_A6	M4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[6]	Output	0
DRAM_A7	H4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[7]	Output	0
DRAM_A8	J3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[8]	Output	0
DRAM_A9	J4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[9]	Output	0
DRAM_CAS_B	P1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_CAS	Output	0
DRAM_CS0_B	N2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_CS[0]	Output	0
DRAM_CS1_B	L2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_CS[1]	Output	0
DRAM_D0	AC2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[0]	Input	PU (100K)
DRAM_D1	AC1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[1]	Input	PU (100K)
DRAM_D10	E3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[10]	Input	PU (100K)
DRAM_D11	D3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[11]	Input	PU (100K)

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
EPDC_PWRSTAT	E10	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[13]	Input	Keeper
EPDC_PWRWAKEUP	D10	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[14]	Input	Keeper
EPDC_SDCE0	C11	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[27]	Input	Keeper
EPDC_SDCE1	A10	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[28]	Input	Keeper
EPDC_SDCE2	B9	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[29]	Input	Keeper
EPDC_SDCE3	A9	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[30]	Input	Keeper
EPDC_SDCLK	B10	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[23]	Input	Keeper
EPDC_SDLE	B8	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[24]	Input	Keeper
EPDC_SDOE	E7	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[25]	Input	Keeper
EPDC_SDSHR	F7	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[26]	Input	Keeper
EPDC_VCOM0	C7	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[3]	Input	Keeper
EPDC_VCOM1	D7	NVCC_GPIO	GPIO	ALT5	gpio2_GPIO[4]	Input	Keeper
FEC_CRS_DV	AC9	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[25]	Input	Keeper
FEC_MDC	AA7	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[23]	Input	Keeper
FEC_MDIO	AB7	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[20]	Input	Keeper
FEC_REF_CLK	W10	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[26]	Input	Keeper
FEC_RX_ER	AD9	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[19]	Input	Keeper
FEC_RXD0	AA10	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[17]	Input	Keeper
FEC_RXD1	AC10	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[18]	Input	Keeper
FEC_TX_CLK	AC8	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[21]	Input	Keeper
FEC_TX_EN	AD10	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[22]	Input	Keeper
FEC_TXD0	Y10	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[24]	Input	Keeper
FEC_TXD1	W11	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[16]	Input	Keeper
HSIC_DAT	AA6	NVCC_GPIO	DDR		usb_H_DATA	Input	PD (100K)
HSIC_STROBE	AB6	NVCC_GPIO	DDR		usb_H_STROBE	Input	PD (100K)
I2C1_SCL	AC13	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[12]	Input	Keeper
I2C1_SDA	AD13	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[13]	Input	Keeper
I2C2_SCL	E18	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[14]	Input	Keeper
I2C2_SDA	D18	NVCC_GPIO	GPIO	ALT5	gpio3_GPIO[15]	Input	Keeper

Table 81. 13 x 13 mm, 0.5 mm Pitch Ball Map (continued)

8	9	10	11	12	13	14
DRAM_D31	EPDC_SDCE3	EPDC_SDCE1	EPDC_GDSP	EPDC_GDCLK	EPDC_D15	EPDC_D14
EPDC_SDLE	EPDC_SDCE2	EPDC_SDCLK	EPDC_PRWCOM	EPDC_GDRL	EPDC_GDOE	EPDC_D13
NC	**NC**	GND	EPDC_SDCE0	**NC**	**NC**	GND
NC	**NC**	EPDC_PWRWAKEUP	EPDC_PWRCTRL0	**NC**	**NC**	EPDC_D12
NC	**NC**	EPDC_PWRSTAT	EPDC_PWRCTRL1	**NC**	**NC**	NVCC18_IO
NC	**NC**	EPDC_PWRINT	EPDC_PWRCTRL2	**NC**	**NC**	EPDC_D11
GND	GND	GND	GND	EPDC_PWRCTRL3	GND	GND
NC	**NC**	NVCC33_IO	NVCC33_IO	**NC**	**NC**	NVCC33_IO
VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_IN	VDD_ARM_IN	VDD_ARM_IN
VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_IN	VDD_ARM_IN	VDD_ARM_IN
NC	GND	GND	GND	GND	GND	GND
GND	GND	GND	GND	GND	GND	GND
GND	GND	GND	GND	GND	GND	GND
NC	GND	GND	GND	GND	GND	GND
VDD_PU_CAP	VDD_PU_CAP	VDD_PU_IN	VDD_PU_IN	VDD_HIGH_IN	VDD_HIGH_IN	VDD_HIGH_CAP
VDD_PU_CAP	VDD_PU_CAP	VDD_PU_IN	VDD_PU_IN	VDD_HIGH_IN	VDD_HIGH_IN	VDD_HIGH_CAP
NC	**NC**	NVCC_3V3	NHVCC_3V3	**NC**	**NC**	VDD_USB_CAP
GND	GND	GND	GND	GND	GND	GND
NC	**NC**	FEC_REF_CLK	FEC_TXD1	**NC**	**NC**	JTAG_TDI
NC	**NC**	FEC_TXD0	NVCC18_IO	**NC**	**NC**	JTAG_MOD
NC	**NC**	FEC_RXD0	SD3_CMD	**NC**	**NC**	JTAG_TCK
NC	**NC**	GND	SD3_CLk	**NC**	**NC**	GND
FEC_TX_CLK	FEC_CRS_DV	FEC_RXD1	SD3_DAT0	SD3_DAT2	I2C1_SCL	REF_CLK_24M
DRAM_D16	FEC_RX_ER	FEC_TX_EN	SD3_DAT1	SD3_DAT3	I2C1_SDA	REF_CLK_32K

7 Revision History

Table 83 provides a revision history for this data sheet.

Table 83. i.MX 6SoloLite Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 1	11/2012	• Updated Table 77, "Interfaces Allocation During Boot," on page 97.
Rev 0.1	11/2012	• Updated Table 8, "Package Thermal Resistance Data," on page 18. • Corrected title of Table 79, “13 x 13 mm Supplies Contact Assignment,” on page 100. • Corrected title of Table 81, “13 x 13 mm, 0.5 mm Pitch Ball Map,” on page 110.
Rev. 0	10/2012	• Initial public release.