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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (3)
Voltage - I/O	1.2V, 1.8V, 3.0V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	432-TFBGA
Supplier Device Package	432-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx6l3dvn10aa

The i.MX 6SoloLite processor features:

- Applications processor—The processor enhances the capabilities of high-tier portable applications by fulfilling the ever increasing MIPS needs of operating systems and games. Freescale's Dynamic Voltage and Frequency Scaling (DVFS) provides significant power reduction, allowing the device to run at lower voltage and frequency with sufficient MIPS for tasks, such as audio decode.
- Multilevel memory system—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processor supports many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, PSRAM, cellular RAM, and managed NAND, including eMMC up to rev 4.4.
- Smart speed technology—The processor has power management throughout the IC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- Dynamic voltage and frequency scaling—The processor improves the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of each processor is enhanced by a multilevel cache system, Neon MPE (Media Processor Engine) co-processor, and a programmable smart DMA (SDMA) controller.
- Powerful graphics acceleration—Each processor provides three independent, integrated graphics processing units: 2D BLit engine, a 2D graphics accelerator, and dedicated OpenVG™ 1.1 accelerator.
- Interface flexibility—The processor supports connections to a variety of interfaces: LCD controller, CMOS sensor interface (parallel), high-speed USB on-the-go with PHY, high-speed USB host PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100 Mbps Ethernet controller, and a variety of other popular interfaces (such as UART, I^2C, and I^2S serial audio).
- Electronic Paper Display Controller—The processor integrates EPD controller that supports E-INK color and monochrome with up to 2048 x 1536 resolution at 106 Hz refresh, 4096 x 4096 resolution at 20 Hz refresh and 5-bit grayscale (32-levels per color channel). The processor also integrates an EPD controller that supports SiPix monochrome panels.
- Advanced security—The processor delivers hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the i.MX 6SoloLite security reference manual. Contact your local Freescale representative for more information.
- Integrated power management—The processor integrates linear regulators and generate internally all the voltage levels for different domains. This significantly simplifies system power management structure.
- GPIO with interrupt capabilities—The new GPIO pad design supports configurable dual voltage rails at 1.8V and 3.3V supplies. The pad is configurable to interface at either voltage level.

  - EPDC, color, and monochrome E-INK, up to 1650x2332 resolution and 5-bit grayscale
  - SPDC, color, and monochrome SiPix panels
- Camera sensors:
  - Parallel Camera port (up to 16 bit)
- Expansion cards:
  - Four MMC/SD/SDIO card ports all supporting:
    - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
    - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
- USB:
  - Two High Speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB Phy
  - One USB 2.0 (480 Mbps) hosts:
    - One HS hosts with integrated HS-IC USB (High Speed Inter-Chip USB) Phy
- Miscellaneous IPs and interfaces:
  - Three I^2S/SSI/AC97 supported
  - Five UARTs, up to 4.0 Mbps each:
    - Providing RS232 interface
    - Supporting 9-bit RS485 multidrop mode
    - One of the five UARTs (UART1) supports 8-wire while others four supports 4-wire. This is due to the SoC IOMUX limitation, since all UART IPs are identical.
  - Four eCSPI (Enhanced CSPI)
  - Three I^2C, supporting 400 kbps
  - Ethernet Controller, 10/100 Mbps
  - Four Pulse Width Modulators (PWM)
  - System JTAG Controller (SJC)
  - GPIO with interrupt capabilities
  - 8x8 Key Pad Port (KPP)
  - Sony Philips Digital Interface (SPDIF), Rx and Tx
  - Two Watchdog timers (WDOG)
  - Audio MUX (AUDMUX)

The i.MX 6SoloLite processor integrates advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use Software State Retention and Power Gating for ARM and MPE
- Support various levels of system power modes
- Use flexible clock gating control scheme

3 Modules List

The i.MX 6SoloLite processor contains a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX 6SoloLite Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
128x8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6SoloLite processor consists of 2-128x8-bit fuse box accessible through OCOTP_CTRL interface.
ARM	ARM Platform	ARM	The ARM Cortex-A9 platform consists of a Cortex-A9 core version r2p10 and associated sub-blocks, including Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, Watchdog, and CoreSight debug modules.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
CCM GPC SRC	Clock Control Module, Global Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6SoloLite platform. The Security Control Registers (SCR) of the CSU are set during boot time by the HAB and are locked to prevent further writing.
CTI-1 CTI-2 CTI-3 CTI-4 CTI-5	Cross Trigger Interfaces	Debug / Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
CTM	Cross Trigger Matrix	Debug / Trace	Cross Trigger Matrix IP is used to route triggering events between CTIs. The CTM module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DCP	Data co-processor	Security	This module provides support for general encryption and hashing functions typically used for security functions. Because its basic job is moving data from memory to memory, it also incorporates a memory-copy (memcopy) function for both debugging and as a more efficient method of copying data between memory blocks than the DMA-based approach.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC-1 uSDHC-2 uSDHC-2 uSDHC-4	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6SoloLite specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.2/4.3/4.4 including high-capacity (size > 2 GB) cards HC MMC. HW reset as specified for eMMC cards is supported at ports #3 and #4 only. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v1.10 • Fully compliant with SD Card Specification, Part A2, SD Host Controller Standard Specification, v2.00 All four ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) However, the SoC level integration and I/O muxing logic restrict the functionality to the following: • Instances #1 and #2 are primarily intended to serve as external slots or interfaces to on-board SDIO devices. These ports are equipped with “Card detection” and “Write Protection” pads and do not support HW reset • All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for Ports #1 and #2 in four bit configuration (SD interface). Port #3 is placed in his own independent power domain and port #4 shares power domain with some other interfaces.
WDOG-1	Watchdog	Timer Peripherals	The Watchdog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG-2 (TZ)	Watchdog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system’s security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode Software.
XTALOSC	Crystal Oscillator I/F	Clocking	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator.

Table 4. JTAG Controller Interface Summary (continued)

JTAG	I/O Type	On-Chip Termination
JTAG_TRSTB	Input	47 kΩ pull-up
JTAG_MOD	Input	100 kΩ pull-up

3.2 Recommended Connections for Unused Analog Interfaces

Table 5 shows the recommended connections for unused analog interfaces.

Table 5. Recommended Connections for Unused Analog Interfaces

Module	Pad Name	Recommendations if Unused?
CCM	CLK1_N, CLK1_P	Float
USB	USB_H1_DN, USB_H1_DP, USB_H1_VBUS, USB_OTG_CHD_B, USB_OTG_DN, USB_OTG_DP, USB_OTG_VBUS	Float

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6SoloLite processor.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 6SoloLite Chip-Level Conditions

For these characteristics, …	Topic appears …
Absolute Maximum Ratings	on page 18
BGA Case 2240 Package Thermal Resistance	on page 18
Operating Ranges	on page 21
External Clock Sources	on page 22
Maximal Supply Currents	on page 23
Low Power Mode Supply Currents	on page 24
USB PHY Current Consumption	on page 26

Table 8. Package Thermal Resistance Data (continued)

Rating	Board	Symbol	No Lid	Unit
Junction to Ambient[1] (at 200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	40	°C/W
	Four layer board (2s2p)	$R_{\theta JMA}$	24	°C/W
Junction to Board[2]	—	$R_{\theta JB}$	14	°C/W
Junction to Case[3] (Top)	—	$R_{\theta JCtop}$	9	°C/W
Junction to Package Top[4]	Natural Convection	Ψ_{JT}	2	°C/W

1 Junction-to-Ambient Thermal Resistance was determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-Board Thermal Resistance was determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

3 Junction-to-Case at the top of the package was determined by using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 9 provides the operating ranges of the i.MX 6SoloLite processor.

Table 9. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
Run mode: LDO enabled	VDD_ARM_IN	1.375[2]		1.5	V	LDO output set at 1.250V minimum for operation up to 996MHz.
		1.275[2]		1.5	V	LDO output set at 1.150V minimum for operation up to 792MHz
		1.075[2]		1.5	V	LDO output set at 0.95V minimum for operation up to 396MHz
		1.075[2]		1.5	V	LDO output set at 0.950V minimum for operation up to 192MHz
		1.050[2]		1.5	V	LDO output set at 0.9250V minimum for operation up to 24MHz
	VDD_SOC_IN[3] VDD_PU_IN	1.275[2,4]		1.5	V	VDD_SOC and VDD_PU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.15 V minimum.
Run mode: LDO bypassed	VDD_ARM_IN	1.250		1.3	V	LDO bypassed for operation up to 996 MHz.
		1.150		1.3	V	LDO bypassed for operation up to 792 MHz.
		0.950		1.3	V	LDO bypassed for operation up to 396 MHz.
		0.950		1.3	V	LDO bypassed for operation up to 192MHz
		0.925		1.3	V	LDO bypassed for operation up to 24MHz
	VDD_SOC_IN[3] VDD_PU_IN	1.15[4]		1.3	V	
Standby/DSM Mode	VDD_ARM_IN	0.9		1.3	V	See Table 12, "Stop Mode Current and Power Consumption," on page 24.
	VDD_SOC_IN VDD_PU_IN	0.9		1.3	V	
VDDHIGH internal Regulator	VDD_HIGH_IN[5]	2.8		3.3	V	Must match the range of voltges that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[5]	2.8		3.3	V	Should be supplied from the same supply as VDDHIGH_IN if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG1_VBUS USB_OTG2_VBUS	4.4		5.25	V	
DDR I/O supply	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2
		1.425	1.5	1.575	V	DDR3
	NVCC_DRAM_2P5	2.5	2.5	2.75	V	

[3] Recommended nominal frequency 32.768 kHz.

[4] External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 10 are required for use with Freescale BSPs to ensure precise time keeping and USB operation. For RTC_XTAL operation, two clock sources are available:

- On-chip 40 kHz ring oscillator: This clock source has the following characteristics:
  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit
  - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator
  - If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision timeout.

4.1.5 Maximal Supply Currents

The Power Virus numbers shown in Table 11 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The MMPF0100xxxx, Freescale's power management IC targeted for the i.MX 6x family, supports the Power Virus mode operating at 1% duty cycle. Higher duty cycles are allowed, but a robust thermal design is required for the increased system power dissipation.

See the i.MX 6SoloLite Power Consumption Measurement Application Note for more details on typical power consumption under various use case definitions.

Table 11. Maximal Supply Currents

Power Line	Conditions	Max Current	Unit
VDD_ARM_IN	1 GHz ARM clock based on Power Virus operation	1100	mA
VDD_SOC_IN	1 GHz ARM clock	650	mA
VDD_PU_IN	1 GHz ARM clock	150	mA
VDD_HIGH_IN	—	30[1]	mA
VDD_SNVS_IN	—	250[2]	µA

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the i.MX 6SoloLite reference manual for details on the power tree scheme recommended operation.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Digital Regulators (LDO_ARM, LDO_PU, LDO_SOC)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of their input supply ripple rejection and their on die trimming. This translates into more voltage for the die producing higher operating frequencies. These regulators have three basic modes.

- Bypass. The regulation FET is switched fully on passing the external voltage, DCDC_LOW, to the load unaltered. The analog part of the regulator is powered down in this state, removing any loss other than the IR drop through the power grid and FET.
- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

For additional information, see the i.MX 6SoloLite reference manual.

4.3.2 Analog Regulators

4.3.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDDHIGH_IN (see Table 9 for min and max input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. Since we are not testing the accuracy or the % regulation, and only testing with the LDO set to either 1.0V or 1.2V, this is the only range that is guaranteed. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 µF (2.2 µF should be considered the recommended minimum value), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For additional information, see the i.MX 6SoloLite reference manual.

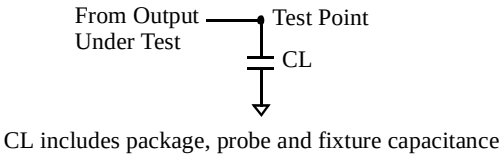

Figure 5. Load Circuit for Output

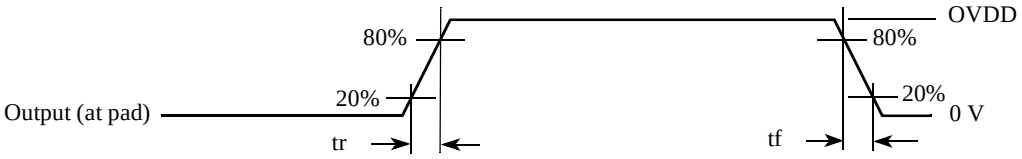

Figure 6. Output Transition Time Waveform

4.7.2 DDR I/O AC Parameters

The LPDDR2 interface mode fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3 interface mode fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 27 shows the AC parameters for DDR I/O operating in LPDDR2 mode.

Table 27. DDR I/O LPDDR2 Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.22	V
AC differential input high voltage[2]	Vidh(ac)	—	0.44	—	—	V
AC differential input low voltage	Vidl(ac)	—	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	-0.12	—	0.12	V
Over/undershoot peak	Vpeak	—	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.3	V-ns
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	50 Ω to Vref. 5 pF load. Drive impedance = 4 0 Ω ±30%	1.5	—	3.5	V/ns
		50 Ω to Vref. 5pF load. Drive impedance = 60 Ω ±30%	1	—	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr – Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) – Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 * OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 28 shows the AC parameters for DDR I/O operating in DDR3 mode.

Table 28. DDR I/O DDR3 Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.175	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.175	V
AC differential input voltage[2]	Vid(ac)	—	0.35	—	—	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	Vref – 0.15	—	Vref + 0.15	V
Over/undershoot peak	Vpeak	—	—	—	0.4	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.5	V-ns

4.8.3 DDR I/O Output Buffer Impedance

The LPDDR2 interface fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 32 shows DDR I/O output buffer impedance of i.MX 6SoloLite processor.

Table 32. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	Drive Strength (DSE) = 000 001 010 011 100 101 110 111	 Hi-Z 240 120 80 60 48 40 34	 Hi-Z 240 120 80 60 48 40 34	Ω

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 W external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is ±5% (max/min impedance) across PVTs.

4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6SoloLite processor.

4.9.1 Reset Timings Parameters

Figure 8 shows the reset timing and Table 33 lists the timing parameters.

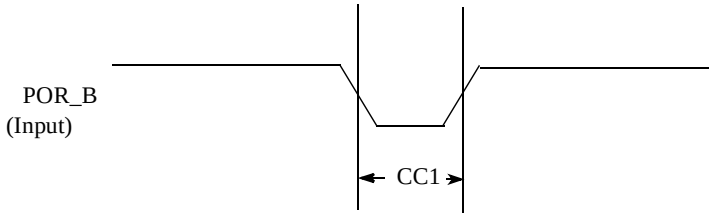

Figure 8. Reset Timing Diagram

Table 38. EIM Asynchronous Timing Parameters Table Relative Chip Select (continued)

Reference Number	Parameter	Determination by Synchronous measured parameters[1]	Min	Max	Unit
WE40A (muxed A/D)	CSx_B Valid to ADV_B Invalid	WE14 - WE6 + (ADVN + ADVA + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	3 + (ADVN + ADVA + 1 - CSA)	ns
WE41	CSx_B Valid to Output Data Valid	WE16 - WE6 - WCSA	—	3 - WCSA	ns
WE41A (muxed A/D)	CSx_B Valid to Output Data Valid	WE16 - WE6 + (WADVN + WADVA + ADH + 1 - WCSA)	—	3 + (WADVN + WADVA + ADH + 1 - WCSA)	ns
WE42	Output Data Invalid to CSx_B Invalid	WE17 - WE7 - CSN	—	3 - CSN	ns
MAXCO	Output maximum delay from internal driving ADDR/control FFs to chip outputs	10	—	—	ns
MAXCSO	Output maximum delay from CSx internal driving FFs to CSx out	10	—	—	ns
MAXDI	Data maximum delay from chip input data to its internal FF	6	—	—	ns
WE43	Input Data Valid to CSx_B Invalid	MAXCO - MAXCSO + MAXDI	MAXCO - MAXCSO + MAXDI	—	ns
WE44	CSx_B Invalid to Input Data invalid	0	0	—	ns
WE45	CSx_B Valid to BEy_B Valid (Write access)	WE12 - WE6 + (WBEA - CSA)	—	3 + (WBEA - CSA)	ns
WE46	BEy_B Invalid to CSx_B Invalid (Write access)	WE7 - WE13 + (WBEN - CSN)	—	-3 + (WBEN - CSN)	ns
MAXDTI	DTACK maximum delay from chip dtack input to its internal FF + 2 cycles for synchronization	10	—	—	ns
WE47	Dtack Active to CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	CSx_B Invalid to Dtack invalid	0	0	—	ns

1 For more information on configuration parameters mentioned in this table, see the i.MX 6SoloLite reference manual.

2 CS Assertion. This bit field determines when CS signal is asserted during read/write cycles.

3 CS Negation. This bit field determines when CS signal is negated during read/write cycles.

4 t is axi_clk cycle time.

5 BE Assertion. This bit field determines when BE signal is asserted during read cycles.

6 BE Negation. This bit field determines when BE signal is negated during read cycles.

4.10.2 CMOS Sensor Interface (CSI) Timing Parameters

4.10.2.0.1 Gated Clock Mode Timing

Figure 28 and Figure 29 shows the gated clock mode timings for CSI, and Table 45 describes the timing parameters (P1–P7) shown in the figures. A frame starts with a rising/falling edge on VSYNC, then HSYNC is asserted and holds for the entire line. The pixel clock is valid as long as HSYNC is asserted.

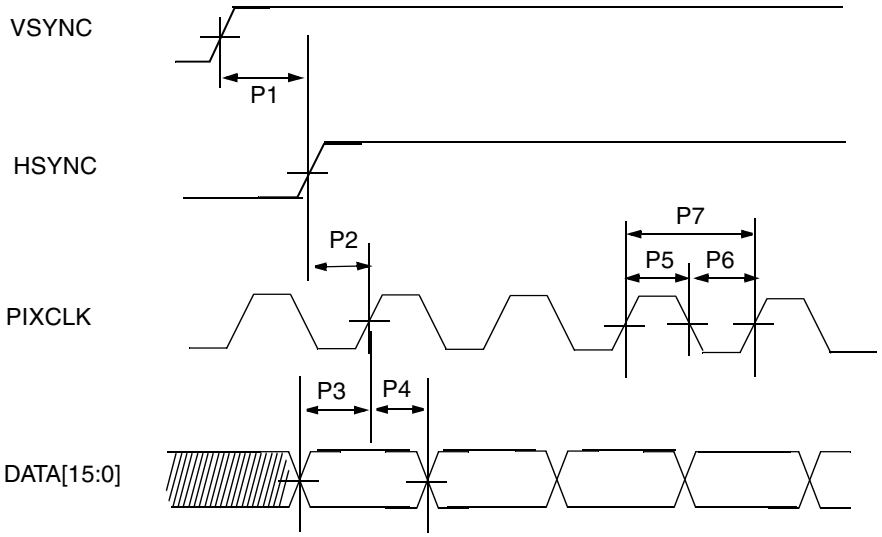

Figure 28. CSI Gated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

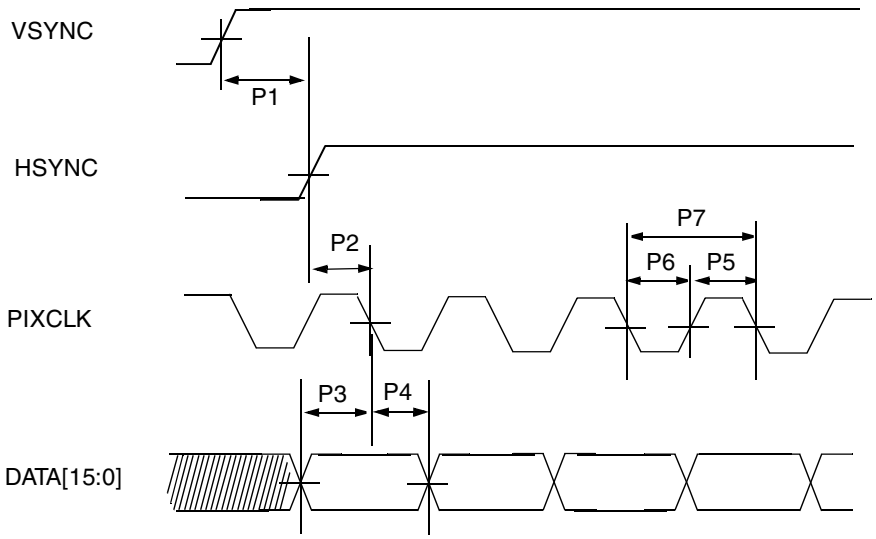

Figure 29. CSI Gated Clock Mode—Sensor Data at Rising Edge, Latch Data at Falling Edge

Table 62. SSI Transmitter Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.10.10.4 SSI Receiver Timing with External Clock

Figure 52 depicts the SSI receiver external clock timing and Table 65 lists the timing parameters for the receiver timing with the external clock.

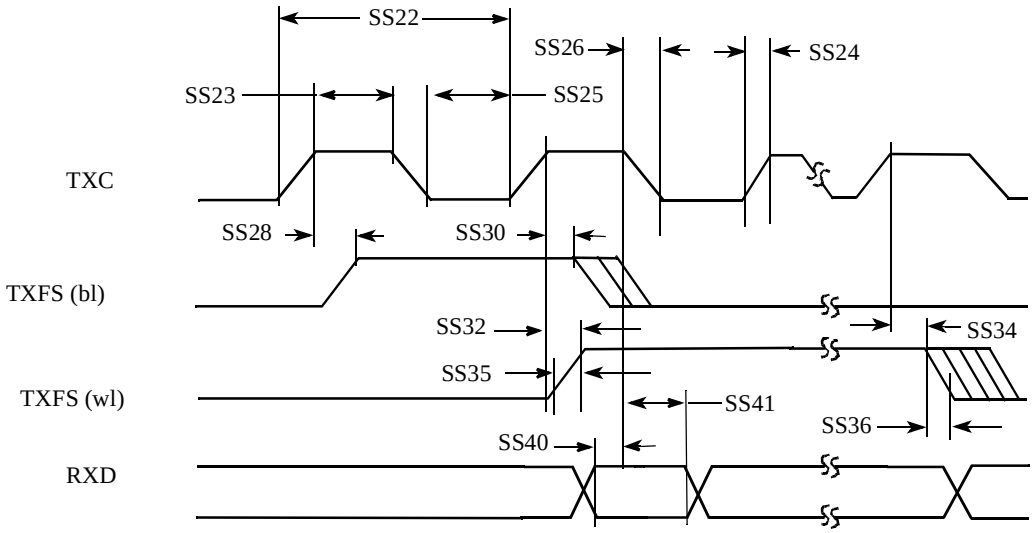

Figure 52. SSI Receiver External Clock Timing Diagram

Table 65. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	(Rx) CK high to FS (bl) high	–10	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10	—	ns
SS32	(Rx) CK high to FS (wl) high	–10	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10	—	ns
SS41	SRXD hold time after (Rx) CK low	2	—	ns

Table 78. 13 x 13, 0.5 mm BGA Package Details

Parameter	Symbol	Common Dimensions		
		Minimum	Normal	Maximum
Total Thickness	A	0.88	-	1.1
Stand Off	A1	0.16	-	0.26
Substrate Thickness	A2	0.26 REF		
Mold Thickness	A3	0.54 REF		
Body Size	D	13 BSC		
	E	13 BSC		
Ball Diameter		0.3		
Ball Opening		0.275		
Ball Width	b	0.27	-	0.37
Ball Pitch	e	0.5 BSC		
Ball Count	n	432		
Edge Ball Center to Center	D1	11.5 BSC		
	E1	11.5 BSC		
Body Center to Contact Ball	SD	0.25 BSC		
	SE	0.25 BSC		
Package Edge Tolerance	aaa	0.1		
Mold Flatness	bbb	0.1		
Coplanarity	ddd	0.08		
Ball Offset (Package)	eee	0.15		
Ball Offset (Ball)	fff	0.05		

6.1.2 13 x 13 mm Ground, Power, Sense, Not Connected and Reference Contact Assignments

Table 79 shows the device connection list for ground, power, sense, and reference contact signals.

Table 79. 13 x 13 mm Supplies Contact Assignment

Supply Rail Name	Ball(s) Position(s)	Remark
DDR_VREF	N5	
GND	A1, A4, A7, A24, C6, C10, C14, C19, D1, D2, E5, G1, G8, G9, G10, G11, G13, G14, G15, G17, G18, H3, H7, H18, H22, J5, K1, L7, L9, L10, L11, L12, L13, L14, L15, L16, M5, M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, M17, N3, N7, N8, N9, N10, N11, N12, N13, N14, N15, N16, N17, N22, P9, P10, P11, P12, P13, P14, P15, P16, R1, T5, U3, U7, U18, U22, V1, V8, V9, V10, V11, V12, V13, V14, V15, V16, V18, Y5, AA1, AA2, AB10, AB14, AB18, AC18, AD1, AD4, AD7, AD24	
GND_Kelvin	V17	Must be connected
GPANAIO	AD22	Analog pad
NVCC_1P2V	W7	
NVCC18_IO	E14, E15, M20, Y11	
NVCC33_IO	H10, H11, H14, H15, L18, M18, T19, U10, U11	
NVCC_DRAM	E6, Y6, G7, H6, J6, N6, P7, T6, U6, V7	Supply of the DDR Interface
NVCC_DRAM_2P5	M6	
NVCC_PLL	Y19	
NVCC_SD1		
NVCC_SD2		
NVCC_SD3		
VDD_ARM_CAP	J15, J16, J17, J18, K15, K16, K17, K18	Secondary Supply for the ARM0 and ARM1 Cores (internal regulator output—requires capacitor if internal regulator is used)
VDD_ARM_IN	J12, J13, J14, K12, K13, K14	Primary Supply, for the ARM0 and ARM1 Core' Regulator
VDD_HIGH_CAP	R14, R15, T14, T15	Secondary Supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used)
VDD_HIGH_IN	R12, R13, T12, T13	Primary Supply for the 2.5 V Regulator
VDD_PU_CAP	R7, R8, R9, T7, T8, T9	Secondary Supply for the VPU and GPU's (internal regulator output—requires capacitor if internal regulator is used)
VDD_PU_IN	R10, R11, T10, T11	

Table 80. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
RTC_XTALI	AB19	VDD_SNVS_CAP			RTC_XTALI	—	—
RTC_XTALO	AA19	VDD_SNVS_CAP			RTC_XTALO	—	—
SD1_CLK	B20	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[15]	Input	Keeper
SD1_CMD	B21	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[14]	Input	Keeper
SD1_DAT0	B23	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[11]	Input	Keeper
SD1_DAT1	A23	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[8]	Input	Keeper
SD1_DAT2	C22	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[13]	Input	Keeper
SD1_DAT3	B22	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[6]	Input	Keeper
SD1_DAT4	A22	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[12]	Input	Keeper
SD1_DAT5	A21	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[9]	Input	Keeper
SD1_DAT6	A20	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[7]	Input	Keeper
SD1_DAT7	A19	NVCC_SD1	GPIO	ALT5	gpio5_GPIO[10]	Input	Keeper
SD2_CLK	AC24	NVCC_SD2	GPIO	ALT5	gpio5_GPIO[5]	Input	Keeper
SD2_CMD	AB24	NVCC_SD2	GPIO	ALT5	gpio5_GPIO[4]	Input	Keeper
SD2_DAT0	AB22	NVCC_SD2	GPIO	ALT5	gpio5_GPIO[1]	Input	Keeper
SD2_DAT1	AB23	NVCC_SD2	GPIO	ALT5	gpio4_GPIO[30]	Input	Keeper
SD2_DAT2	AA22	NVCC_SD2	GPIO	ALT5	gpio5_GPIO[3]	Input	Keeper
SD2_DAT3	AA23	NVCC_SD2	GPIO	ALT5	gpio4_GPIO[28]	Input	Keeper
SD2_DAT4	AA24	NVCC_SD2	GPIO	ALT5	gpio5_GPIO[2]	Input	Keeper
SD2_DAT5	Y20	NVCC_SD2	GPIO	ALT5	gpio4_GPIO[31]	Input	Keeper
SD2_DAT6	Y21	NVCC_SD2	GPIO	ALT5	gpio4_GPIO[29]	Input	Keeper
SD2_DAT7	Y22	NVCC_SD2	GPIO	ALT5	gpio5_GPIO[0]	Input	Keeper
SD2_RST	Y23	NVCC_SD2	GPIO	ALT5	gpio4_GPIO[27]	Input	Keeper
SD3_CLK	AB11	NVCC_SD3	GPIO	ALT5	gpio5_GPIO[18]	Input	Keeper
SD3_CMD	AA11	NVCC_SD3	GPIO	ALT5	gpio5_GPIO[21]	Input	Keeper
SD3_DAT0	AC11	NVCC_SD3	GPIO	ALT5	gpio5_GPIO[19]	Input	Keeper
SD3_DAT1	AD11	NVCC_SD3	GPIO	ALT5	gpio5_GPIO[20]	Input	Keeper
SD3_DAT2	AC12	NVCC_SD3	GPIO	ALT5	gpio5_GPIO[16]	Input	Keeper
SD3_DAT3	AD12	NVCC_SD3	GPIO	ALT5	gpio5_GPIO[17]	Input	Keeper

7 Revision History

Table 83 provides a revision history for this data sheet.

Table 83. i.MX 6SoloLite Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 1	11/2012	• Updated Table 77, "Interfaces Allocation During Boot," on page 97.
Rev 0.1	11/2012	• Updated Table 8, "Package Thermal Resistance Data," on page 18. • Corrected title of Table 79, “13 x 13 mm Supplies Contact Assignment,” on page 100. • Corrected title of Table 81, “13 x 13 mm, 0.5 mm Pitch Ball Map,” on page 110.
Rev. 0	10/2012	• Initial public release.